

# HEF4093B

## Quad 2-input NAND Schmitt trigger

Rev. 9 — 15 December 2015

Product data sheet

### 1. General description

The HEF4093B is a quad two-input NAND gate. Each input has a Schmitt trigger circuit. The gate switches at different points for positive-going and negative-going signals. The difference between the positive voltage ( $V_{T+}$ ) and the negative voltage ( $V_{T-}$ ) is defined as hysteresis voltage ( $V_H$ ).

It operates over a recommended  $V_{DD}$  power supply range of 3 V to 15 V referenced to  $V_{SS}$  (usually ground). Unused inputs must be connected to  $V_{DD}$ ,  $V_{SS}$ , or another input.

### 2. Features and benefits

- Schmitt trigger input discrimination
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from  $-40\text{ °C}$  to  $+85\text{ °C}$  and  $-40\text{ °C}$  to  $+125\text{ °C}$
- Complies with JEDEC standard JESD 13-B

### 3. Applications

- Wave and pulse shapers
- Astable multivibrators
- Monostable multivibrators

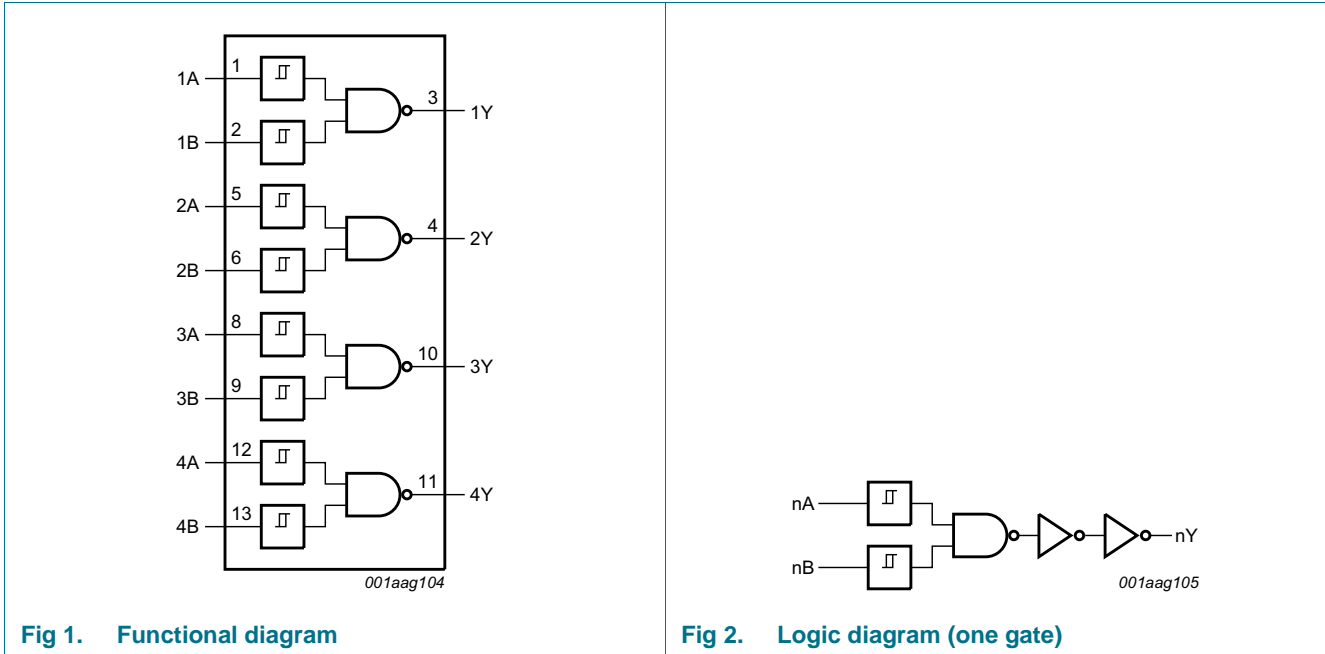
### 4. Ordering information

Table 1. Ordering information

All types operate from  $-40\text{ °C}$  to  $+125\text{ °C}$

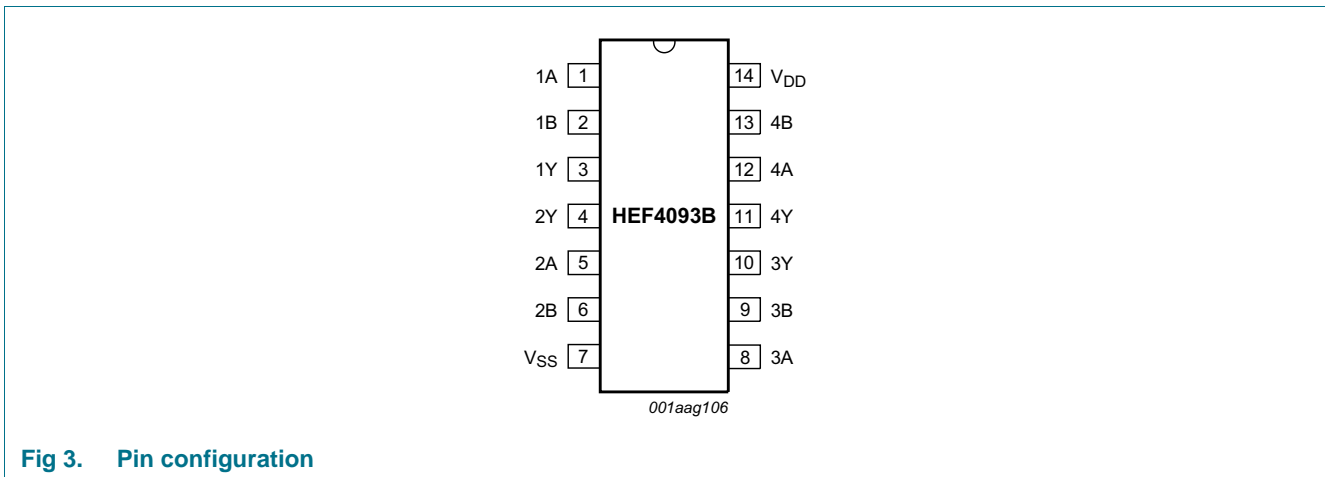
Type number	Package		
	Name	Description	Version
HEF4093BT	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1

## 5. Functional diagram



## 6. Pinning information

### 6.1 Pinning



## 6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A to 4A	1, 5, 8, 12	input
1B to 4B	2, 6, 9, 13	input
1Y to 4Y	3, 4, 10, 11	output
V <sub>DD</sub>	14	supply voltage
V <sub>SS</sub>	7	ground (0 V)

## 7. Functional description

Table 3. Function table<sup>[1]</sup>

Input		Output
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

[1] H = HIGH voltage level; L = LOW voltage level.

## 8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to V<sub>SS</sub> = 0 V (ground).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DD</sub>	supply voltage		-0.5	+18	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < -0.5 V or V <sub>I</sub> > V <sub>DD</sub> + 0.5 V	-	±10	mA
V <sub>I</sub>	input voltage		-0.5	V <sub>DD</sub> + 0.5	V
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < -0.5 V or V <sub>O</sub> > V <sub>DD</sub> + 0.5 V	-	±10	mA
I <sub>I/O</sub>	input/output current		-	±10	mA
I <sub>DD</sub>	supply current		-	50	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
T <sub>amb</sub>	ambient temperature		-40	+125	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +125 °C			
		SO14 <sup>[1]</sup>	-	500	mW
P	power dissipation	per output	-	100	mW

[1] For SO14 packages: above T<sub>amb</sub> = 70 °C, P<sub>tot</sub> derates linearly with 8 mW/K.

## 9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD}$	supply voltage		3	15	V
$V_I$	input voltage		0	$V_{DD}$	V
$T_{amb}$	ambient temperature	in free air	-40	+125	°C

## 10. Static characteristics

Table 6. Static characteristics

$V_{SS} = 0$  V;  $V_I = V_{SS}$  or  $V_{DD}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	$V_{DD}$	$T_{amb} = -40$ °C		$T_{amb} = +25$ °C		$T_{amb} = +85$ °C		$T_{amb} = +125$ °C		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
$V_{OH}$	HIGH-level output voltage	$ I_O  < 1$ $\mu$ A	5 V	4.95	-	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	14.95	-	V
$V_{OL}$	LOW-level output voltage	$ I_O  < 1$ $\mu$ A	5 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	-	0.05	V
$I_{OH}$	HIGH-level output current	$V_O = 2.5$ V	5 V	-	-1.7	-	-1.4	-	-1.1	-	-1.1	mA
		$V_O = 4.6$ V	5 V	-	-0.64	-	-0.5	-	-0.36	-	-0.36	mA
		$V_O = 9.5$ V	10 V	-	-1.6	-	-1.3	-	-0.9	-	-0.9	mA
		$V_O = 13.5$ V	15 V	-	-4.2	-	-3.4	-	-2.4	-	-2.4	mA
$I_{OL}$	LOW-level output current	$V_O = 0.4$ V	5 V	0.64	-	0.5	-	0.36	-	0.36	-	mA
		$V_O = 0.5$ V	10 V	1.6	-	1.3	-	0.9	-	0.9	-	mA
		$V_O = 1.5$ V	15 V	4.2	-	3.4	-	2.4	-	2.4	-	mA
$I_I$	input leakage current		15 V	-	$\pm 0.1$	-	$\pm 0.1$	-	$\pm 1.0$	-	$\pm 1.0$	$\mu$ A
$I_{DD}$	supply current	all valid input combinations; $I_O = 0$ A	5 V	-	0.25	-	0.25	-	7.5	-	7.5	$\mu$ A
			10 V	-	0.5	-	0.5	-	15.0	-	15.0	$\mu$ A
			15 V	-	1.0	-	1.0	-	30.0	-	30.0	$\mu$ A
$C_I$	input capacitance			-	-	-	7.5	-	-	-	pF	

## 11. Dynamic characteristics

**Table 7. Dynamic characteristics**

$T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $C_L = 50\text{ pF}$ ;  $t_r = t_f \leq 20\text{ ns}$ ; wave forms see [Figure 4](#); test circuit see [Figure 5](#); unless otherwise specified.

Symbol	Parameter	Conditions	V <sub>DD</sub>	Extrapolation formula <sup>[1]</sup>	Min	Typ	Max	Unit
t <sub>PHL</sub>	HIGH to LOW propagation delay	nA or nB to nY	5 V	$63\text{ ns} + (0.55\text{ ns/pF})C_L$	-	90	185	ns
			10 V	$29\text{ ns} + (0.23\text{ ns/pF})C_L$	-	40	80	ns
			15 V	$22\text{ ns} + (0.16\text{ ns/pF})C_L$	-	30	60	ns
t <sub>PLH</sub>	LOW to HIGH propagation delay	nA or nB to nY	5 V	$58\text{ ns} + (0.55\text{ ns/pF})C_L$	-	85	170	ns
			10 V	$29\text{ ns} + (0.23\text{ ns/pF})C_L$	-	40	80	ns
			15 V	$22\text{ ns} + (0.16\text{ ns/pF})C_L$	-	30	60	ns
t <sub>THL</sub>	HIGH to LOW output transition time	nY to LOW	5 V	$10\text{ ns} + (1.00\text{ ns/pF})C_L$	-	60	120	ns
			10 V	$9\text{ ns} + (0.42\text{ ns/pF})C_L$	-	30	60	ns
			15 V	$6\text{ ns} + (0.28\text{ ns/pF})C_L$	-	20	40	ns
t <sub>TLH</sub>	LOW to HIGH output transition time	nA or nB to HIGH	5 V	$10\text{ ns} + (1.00\text{ ns/pF})C_L$	-	60	120	ns
			10 V	$9\text{ ns} + (0.42\text{ ns/pF})C_L$	-	30	60	ns
			15 V	$6\text{ ns} + (0.28\text{ ns/pF})C_L$	-	20	40	ns

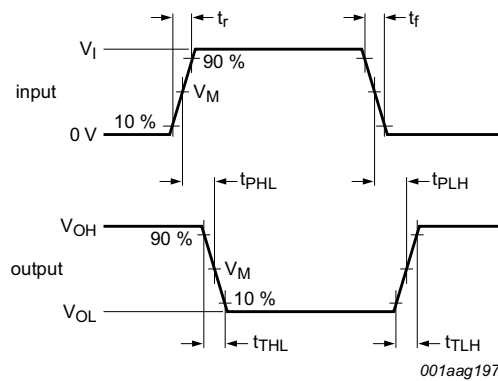
[1] Typical value of the propagation delay and output transition time can be calculated with the extrapolation formula ( $C_L$  in pF).

**Table 8. Dynamic power dissipation**

$V_{SS} = 0\text{ V}$ ;  $t_r = t_f \leq 20\text{ ns}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .

Symbol	Parameter	V <sub>DD</sub>	Typical formula	where:
P <sub>D</sub>	dynamic power dissipation	5 V	$P_D = 1300 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2\text{ (}\mu\text{W)}$	$f_i$ = input frequency in MHz; $f_o$ = output frequency in MHz; $C_L$ = output load capacitance in pF; $\Sigma(f_o \times C_L)$ = sum of the outputs; $V_{DD}$ = supply voltage in V.
		10 V	$P_D = 6400 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2\text{ (}\mu\text{W)}$	
		15 V	$P_D = 18700 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2\text{ (}\mu\text{W)}$	

## 12. Waveforms

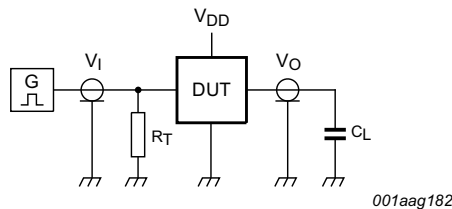


Measurement points are given in [Table 9](#).  
 Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.  
 $t_r$ ,  $t_f$  = input rise and fall times.

**Fig 4. Propagation delay and output transition time**

**Table 9. Measurement points**

Supply voltage	Input	Output
$V_{DD}$	$V_M$	$V_M$
5 V to 15 V	$0.5V_{DD}$	$0.5V_{DD}$



Test data given in [Table 10](#).  
 Definitions for test circuit:  
 DUT = Device Under Test.  
 $C_L$  = load capacitance including jig and probe capacitance.  
 $R_T$  = termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator.

**Fig 5. Test circuit for measuring switching times**

**Table 10. Test data**

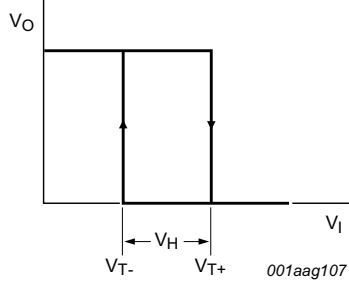
Supply voltage	Input		Load
$V_{DD}$	$V_I$	$t_r, t_f$	$C_L$
5 V to 15 V	$V_{SS}$ or $V_{DD}$	$\leq 20$ ns	50 pF

### 13. Transfer characteristics

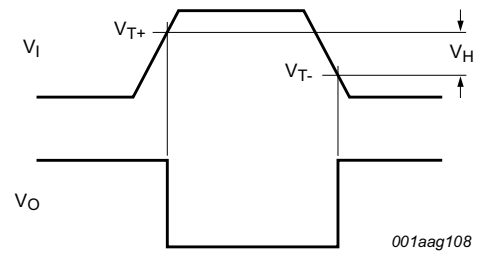
**Table 11. Transfer characteristics**

$V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ °C}$ ; see [Figure 6](#) and [Figure 7](#).

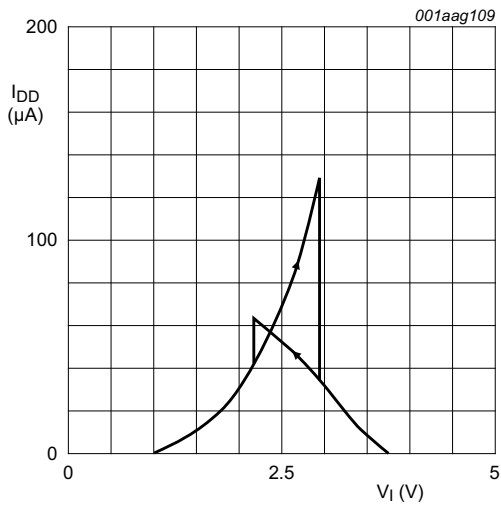
Symbol	Parameter	Conditions	$V_{DD}$	Min	Typ	Max	Unit
$V_{T+}$	positive-going threshold voltage		5 V	1.9	2.9	3.5	V
			10 V	3.6	5.2	7	V
			15 V	4.7	7.3	11	V
$V_{T-}$	negative-going threshold voltage		5 V	1.5	2.2	3.1	V
			10 V	3	4.2	6.4	V
			15 V	4	6.0	10.3	V
$V_H$	hysteresis voltage		5 V	0.4	0.7	-	V
			10 V	0.6	1.0	-	V
			15 V	0.7	1.3	-	V



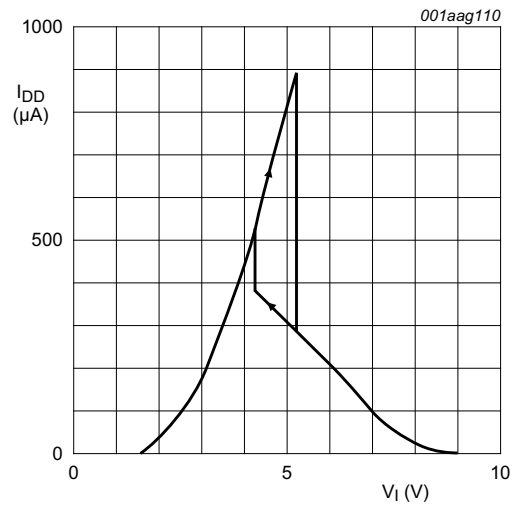
**Fig 6. Transfer characteristic**



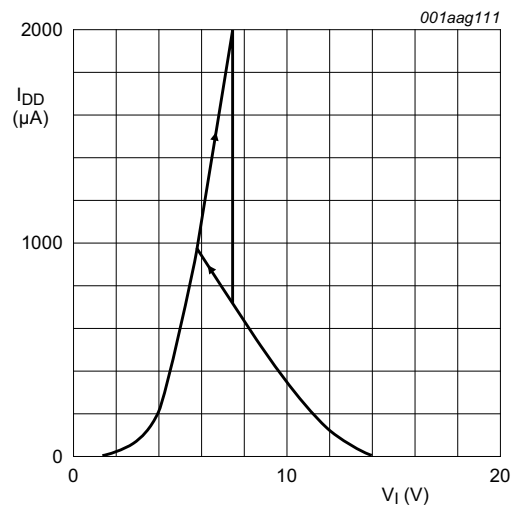
**Fig 7. Waveforms showing definition of  $V_{T+}$  and  $V_{T-}$  (between limits at 30 % and 70 %) and  $V_H$**



a.  $V_{DD} = 5\text{ V}$ ;  $T_{amb} = 25\text{ }^\circ\text{C}$



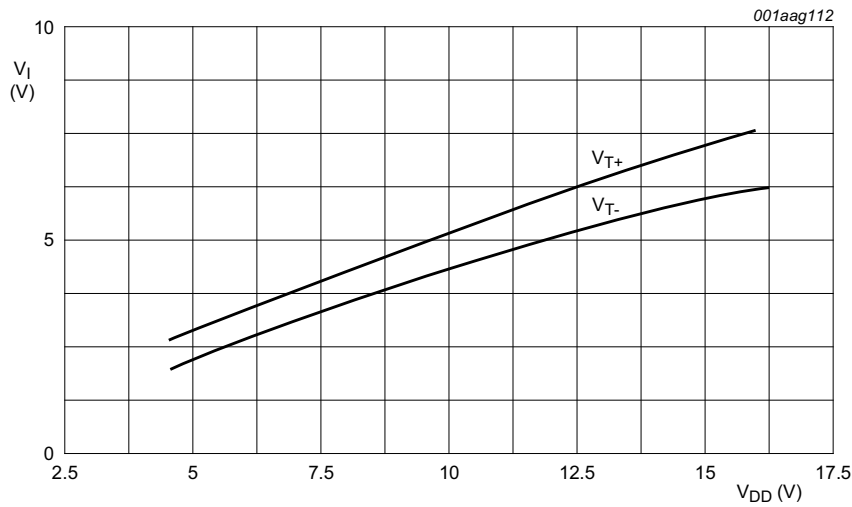
b.  $V_{DD} = 10\text{ V}$ ;  $T_{amb} = 25\text{ }^\circ\text{C}$



c.  $V_{DD} = 15\text{ V}$ ;  $T_{amb} = 25\text{ }^\circ\text{C}$

**Fig 8. Typical drain current as a function of input**





T<sub>amb</sub> = 25 °C.

Fig 9. Typical switching levels as a function of supply voltage

## 14. Application information

Some examples of applications for the HEF4093B are:

- Wave and pulse shapers
- Astable multivibrators
- Monostable multivibrators

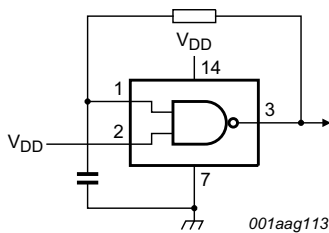


Fig 10. Astable multivibrator

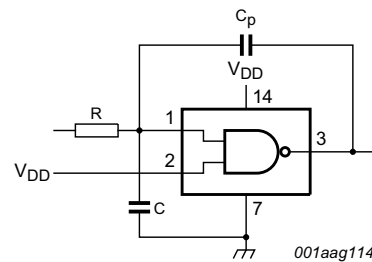


Fig 11. Schmitt trigger driven via a high-impedance input

If a Schmitt trigger is driven via a high-impedance ( $R > 1 \text{ k}\Omega$ ), then it is necessary to incorporate a capacitor C with a value of  $\frac{C}{C_p} > \frac{V_{DD} - V_{SS}}{V_H}$ ; otherwise oscillation can occur on the edges of a pulse.

C<sub>p</sub> is the external parasitic capacitance between inputs and output; the value depends on the circuit board layout.

**Remark:** The two inputs may be connected together, but this will result in a larger through-current at the moment of switching.

15. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

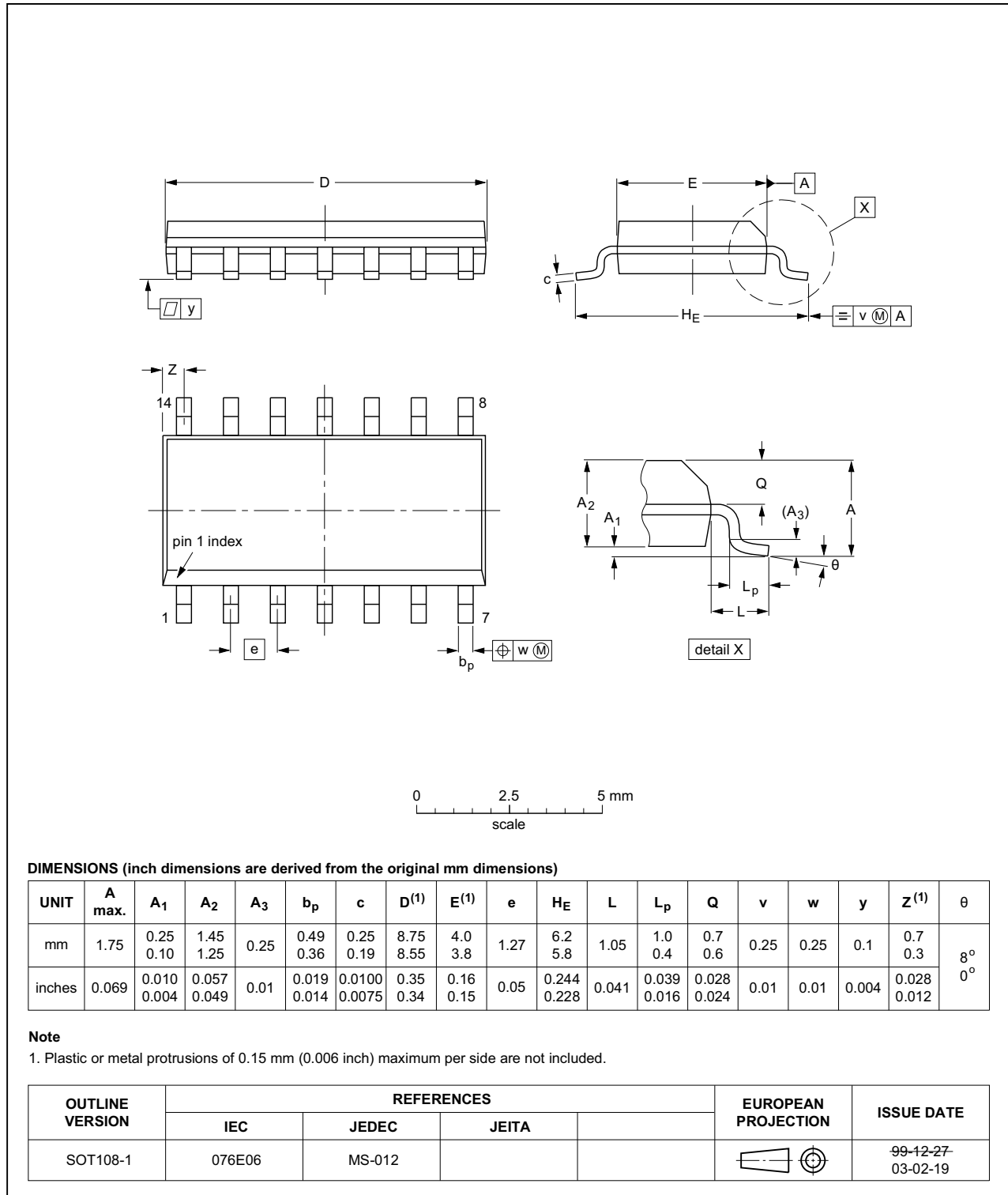


Fig 12. Package outline SOT108-1 (SO14)

## 16. Abbreviations

Table 12. Abbreviations

Acronym	Description
DUT	Device Under Test

## 17. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4093B v.9	20151215	Product data sheet	-	HEF4093B v.8
Modifications:	<ul style="list-style-type: none"> <li>Type number HEF4093BP (SOT27-1) removed.</li> </ul>			
HEF4093B v.8	20111121	Product data sheet	-	HEF4093B v.7
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Table 6</a>: I<sub>OH</sub> minimum values changed to maximum</li> </ul>			
HEF4093B v.7	20100901	Product data sheet	-	HEF4093B v.6
HEF4093B v.6	20091202	Product data sheet	-	HEF4093B v.5
HEF4093B v.5	20090728	Product data sheet	-	HEF4093B v.4
HEF4093B v.4	20080612	Product data sheet	-	HEF4093B_CNV v.3
HEF4093B_CNV v.3	19950101	Product specification	-	HEF4093B_CNV v.2
HEF4093B_CNV v.2	19950101	Product specification	-	-

## 18. Legal information

### 18.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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[NLX1G11AMUTCG](#) [NLX1G97MUTCG](#) [74LS38](#) [74LVC32ADTR2G](#) [MC74HCT20ADTR2G](#) [NLV17SZ00DFT2G](#) [NLV74HC02ADR2G](#)  
[74HC32S14-13](#) [74LS133](#) [74LVC1G86Z-7](#) [74LVC2G08RA3-7](#) [NLV74HC08ADTR2G](#) [NLV74HC14ADR2G](#) [NLV74HC20ADR2G](#)  
[NLVVHC1G09DFT1G](#) [NLX2G86MUTCG](#) [74LVC2G02HD4-7](#) [NLU1G00AMUTCG](#) [74LVC2G32RA3-7](#) [74LVC2G00HD4-7](#)  
[NL17SG02P5T5G](#) [74LVC2G00HK3-7](#) [74LVC2G86HK3-7](#) [NLX1G99DMUTWG](#) [NLVVHC1G00DFT2G](#) [NLVHC1G08DFT2G](#)  
[NLV7SZ57DFT2G](#) [NLV74VHC04DTR2G](#) [NLV27WZ86USG](#) [NLV27WZ00USG](#) [NLU1G86CMUTCG](#) [NLU1G08CMUTCG](#)  
[NL17SZ32P5T5G](#) [NL17SZ00P5T5G](#) [NL17SH02P5T5G](#) [74AUP2G00RA3-7](#) [NLV74HC02ADTR2G](#) [NLX1G332CMUTCG](#)  
[NL17SG86P5T5G](#) [NL17SZ05P5T5G](#) [NLV74VHC00DTR2G](#) [NLVVHC1G02DFT1G](#) [NL17SZ38DBVT1G](#)