

# HEF4794B-Q100

## 8-stage shift-and-store register LED driver

Rev. 2 — 7 November 2018

Product data sheet

### 1. General description

The HEF4794B-Q100 is an 8-stage serial shift register. It has a storage latch associated with each stage for strobing data from the serial input (D) to the parallel LED driver outputs (QP0 to QP7). Data is shifted on the positive-going clock (CP) transitions. The data in each shift register stage is transferred to the storage register when the strobe input (STR) is HIGH. Data in the storage register appears at the outputs whenever the output enable input (OE) signal is HIGH.

Two serial outputs (QS1 and QS2) are available for cascading a number of HEF4794B-Q100 devices. Serial data is available at QS1 on positive-going clock edges to allow high-speed operation in cascaded systems with a fast clock rise time. The same serial data is available at QS2 on the next negative going clock edge. This is used for cascading HEF4794B-Q100 devices when the clock has a slow rise time.

It operates over a recommended  $V_{DD}$  power supply range of 3 V to 15 V referenced to  $V_{SS}$  (usually ground). Unused inputs must be connected to  $V_{DD}$ ,  $V_{SS}$ , or another input.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

### 2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- ESD protection:
  - MIL-STD-883, method 3015 exceeds 2000 V
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V (C = 200 pF; R = 0 Ω)
- Complies with JEDEC standard JESD 13-B

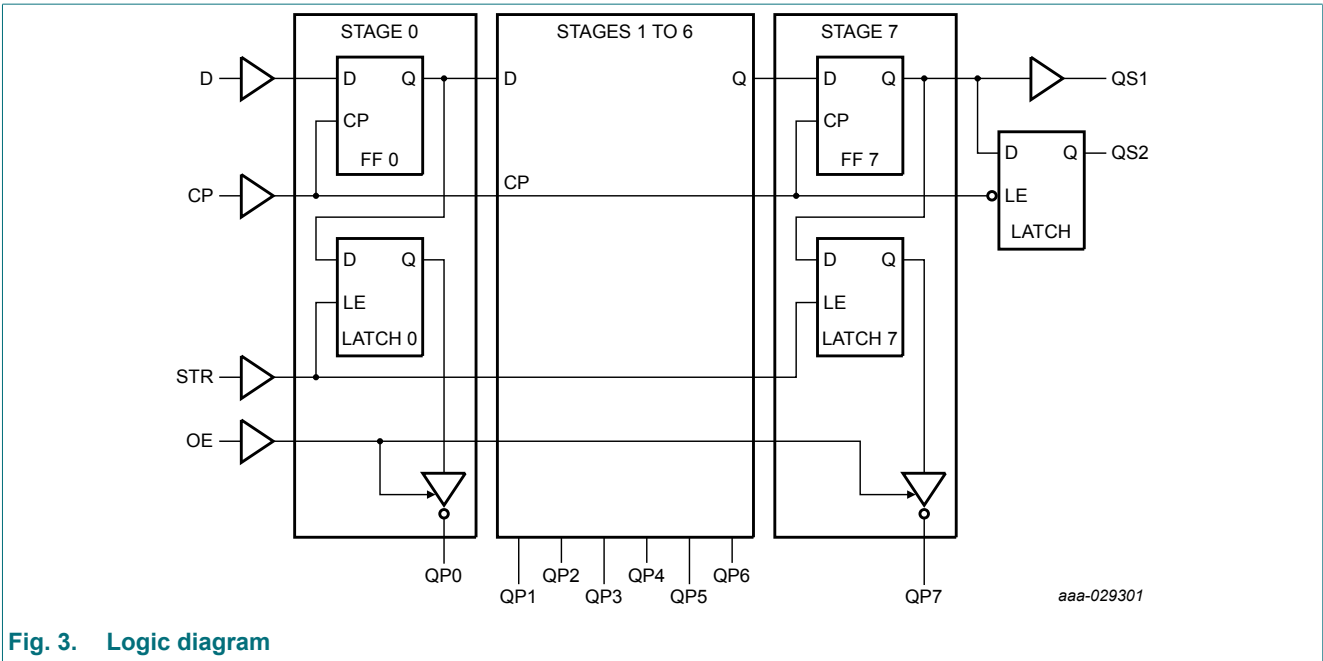
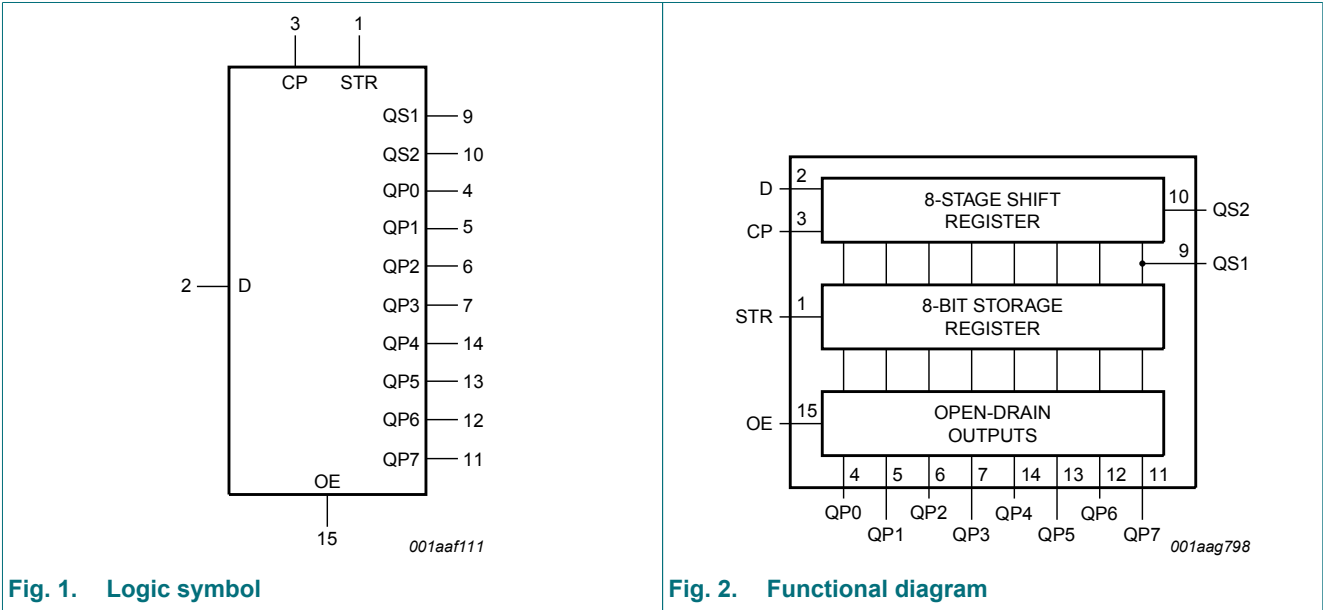
### 3. Ordering information

**Table 1. Ordering information**

All types operate from -40 °C to +125 °C.

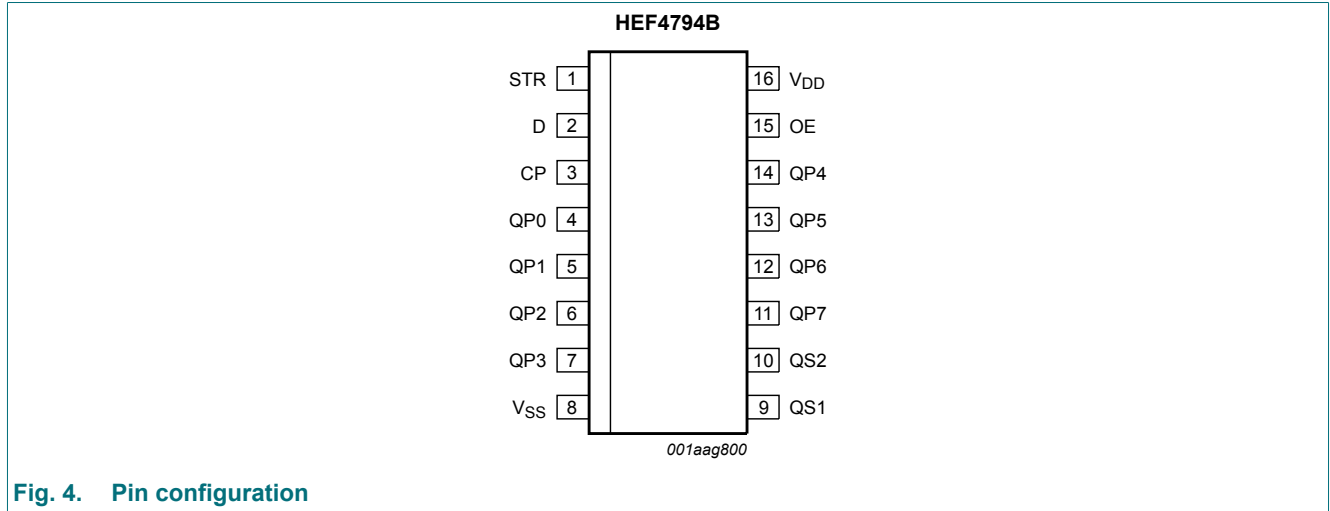
Type number	Package		
	Name	Description	Version
HEF4794BT-Q100	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

4. Functional diagram



## 5. Pinning information

### 5.1. Pinning



### 5.2. Pin description

**Table 2. Pin description**

Symbol	Pin	Description
D	2	serial input
QP0 to QP7	4, 5, 6, 7, 14, 13, 12, 11	parallel output (open-drain)
QS1	9	serial output
QS2	10	serial output
CP	3	clock input
STR	1	strobe input
OE	15	output enable input
V <sub>DD</sub>	16	supply voltage
V <sub>SS</sub>	8	ground (0 V)

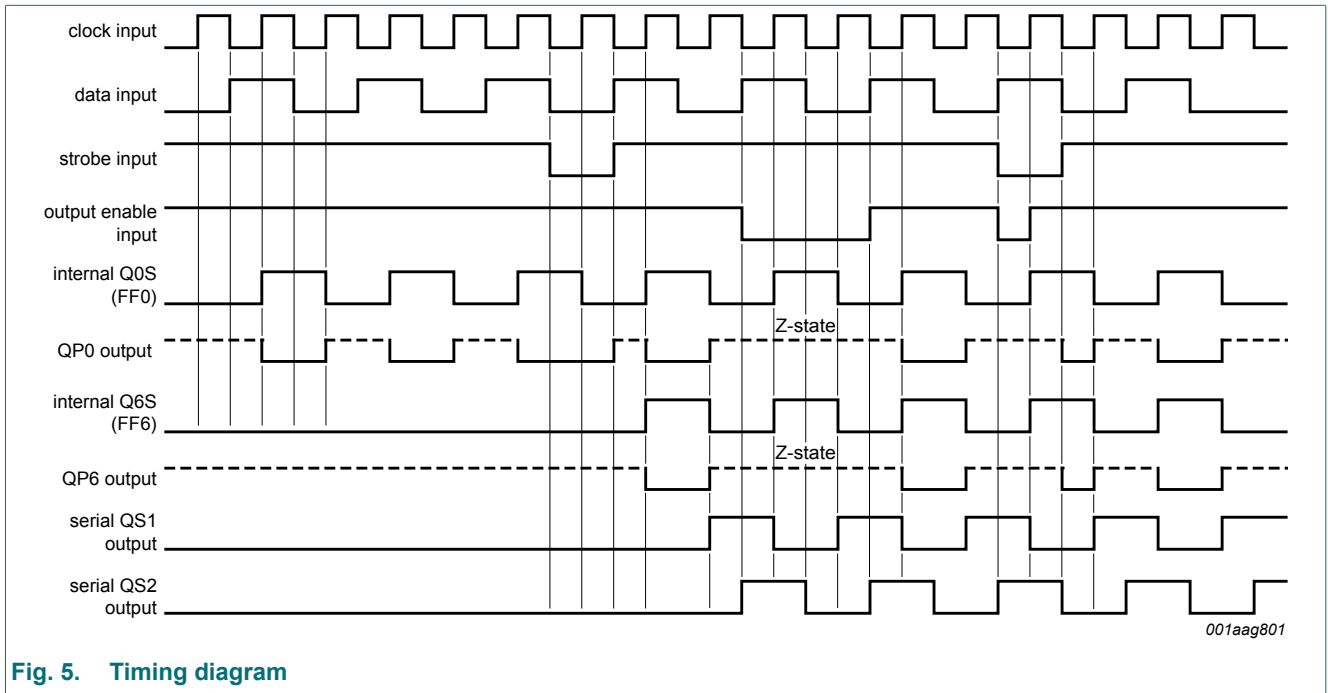
## 6. Functional description

**Table 3. Function table**

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state;  
 ↑ = LOW-to-HIGH clock transition; ↓ = HIGH-to-LOW clock transition.

Input				Parallel output		Serial output	
CP	OE	STR	D	QP0	QPn	QS1[1]	QS2[2]
↑	L	X	X	Z	Z	Q6S	no change
↓	L	X	X	Z	Z	n.c.	Q7S
↑	H	L	X	no change	no change	Q6S	no change
↑	H	H	L	Z	QPn - 1	Q6S	no change
↑	H	H	H	L	QPn - 1	Q6S	no change
↓	H	H	H	no change	no change	no change	Q7S

- [1] Q6S = the data in register stage 6 before the LOW to HIGH clock transition.
- [2] Q7S = the data in register stage 7 before the HIGH to LOW clock transition.



**Fig. 5. Timing diagram**

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD}$	supply voltage		-0.5	+18	V
$I_{IK}$	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{DD} + 0.5\text{ V}$	-	$\pm 10$	mA
$V_I$	input voltage		-0.5	$V_{DD} + 0.5$	V
$I_{OK}$	output clamping current	QSn outputs; $V_O < -0.5\text{ V}$ or $V_O > V_{DD} + 0.5\text{ V}$	-	$\pm 10$	mA
		QPn outputs; $V_O < -0.5\text{ V}$	-	40	mA
$I_I$	input leakage current		-	$\pm 10$	mA
$I_O$	output current	QSn outputs	-	$\pm 10$	mA
		QPn outputs	-	40	mA
$T_{stg}$	storage temperature		-65	+150	°C
$T_{amb}$	ambient temperature		-40	+125	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$			
		SO16 package [1]	-	500	mW
$P$	power dissipation	per output	-	100	mW

[1] For SO16 package:  $P_{tot}$  derates linearly with 8 mW/K above 70 °C.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD}$	supply voltage		3	15	V
$V_I$	input voltage		0	$V_{DD}$	V
$T_{amb}$	ambient temperature	in free air	-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{DD} = 5\text{ V}$	-	3.75	$\mu\text{s/V}$
		$V_{DD} = 10\text{ V}$	-	0.5	$\mu\text{s/V}$
		$V_{DD} = 15\text{ V}$	-	0.08	$\mu\text{s/V}$

## 9. Static characteristics

**Table 6. Static characteristics**

$V_{SS} = 0\text{ V}$ ;  $V_I = V_{SS}$  or  $V_{DD}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	V <sub>DD</sub>	T <sub>amb</sub> = -40 °C		T <sub>amb</sub> = 25 °C		T <sub>amb</sub> = 85 °C		T <sub>amb</sub> = 125 °C		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
V <sub>IH</sub>	HIGH-level input voltage	I <sub>ol</sub>   < 1 μA	5 V	3.5	-	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	11.0	-	V
V <sub>IL</sub>	LOW-level input voltage	I <sub>ol</sub>   < 1 μA	5 V	-	1.5	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	-	4.0	V
V <sub>OH</sub>	HIGH-level output voltage	QSn outputs;  I <sub>ol</sub>   < 1 μA	5 V	4.95	-	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	14.95	-	V
V <sub>OL</sub>	LOW-level output voltage	QSn outputs;  I <sub>ol</sub>   < 1 μA	5 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	-	0.05	V
		QPn outputs;  I <sub>ol</sub>   < 20 mA	5 V	-	0.75	-	0.75	-	1.5	-	1.5	V
			10 V	-	0.75	-	0.75	-	1.5	-	1.5	V
			15 V	-	0.75	-	0.75	-	1.5	-	1.5	V
I <sub>OH</sub>	HIGH-level output current	QSn outputs										
		V <sub>O</sub> = 2.5 V	5 V	-	-1.7	-	-1.4	-	-1.1	-	-1.1	mA
		V <sub>O</sub> = 4.6 V	5 V	-	-0.64	-	-0.5	-	-0.36	-	-0.36	mA
		V <sub>O</sub> = 9.5 V	10 V	-	-1.6	-	-1.3	-	-0.9	-	-0.9	mA
		V <sub>O</sub> = 13.5 V	15 V	-	-4.2	-	-3.4	-	-2.4	-	-2.4	mA
I <sub>OL</sub>	LOW-level output current	QSn outputs										
		V <sub>O</sub> = 0.4 V	5 V	0.64	-	0.5	-	0.36	-	0.36	-	mA
		V <sub>O</sub> = 0.5 V	10 V	1.6	-	1.3	-	0.9	-	0.9	-	mA
		V <sub>O</sub> = 1.5 V	15 V	4.2	-	3.4	-	2.4	-	2.4	-	mA
I <sub>I</sub>	input leakage current		15 V	-	±0.1	-	±0.1	-	±1.0	-	±1.0	μA
I <sub>OZ</sub>	OFF-state output current	QPn output is HIGH; V <sub>O</sub> = 15 V	5 V	-	2	-	2	-	15	-	15	μA
			10 V	-	2	-	2	-	15	-	15	μA
			15 V	-	2	-	2	-	15	-	15	μA
I <sub>DD</sub>	supply current	I <sub>O</sub> = 0 A	5 V	-	5	-	5	-	150	-	150	μA
			10 V	-	10	-	10	-	300	-	300	μA
			15 V	-	20	-	20	-	600	-	600	μA
C <sub>I</sub>	input capacitance		-	-	-	-	-	7.5	-	-	-	pF

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

$V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ °C}$  unless otherwise specified. For test circuit, see Fig. 10.

Symbol	Parameter	Conditions	V <sub>DD</sub>	Extrapolation formula	Min	Typ	Max	Unit
t <sub>PHL</sub>	HIGH to LOW propagation delay	CP to QS1; see Fig. 6	5 V [1]	132 ns + (0.55 ns/pF)C <sub>L</sub>	-	160	320	ns
			10 V	53 ns + (0.23 ns/pF)C <sub>L</sub>	-	65	130	ns
			15 V	37 ns + (0.16 ns/pF)C <sub>L</sub>	-	45	90	ns
		CP to QS2; see Fig. 6	5 V	92 ns + (0.55 ns/pF)C <sub>L</sub>	-	120	240	ns
			10 V	39 ns + (0.23 ns/pF)C <sub>L</sub>	-	50	100	ns
			15 V	32 ns + (0.16 ns/pF)C <sub>L</sub>	-	40	80	ns
t <sub>PLH</sub>	LOW to HIGH propagation delay	CP to QS1; see Fig. 6	5 V [1]	102 ns + (0.55 ns/pF)C <sub>L</sub>	-	130	260	ns
			10 V	44 ns + (0.23 ns/pF)C <sub>L</sub>	-	55	110	ns
			15 V	32 ns + (0.16 ns/pF)C <sub>L</sub>	-	40	80	ns
		CP to QS2; see Fig. 6	5 V	102 ns + (0.55 ns/pF)C <sub>L</sub>	-	130	260	ns
			10 V	49 ns + (0.23 ns/pF)C <sub>L</sub>	-	60	120	ns
			15 V	37 ns + (0.16 ns/pF)C <sub>L</sub>	-	45	90	ns
t <sub>PZL</sub>	OFF-state to LOW propagation delay	CP to QPn; see Fig. 6	5 V		-	240	480	ns
			10 V		-	80	160	ns
			15 V		-	55	110	ns
		STR to QPn; see Fig. 7	5 V		-	140	280	ns
			10 V		-	70	140	ns
			15 V		-	55	110	ns
t <sub>PLZ</sub>	LOW to OFF-state propagation delay	CP to QPn; see Fig. 6	5 V		-	170	340	ns
			10 V		-	75	150	ns
			15 V		-	60	120	ns
		STR to QPn; see Fig. 7	5 V		-	100	200	ns
			10 V		-	40	100	ns
			15 V		-	35	70	ns
t <sub>en</sub>	enable time	OE to QPn; see Fig. 8	5 V [2]		-	100	200	ns
			10 V		-	55	110	ns
			15 V		-	50	100	ns
t <sub>dis</sub>	disable time	OE to QPn; see Fig. 8	5 V [2]		-	80	160	ns
			10 V		-	40	80	ns
			15 V		-	30	60	ns
t <sub>t</sub>	transition time	QS1, QS2; see Fig. 6	5 V [1][3]	35 ns + (1.00 ns/pF)C <sub>L</sub>	-	85	170	ns
			10 V	19 ns + (0.42 ns/pF)C <sub>L</sub>	-	40	80	ns
			15 V	16 ns + (0.28 ns/pF)C <sub>L</sub>	-	30	60	ns
t <sub>w</sub>	pulse width	CP LOW and HIGH; see Fig. 6	5 V		60	30	-	ns
			10 V		30	15	-	ns
			15 V		24	12	-	ns
		STR HIGH; see Fig. 7	5 V		80	40	-	ns
			10 V		60	30	-	ns
			15 V		24	12	-	ns

Symbol	Parameter	Conditions	V <sub>DD</sub>	Extrapolation formula	Min	Typ	Max	Unit
t <sub>su</sub>	set-up time	D to CP; see Fig. 9	5 V		60	30	-	ns
			10 V		20	10	-	ns
			15 V		15	5	-	ns
t <sub>h</sub>	hold time	D to CP; see Fig. 9	5 V		+5	-15	-	ns
			10 V		20	5	-	ns
			15 V		20	5	-	ns
f <sub>clk(max)</sub>	maximum clock frequency	CP; see Fig. 6	5 V		5	10	-	MHz
			10 V		11	22	-	MHz
			15 V		14	28	-	MHz

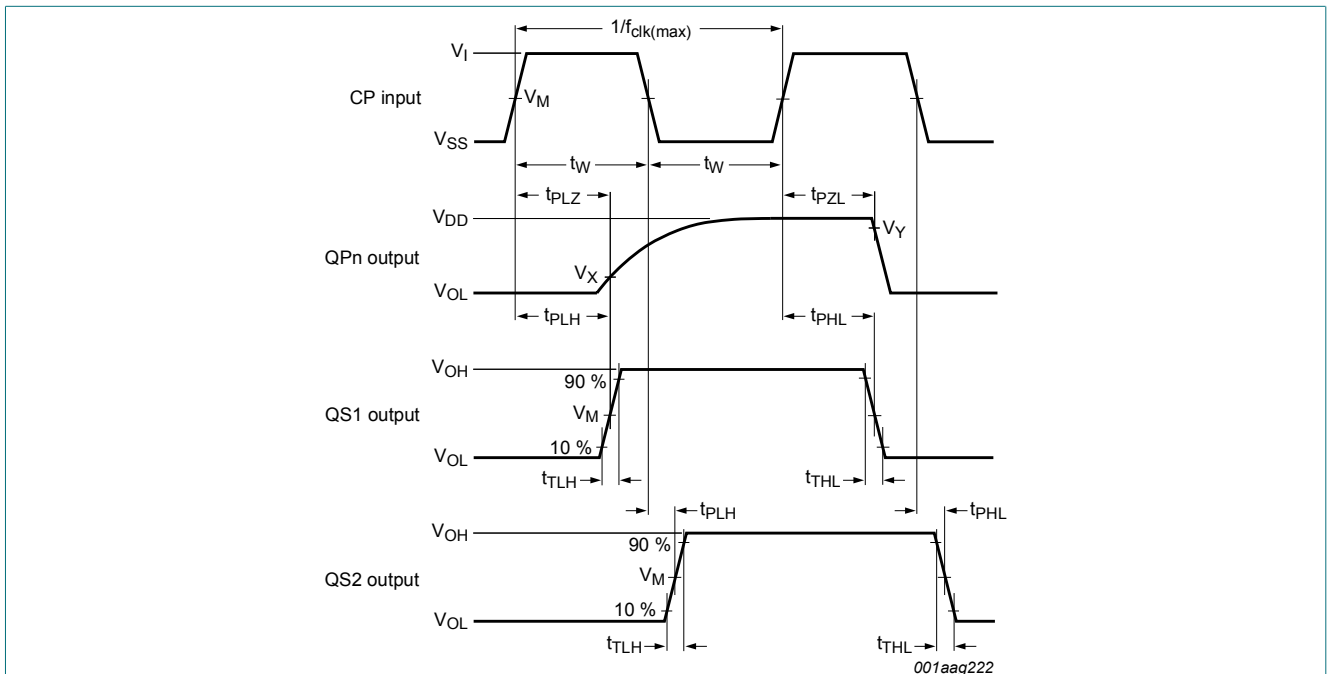
- [1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C<sub>L</sub> in pF).
- [2] t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>dis</sub> is the same as t<sub>PLZ</sub>
- [3] t<sub>t</sub> is the same as t<sub>TLH</sub> and t<sub>THL</sub>

**Table 8. Dynamic power dissipation**

P<sub>D</sub> can be calculated from the formulas shown. V<sub>SS</sub> = 0 V; t<sub>r</sub> = t<sub>f</sub> ≤ 20 ns; T<sub>amb</sub> = 25 °C.

Symbol	Parameter	V <sub>DD</sub>	Typical formula	Where
P <sub>D</sub>	dynamic power dissipation	5 V	$P_D = 1\,200 \times f_i + \sum(f_o \times C_L) \times V_{DD}^2 \mu W$	f <sub>i</sub> = input frequency in MHz; f <sub>o</sub> = output frequency in MHz; C <sub>L</sub> = output load capacitance in pF; Σ(f <sub>o</sub> × C <sub>L</sub> ) = sum of the outputs; V <sub>DD</sub> = supply voltage in V.
		10 V	$P_D = 5\,550 \times f_i + \sum(f_o \times C_L) \times V_{DD}^2 \mu W$	
		15 V	$P_D = 15\,000 \times f_i + \sum(f_o \times C_L) \times V_{DD}^2 \mu W$	

### 10.1. Waveforms and test circuit



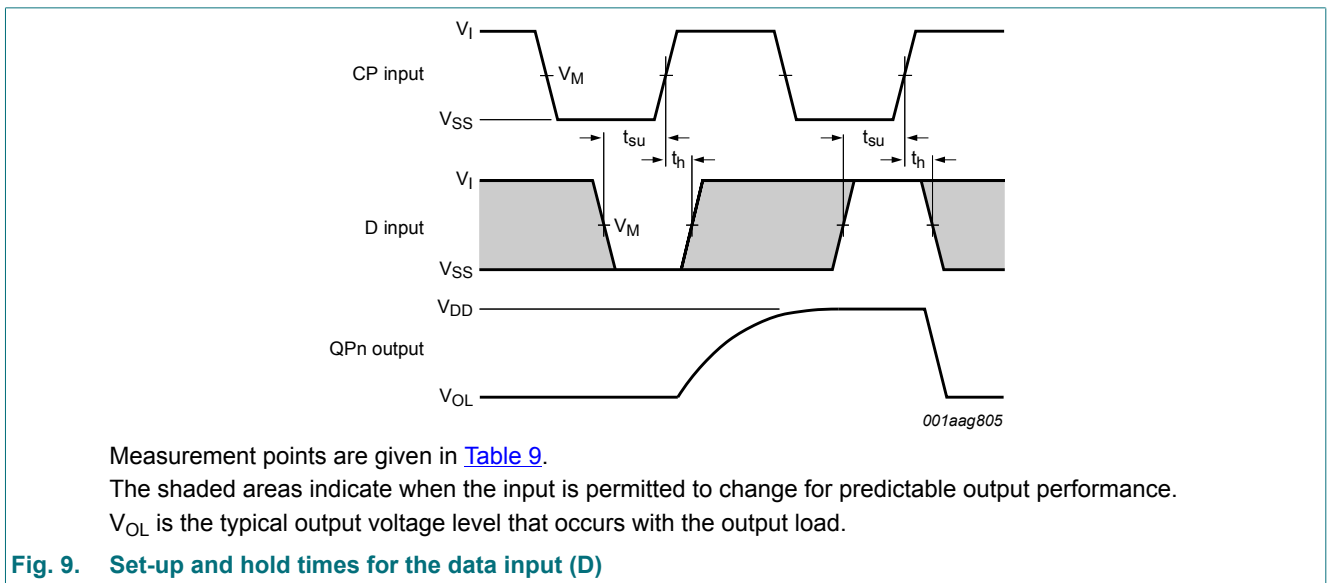
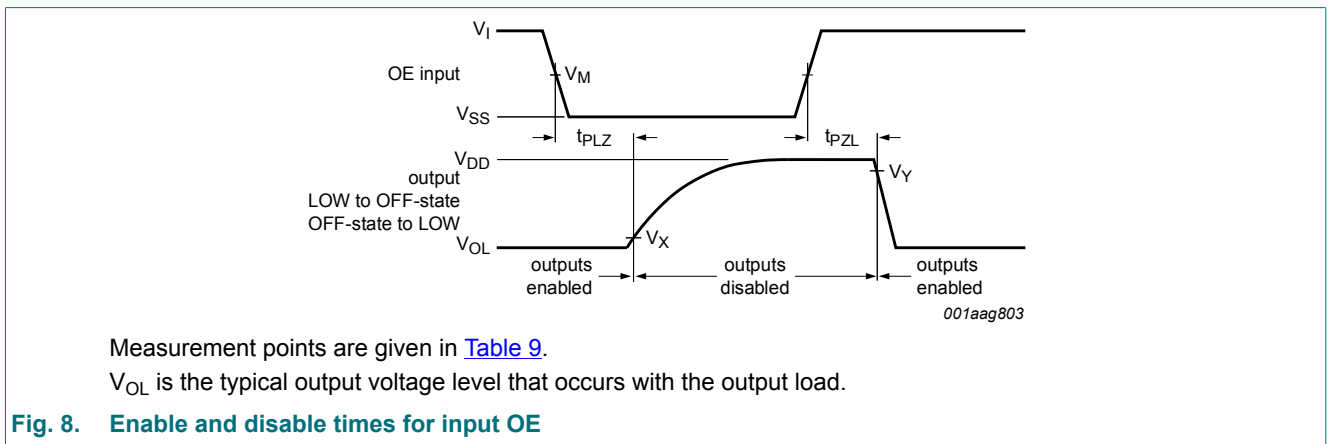
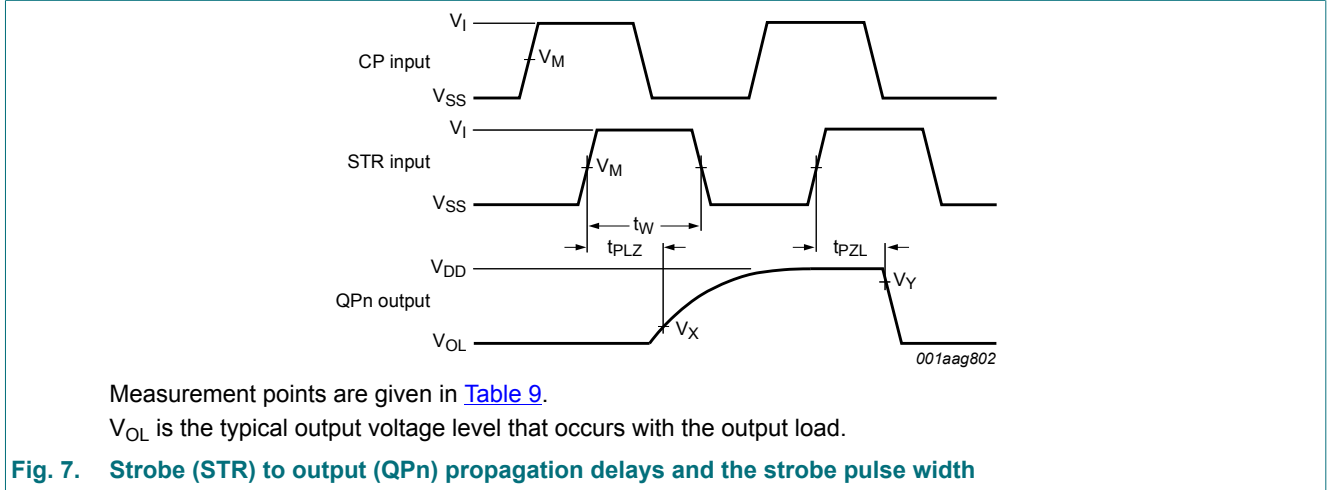
Parallel output measurement points are given in Table 9.  
V<sub>OL</sub> and V<sub>OH</sub> are typical output voltage levels that occur with the output load.

**Fig. 6. Propagation delay clock (CP) to output (QPn, QS1, QS2), clock pulse width and maximum clock frequency**



Table 9. Measurement points

Supply	Input	Output		
$V_{DD}$	$V_M$	$V_M$	$V_X$	$V_Y$
5 V to 15 V	$0.5V_{DD}$	$0.5V_{DD}$	$0.1V_O$	$0.9V_O$



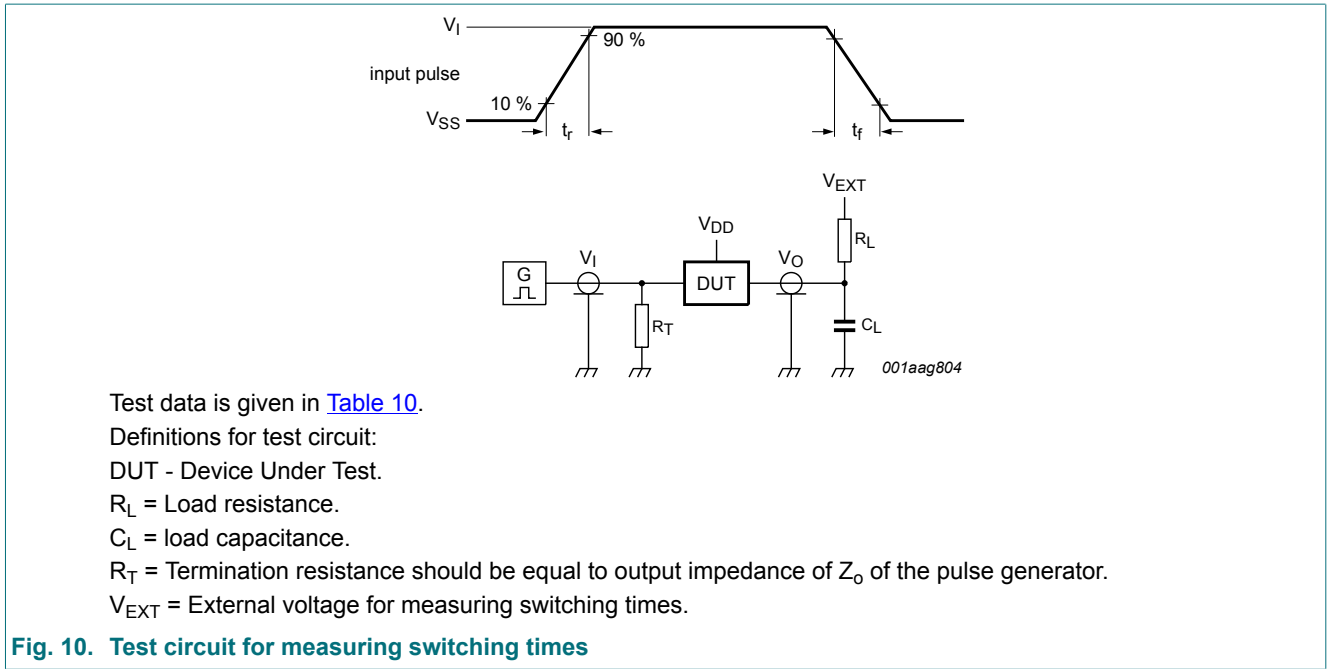
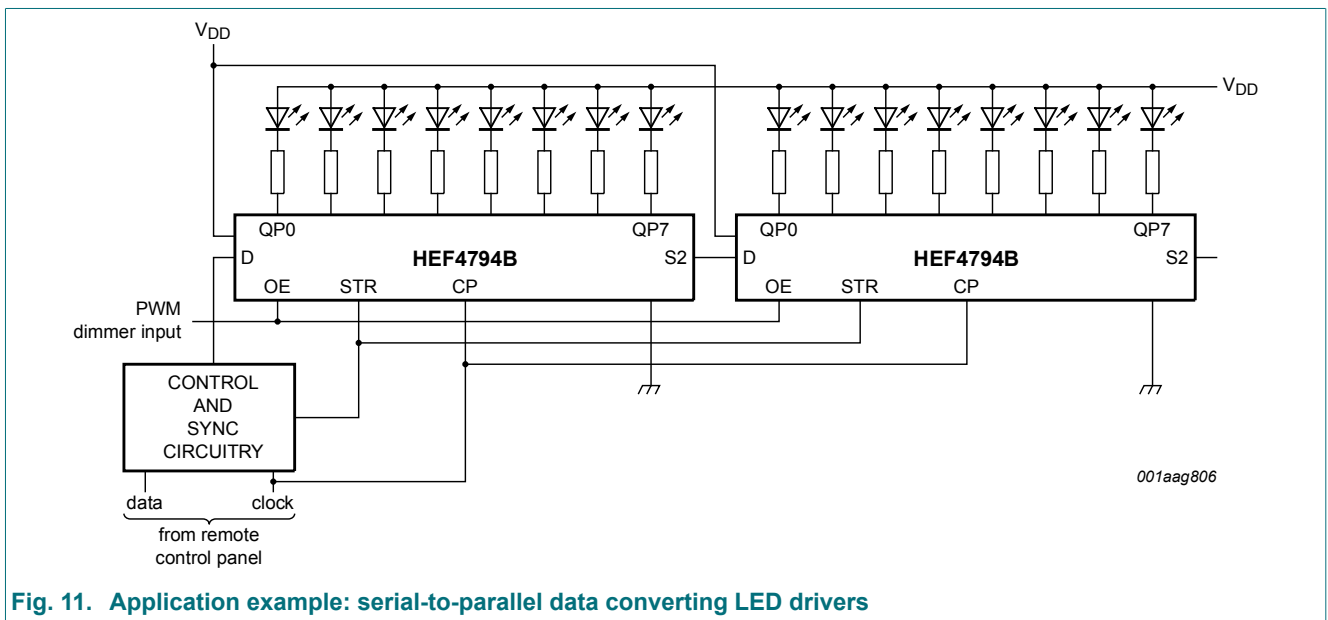


Table 10. Test data

Supply	Input	$V_{EXT}$	Load
$V_{DD}$	$V_I$	$t_{PLZ}, t_{PZL}$	$C_L$
5 V to 15 V	$V_{DD}$	$t_r, t_f$	$R_L$
		$\leq 20$ ns	50 pF
		$V_{DD}$	1 k $\Omega$
		$t_{PLH}, t_{PHL}$	open

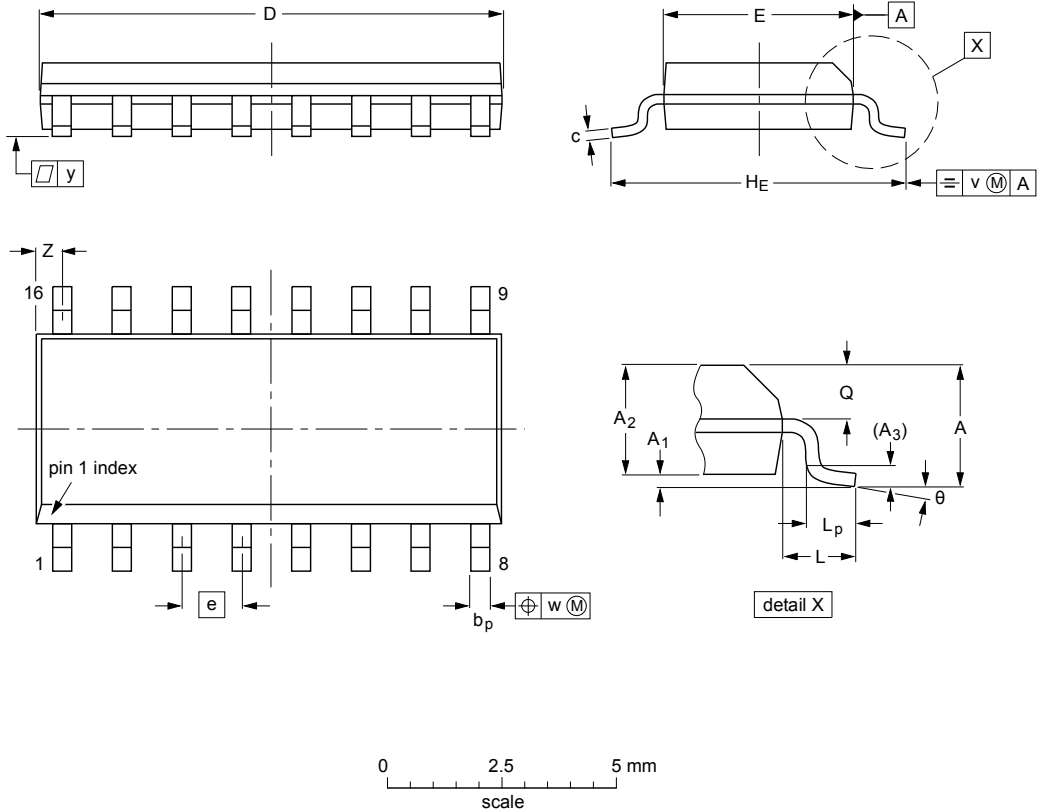
## 11. Application information



12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				99-12-27 03-02-19

Fig. 12. Package outline SOT109-1 (SO16)

## 13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4794B_Q100 v.2	20181107	Product data sheet	-	HEF4794B_Q100 v.1
Modifications:	<ul style="list-style-type: none"><li>• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li><li>• Legal texts have been adapted to the new company name where appropriate.</li><li>• <a href="#">Fig. 5</a> corrected.</li></ul>			
HEF4794B_Q100 v.1	20120807	Product data sheet	-	-

## 14. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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