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Kind regards,

Team Nexperia



IP4221CZ6-S

ESD protection for high-speed interfaces

Rev. 2 — 13 December 2012

Product data sheet

1. Product profile

1.1 General description

The device is designed to protect high-speed interfaces such as USB 2.0, Ethernet and Digital Visual Interface (DVI) against ElectroStatic Discharge (ESD).

The device includes four high-level ESD protection diode structures for high-speed signal lines and is encapsulated in a leadless ultra small DFN1410-6 (SOT886) plastic package.

Special diode configuration protects all signal lines and offers ultra low line capacitance of only 1 pF. The rail-to-rail diodes are connected to the Zener diode which allows ESD protection to be independent of supply voltage.

1.2 Features and benefits

- System ESD protection for high-speed data lines such as USB 2.0, Ethernet and DVI
- All signal lines with integrated rail-to-rail clamping diodes for downstream ESD protection of ± 8 kV according to IEC 61000-4-2, level 4
- Line capacitance of only 1 pF for each channel
- Leadless ultra small DFN1410-6 package: $1 \times 1.45 \times 0.5$ mm; pitch 0.5 mm

1.3 Applications

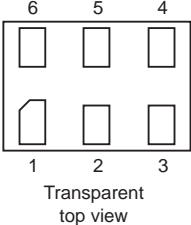
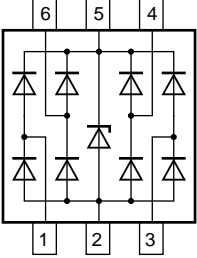
The device is designed for high-speed receiver and transmitter port protection:

- Mobile phones, smartphones and handsets
- TVs and monitors
- DVD recorders and players
- Notebooks, mother boards, graphic cards and ports
- Set-top boxes and game consoles



2. Pinning information

Table 1. Pinning

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	I/O 1	ESD protection	 <p>Transparent top view</p>	
2	GND	ground		
3	I/O 2	ESD protection		
4	I/O 3	ESD protection		
5	V _{CC}	supply voltage		
6	I/O 4	ESD protection		

001aag273

3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
IP4221CZ6-S	DFN1410-6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1.45 × 0.5 mm	SOT886

4. Marking

Table 3. Marking codes

Type number	Marking code
IP4221CZ6-S	1S

5. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _I	input voltage		-0.5	+5.5	V
V _{ESD}	electrostatic discharge voltage	IEC 61000-4-2, level 4; [1] contact discharge	-8	+8	kV
T _{stg}	storage temperature		-55	+125	°C
T _{amb}	ambient temperature		-40	+85	°C

[1] All pins to ground.

6. Characteristics

Table 5. Characteristics

$T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$C_{(I/O-GND)}$	input/output to ground capacitance	$V_I = 0\text{ V}$; $f = 1\text{ MHz}$; $V_{CC} = 3\text{ V}$	[1][2] -	1	1.2	pF
I_{RM}	reverse leakage current	$V_I = 3\text{ V}$	[3][2] -	-	100	nA
V_{BRzd}	Zener diode breakdown voltage	$I_I = 1\text{ mA}$	[4] 6	-	9	V
V_F	forward voltage	$I_{test} = 10\text{ mA}$	-	0.7	-	V

[1] This parameter is guaranteed by design.

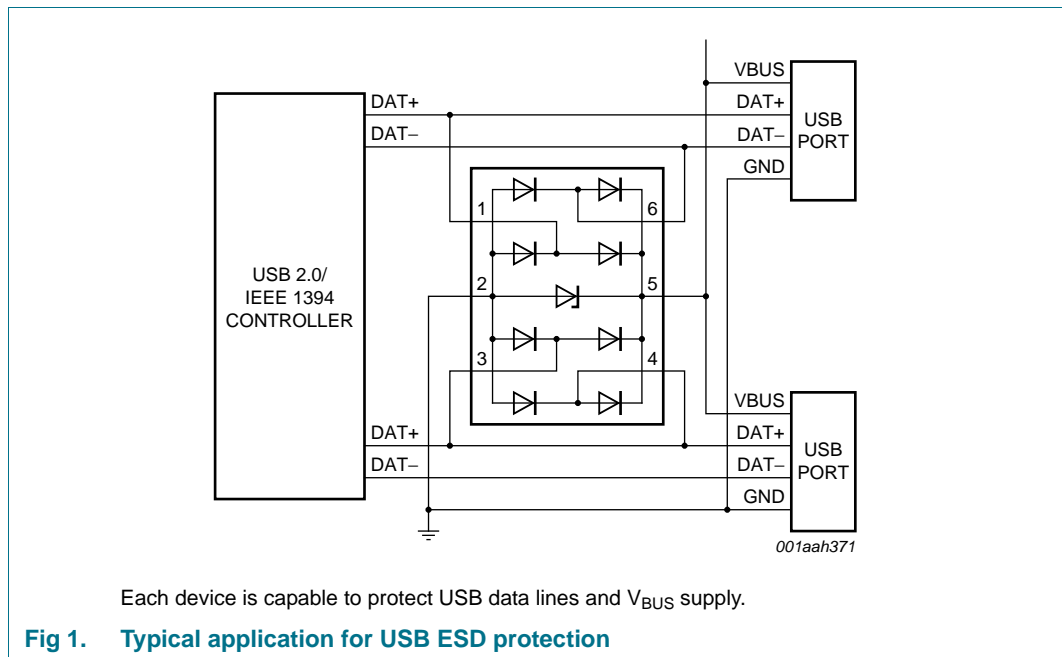
[2] Pins 1, 3, 4 and 6 are measured to ground.

[3] All pins measured to ground (pin 2).

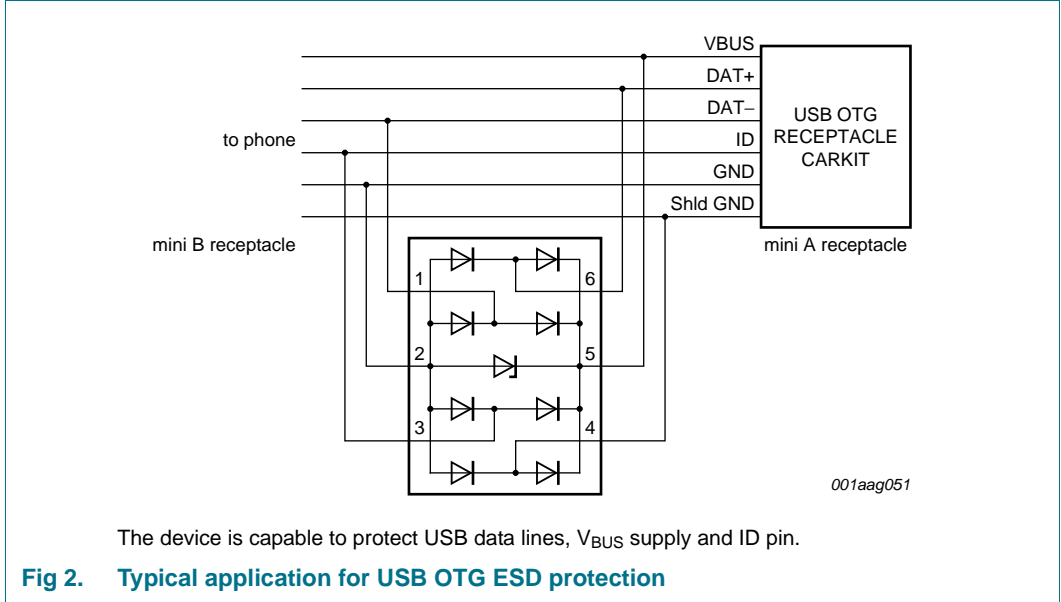
[4] Measured from pin 5 to pin 2.

7. Application information

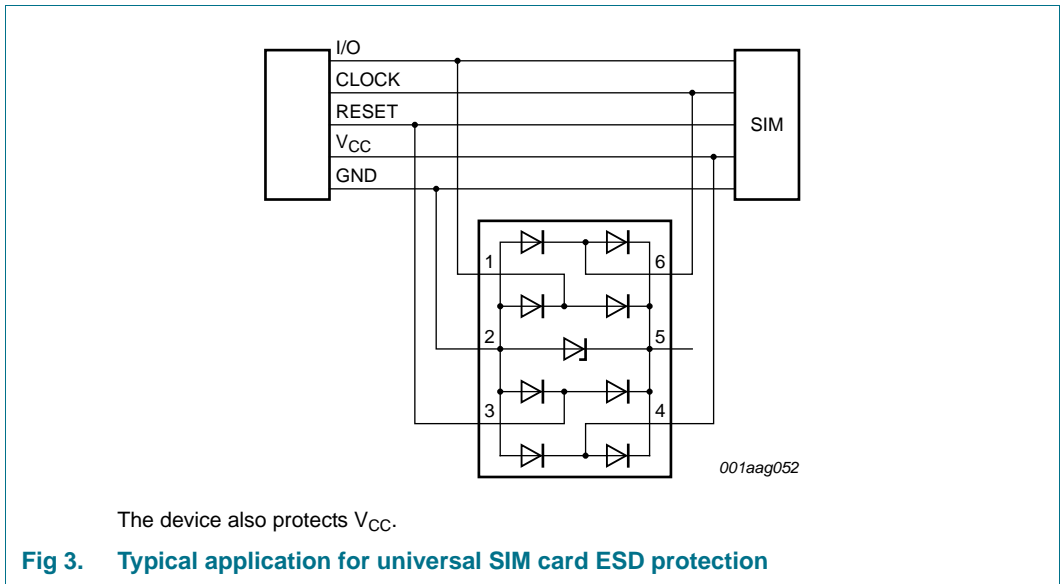
7.1 USB 1.1 and 2.0 protection



7.2 USB On-The-GO (OTG) protection



7.3 Universal SIM card protection



7.4 IEEE 1394a/b protection

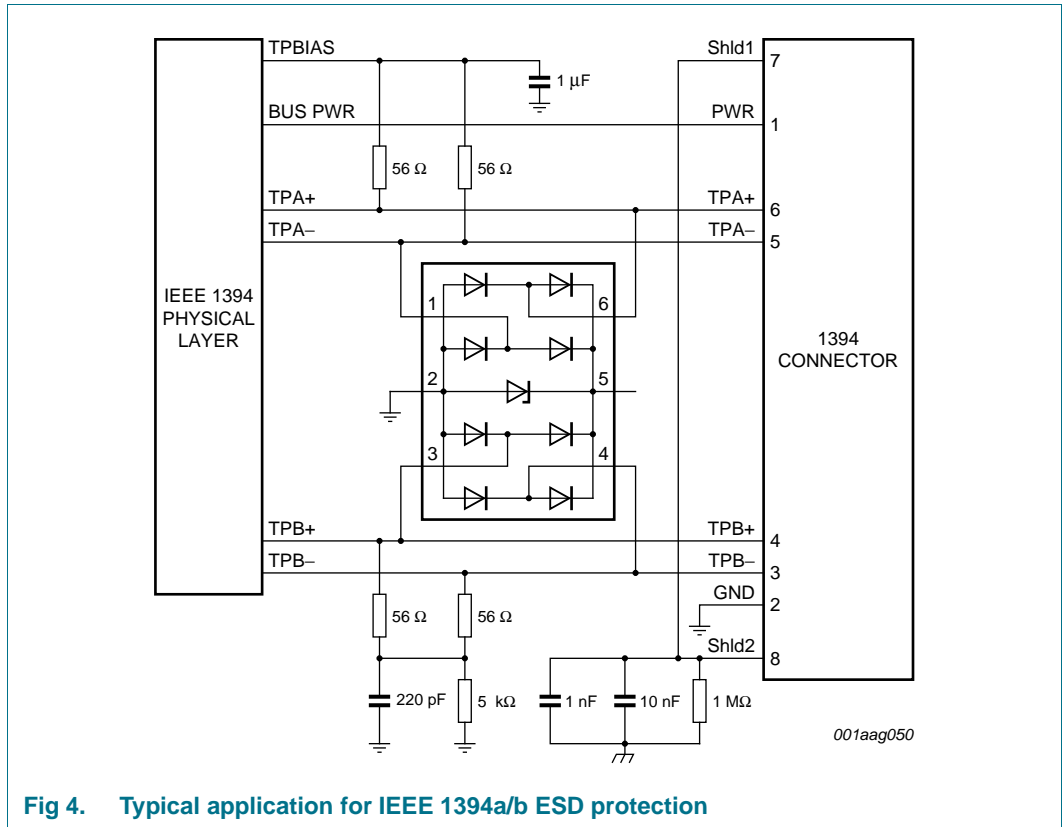


Fig 4. Typical application for IEEE 1394a/b ESD protection

7.5 Gigabit Ethernet transceiver protection

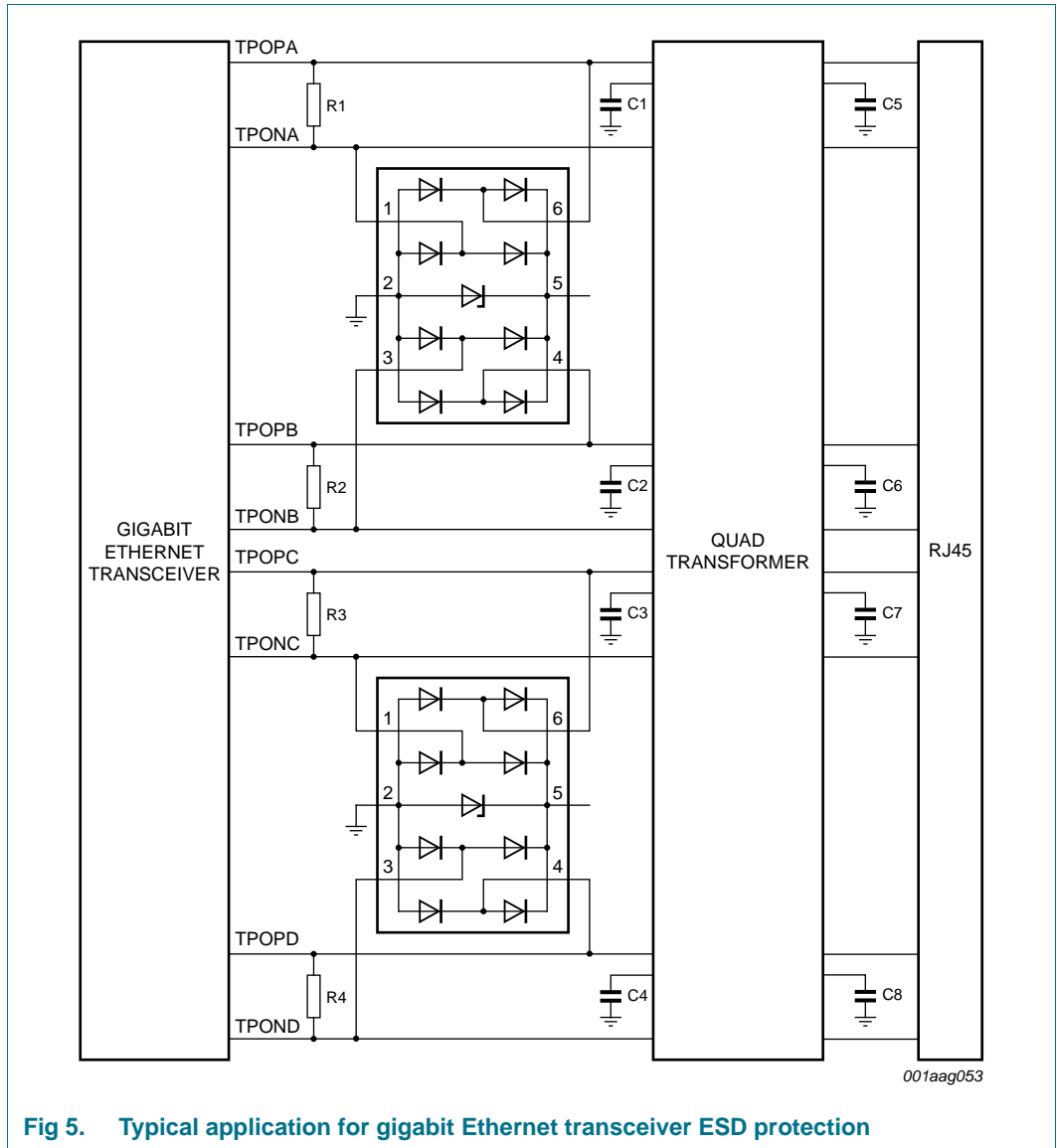


Fig 5. Typical application for gigabit Ethernet transceiver ESD protection

7.6 Universal microSD/TransFlash and SD memory card protection

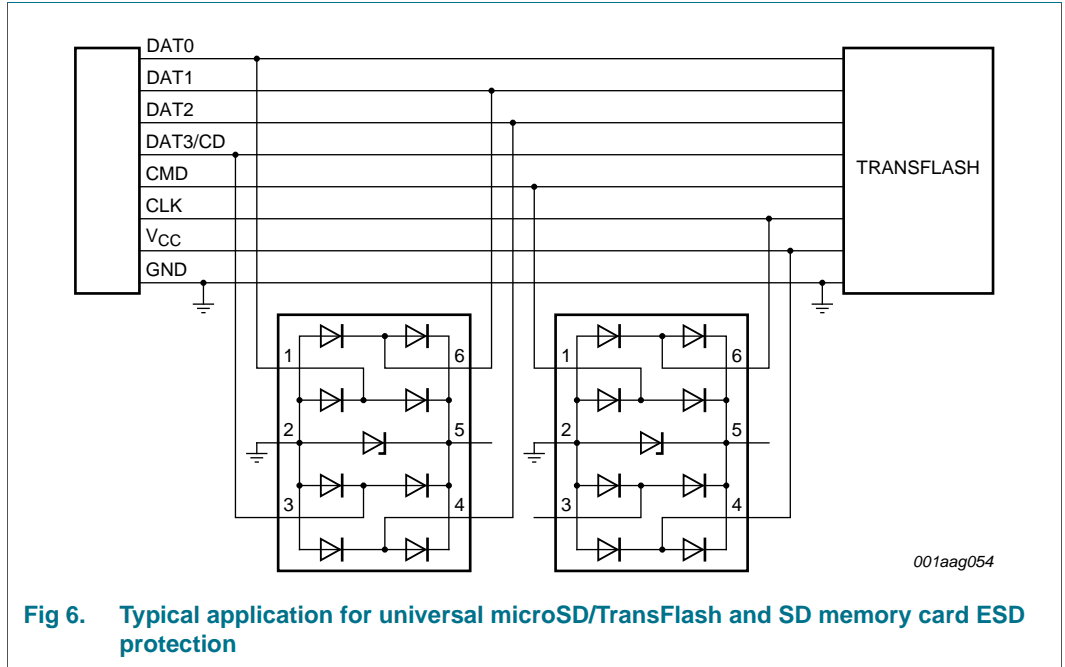


Fig 6. Typical application for universal microSD/TransFlash and SD memory card ESD protection

8. Package outline

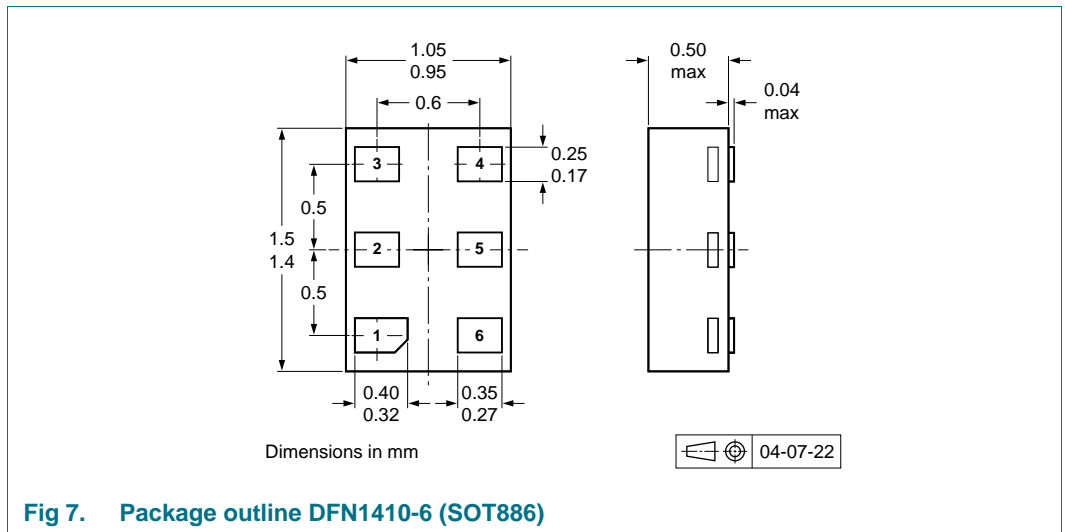


Fig 7. Package outline DFN1410-6 (SOT886)

9. Packing information

Table 6. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code. [1]

Type number	Package	Description	Packing quantity	
				5000
IP4221CZ6-S	DFN1410-6 (SOT886)	4 mm pitch, 8 mm tape and reel; T1	[2]	-115
		4 mm pitch, 8 mm tape and reel; T4	[3]	-132

[1] For further information and the availability of packing methods, see [Section 13](#).

[2] T1: normal taping

[3] T4: reverse taping

10. Soldering

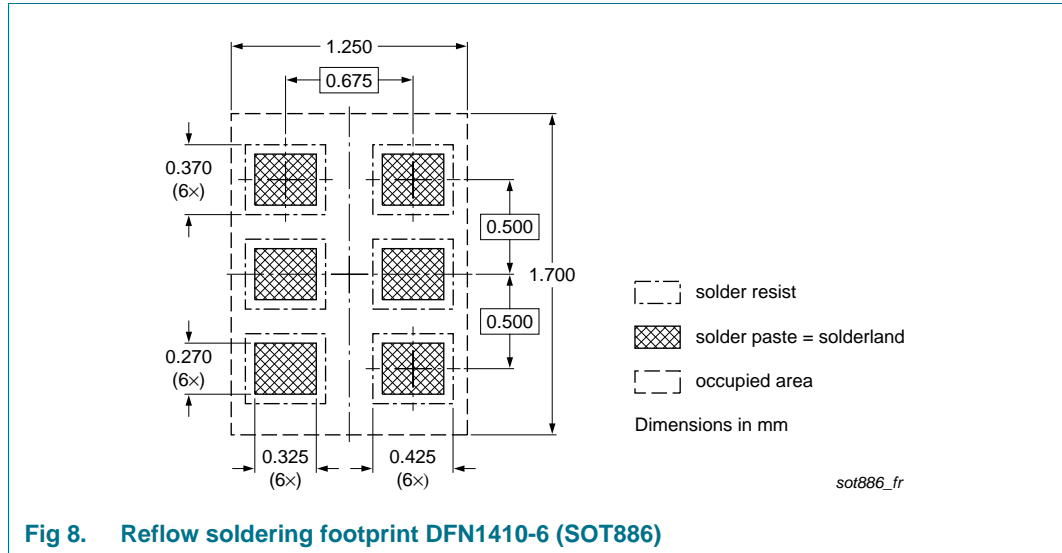


Fig 8. Reflow soldering footprint DFN1410-6 (SOT886)

11. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
IP4221CZ6-S v.2	20121213	Product data sheet	-	IP4221CZ6-S v.1
Modifications:	<ul style="list-style-type: none"> • Section 1 "Product profile": updated • Section 4 "Marking": added • Section 5 "Limiting values": T_{amb} added • Recommended operating conditions: removed • Table 5 "Characteristics": updated • Section 7 "Application information": updated • Section 8 "Package outline": drawing replaced with minimized package outline drawing • Section 10 "Soldering": updated • Section 12 "Legal information": updated 			
IP4221CZ6-S v.1	20080429	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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