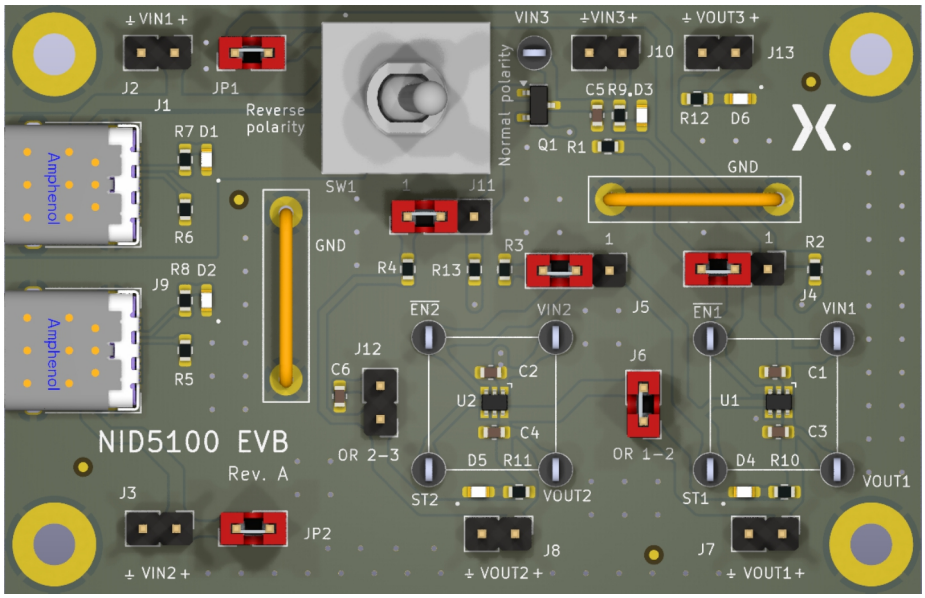
UM90040

Rev. 1 — 25 July 2024

user manual

NID5100, 1.2 V to 5.5 V, 1.5 A input polarity protected, low quiescent current ideal diode evaluation board



Abstract: The NEVB-NID5100 evaluation board is a two-layer PCB equipped with two NID5100 ideal diodes. It allows users to explore the device's behavior under various application conditions.

Keywords: Ideal diode, Schottky replacement, OR-ing diode, reverse polarity protection, evaluation board (EVB)

nexperia

1. Introduction

The NID5100 is a low forward voltage, integrated ideal diode capable of replacing traditional diodes in low voltage systems unable to tolerate the high voltage drops of traditional rectifier components. The device contains a 1.5 A continuous current rated P-channel MOSFET that can operate over an input voltage range of 1.2 V to 5.5 V.

This evaluation Printed Circuit Board (PCB) incorporates two NID5100 ideal diodes and one PMOS transistor to assess performance and behavior across various use cases such as OR-ing, OR-ing with an external PMOS transistor, priority OR-ing, and reverse polarity protection. It offers multiple methods for applying power to the inputs and testing reverse polarity protection using a switch, while also providing access to all device pins.

2. Features

The following features are available on this evaluation board:

- Input operating voltage range (V_{IN}) 1.2 V to 5.5 V
- Continuous output current 1.5 A
- Three supply inputs
- Two additional USB-C supply inputs
- Access to all device pins
- Use case selection by means of jumpers

3. Schematic

Fig. 1 shows the schematic of the NEVB-NID5100 evaluation board. Explanation of the test pins, jumpers and other features can be found in the next sections.

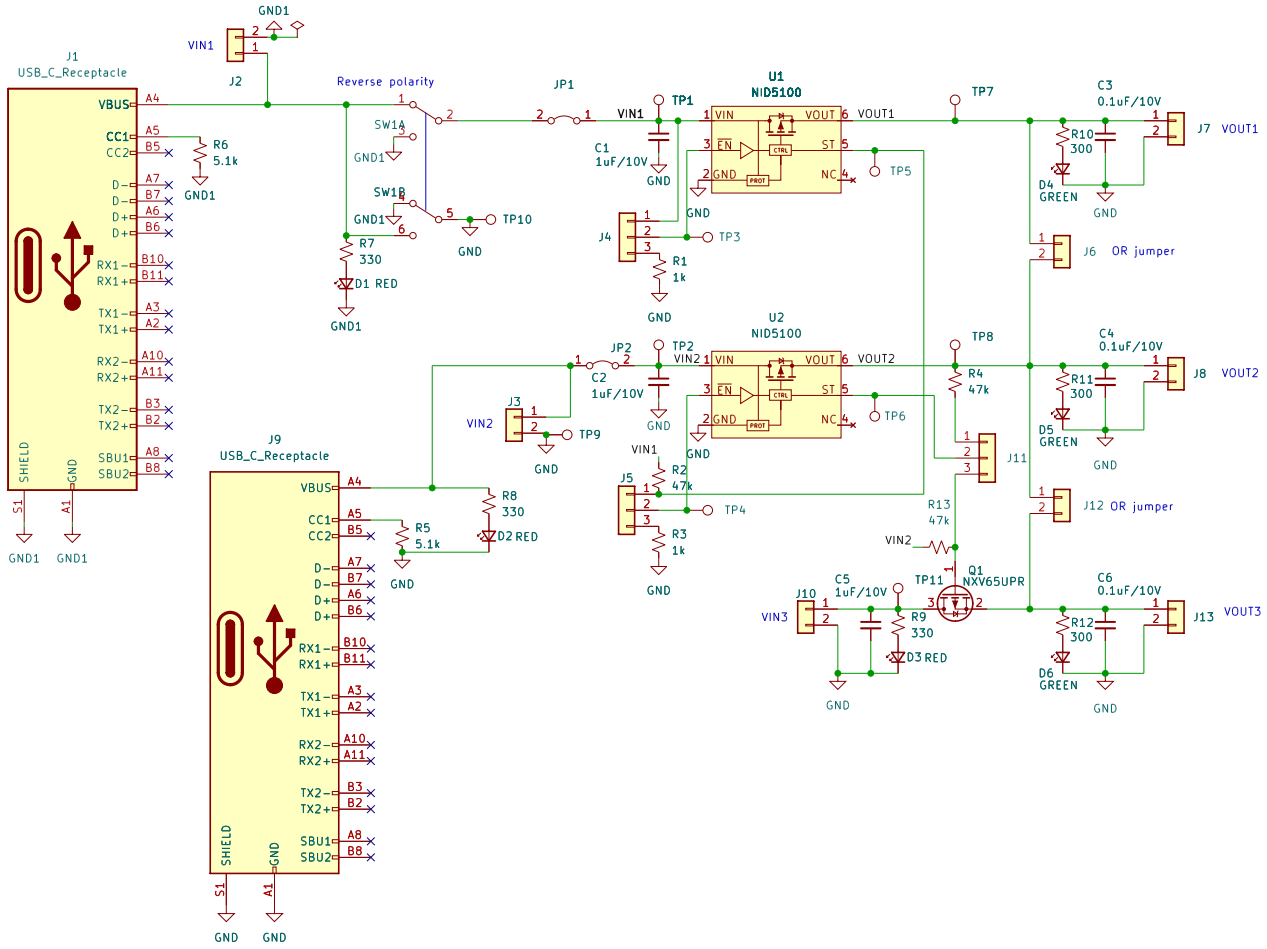


Fig. 1. NEVB-NID5100 EVB schematic

4. PCB layout

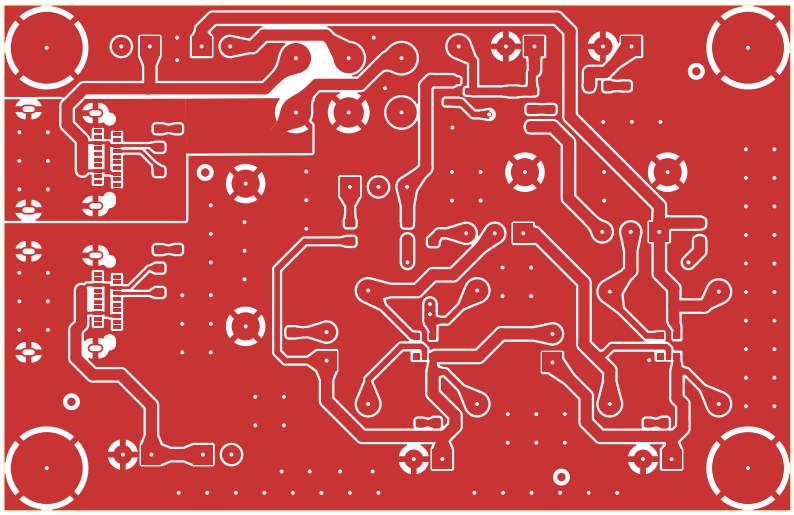


Fig. 2. Top copper layer

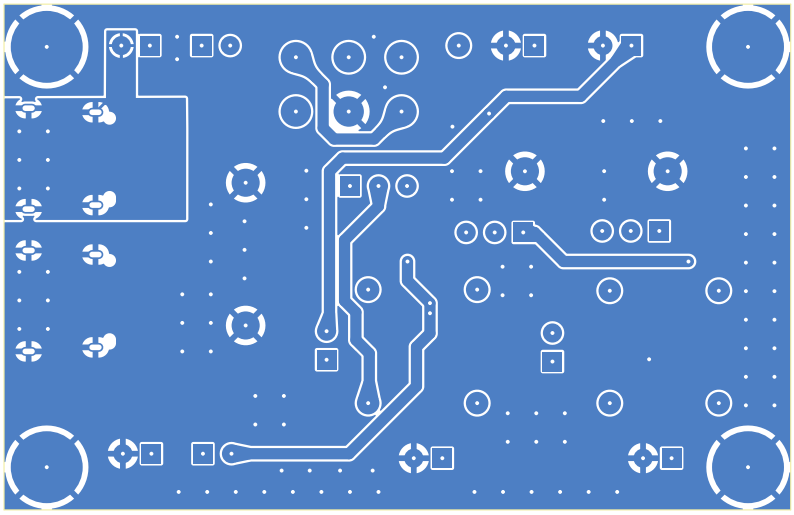


Fig. 3. Bottom copper layer

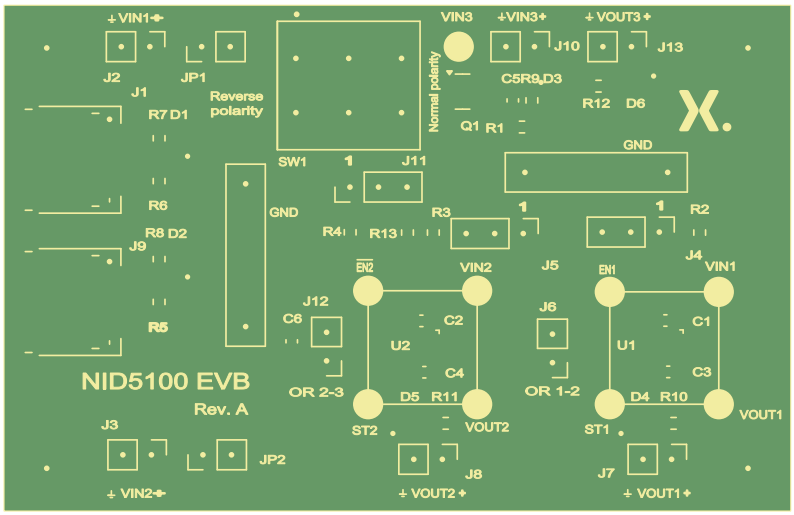


Fig. 4. Silkscreen top

5. Bill of material

Table 1. Bill of Material (BOM)

Reference	Quantity	Value	Manufacturer name	Manufacturer part number
C1, C2, C5	3	1 µF/10 V	KEMET	C0603C105K8RACTU
C3, C4, C6	3	0.1 µF/10 V	KEMET	C0603C104K8RAC
D1, D2, D3	3	RED	Kingbright	APHD1608LSURCK
D4, D5, D6	3	GREEN	Kingbright	APTD1608LCGCK
J1, J9	2	USB_C_Receptacle	Amphenol Commercial Products	12401610E4#2A
J2, J3, J6, J7, J8, J10, J12, J13	8	Conn_01x02	Wurth Elektronik	61300211121
J4, J5, J11	3	Conn_01x03	Wurth Elektronik	61300311121
JP1, JP2	2	Jumper_2_Bridged	Wurth Elektronik	61300211121
Q1	1	NXV65UPR	Nexperia	NXV65UPR
R1, R3	2	1 kΩ	Yageo	AC0603FR-104K7L
R2, R4, R13	3	47 kΩ	Yageo	RC0603FR-0747KL
R5, R6	2	5.1 kΩ	Bourns	CR0603-FX-5101ELF
R7, R8, R9	3	330 Ω	Bourns	CR0603-JW-331ELF
R10, R11, R12	3	300 Ω	Bourns	CR0603-JW-301ELF
SW1	1	SW_DPDT_x2	E-Switch	100DP1T1B1M2QEH
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP11	9	TestPoint	Keystone Electronics	5000
TP9, TP10	2	TestPoint	Keystone Electronics	1430-5
U1, U2	2	NID5100GW	Nexperia	NID5100
-	6	Open Top Jumper Socket RED	Harwin	M7581-46

6. Quick start

The PCB is by default configured in the dual OR-ing application. When connecting the two USB-C ports to a supply (for instance two different USB ports on a pc), the input with the highest voltage will be available on connectors V_{OUT1} (J7) and V_{OUT2} (J8). One can disconnect either one of the supplies and observe that still an output voltage will be available.

7. Test setup and operation

There are multiple supply inputs available. Two USB-C ports (J1 and J9) and three headers (J2, J3 and J10). A red LED indicates the presence of an input voltage. Headers J2 and J3 are in parallel with USB-C port J1 and J9 respectively and can be used to connect a battery pack or lab supply.

Output voltages are available at J7, J8 and J13. If present a green LED will light up.

Jumpers JP1 and JP2 can be used to disconnect the NID5100 from the supply or measure the supply current.

Switch SW1 can be used to validate the reverse polarity protection. It reverses the polarity of USB-C port J1 and header J2.

Jumpers J4-J6, J11 and J12 are used to set the use case which are explained in the next section.

Table 2. Jumper settings

X=don't care

Use case	SW1	JP1	JP2	J4	J5	J6	J11	J12
Reverse Polarity	2-3 5-6	closed	X	2-3	X	open	X	open
Reverse Current Blocking	1-2 4-5	X	X	X	X	open	X	open
Dual OR	1-2 4-5	closed	closed	2-3	2-3	closed	1-2	open
Priority OR	1-2 4-5	closed	closed	2-3 drive 2-3	1-2	closed	1-2	open
Dual OR with PMOS	X	X	closed	X	2-3	open	2-3	closed

Reverse polarity protection

By toggling switch SW1 one can reverse the supply polarity of J2 (V_{IN1}) and USB-C input J1. Device U1 should be enabled by connecting a jumper between J4 pin 2-3. Output V_{OUT1} is fully protected and will stay off. The board setup is depicted in Fig. 5, results can be found in Fig. 6.

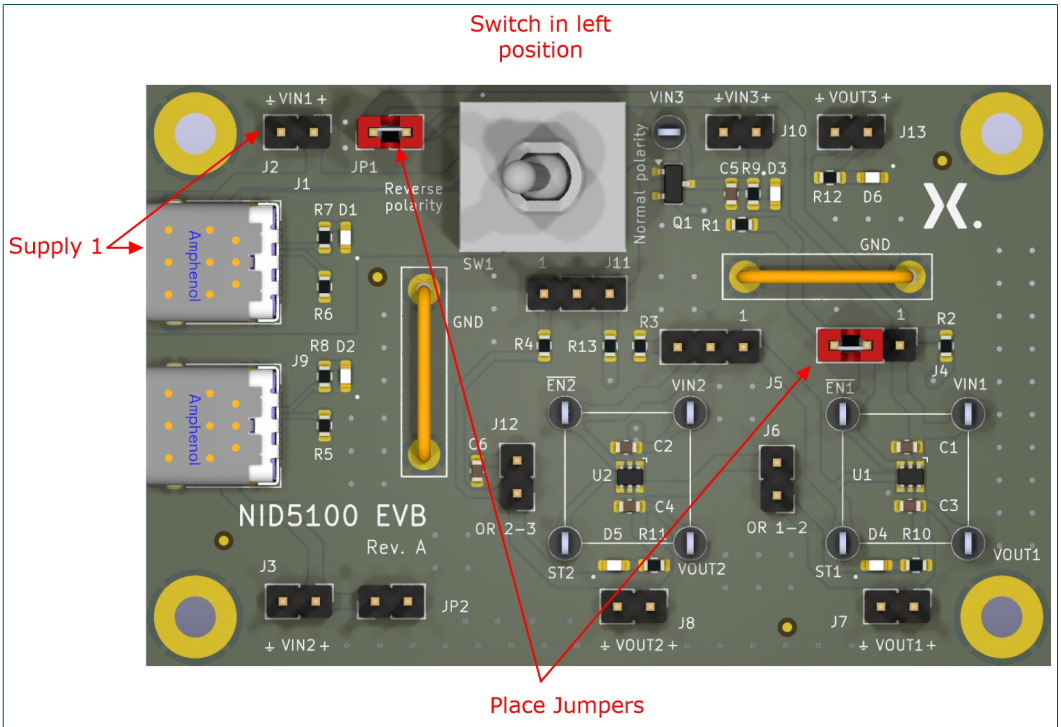


Fig. 5. Board setup for reverse polarity protection

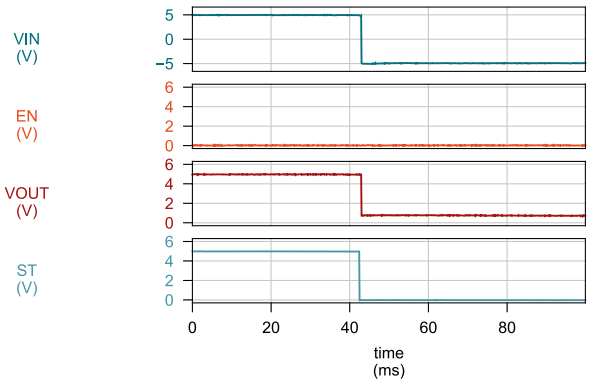


Fig. 6. Oscilloscope traces showing reverse polarity protection of V_{IN1}

Reverse current blocking

Reverse current blocking is always active independent of the enable state of the device. By lifting V_{OUT1} or V_{OUT2} typically 30.5 mV above V_{IN} the behavior can be validated.

Dual OR-ing

The evaluation PCB can be configured to OR between V_{IN1} and V_{IN2}. Switch SW1 should be in the right position. Both U1 and U2 need to be enabled and in parallel. Enabling both devices is done by placing jumpers on J4 and J5 between pin 2-3. Putting the devices in parallel is done by placing a jumper on J6. Monitoring the device state can be done by connecting the status pin of device U2 to V_{OUT2} by placing a jumper between J11 pin 1–2. The status pin of U1 is always connected via R2. The board setup and jumper placement are shown in Fig. 7.

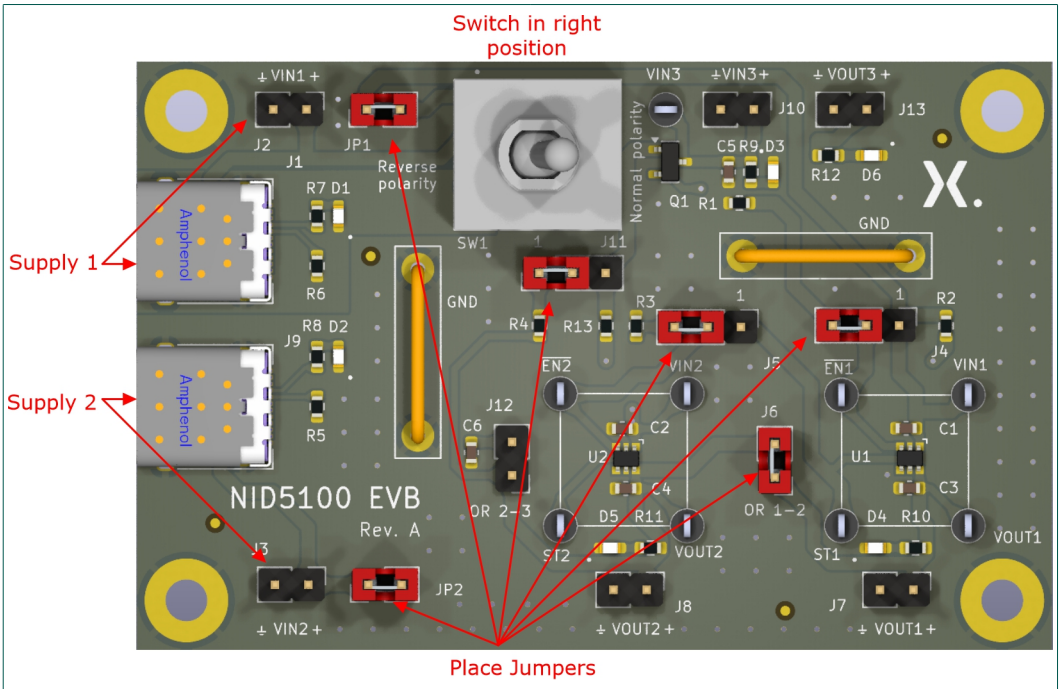


Fig. 7. Board setup for OR-ing between supply 1 and supply 2

Fig. 8 shows the results when OR-ing two supplies. V_{IN1} has been connected to a 5 V source while V_{IN2} has been connected to a 3.3 V source. Initially V_{IN1} is supplying V_{OUT}. When V_{IN1} drops below V_{IN2}, V_{IN2} takes over. The status pins are active low when the device is disabled, hence one can see which device is enabled. If V_{IN1} rises again above V_{IN2}, the initial situation is restored.

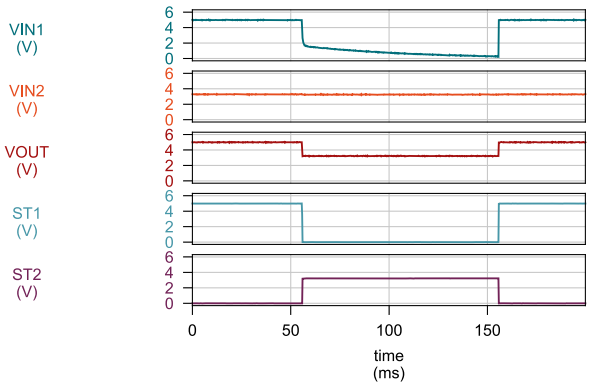


Fig. 8. Oscilloscope traces showing OR-ing between supply 1 and supply 2

Priority OR-ing

Priority OR-ing can be used when on-system level power management tasks are required. This use case makes it possible to have a microcontroller selecting between multiple equal power sources.

The enable signal of U1 is driven from the microcontroller via J4 pin 2-3. Resistor R1 enables U1 in case the microcontroller GPIO pin is low or high-impedance Z.

The enable pin of U2 is connected to the ST pin of U1 via J5 pin 1-2. Resistor R2 inverts the ST signal of U1. If U1 is enabled (ST1 = HIGH), U2 is disabled and vice versa. The board setup is shown in Fig. 9.

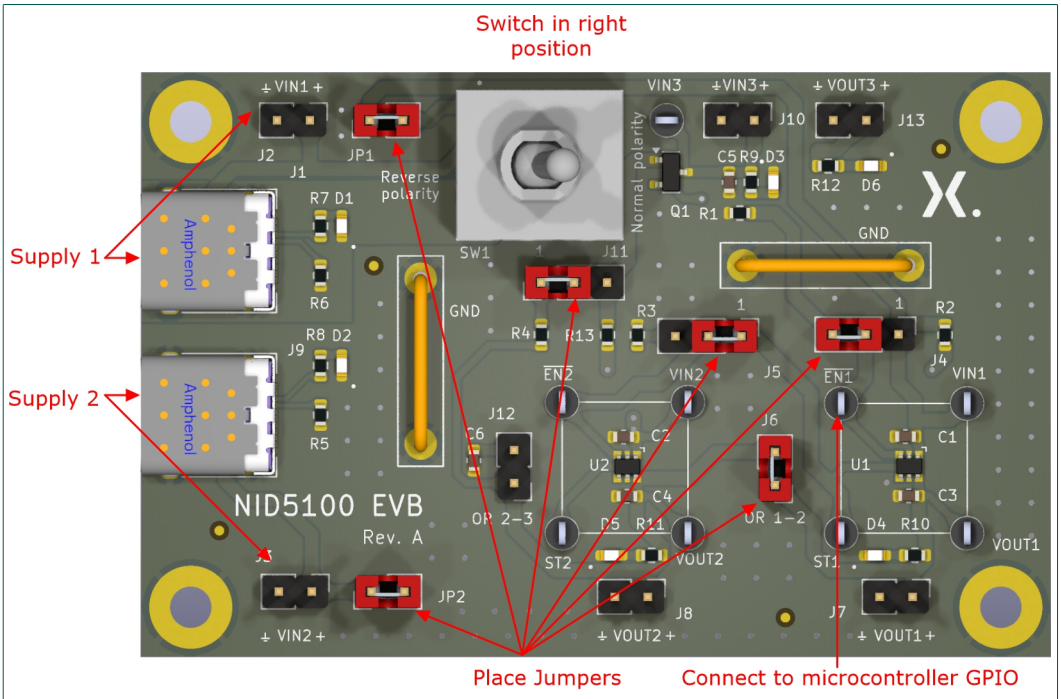


Fig. 9. Board setup for priority OR-ing between supply 1 and supply 2

Fig. 10 shows the oscilloscope traces for this use case. Since Both V_{IN1} and V_{IN2} are 5 V it is not possible to distinguish by means of V_{OUT} which supply is active. Therefore, this application was loaded with resistor of 47 Ω. By means of the PRIO signal one can defer the load current to either U1 or U2.

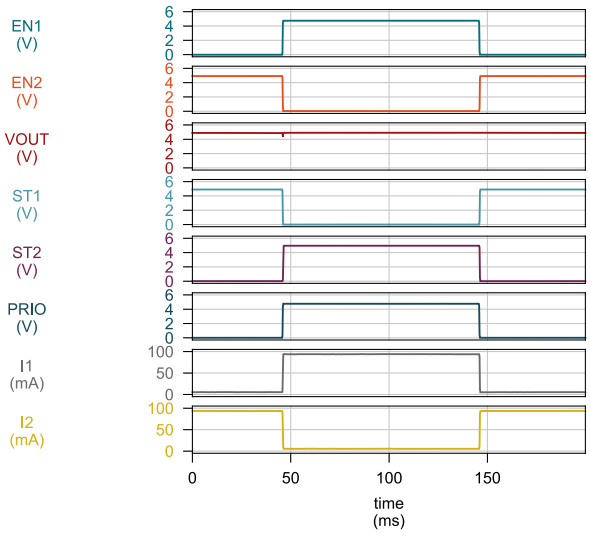


Fig. 10. Oscilloscope traces showing priority OR-ing between supply 1 and supply 2

OR-ing with external MOSFET

The evaluation board is equipped with a PMOS transistor providing the OR-ing function between V_{IN2} and V_{IN3}. A jumper between pin 2-3 of J11 needs to be placed, as well as a jumper on J12. Device U2 needs to be enabled by connecting a jumper to J5 pin 2-3. If U2 is enabled, the ST output will be high-impedance Z, the pass FET will not conduct until V_{IN3} exceeds V_{IN2}.

When V_{IN3} is higher than V_{IN2} + $V_{THmosfet}$, the MOSFET starts conducting. The reverse current block of U2 will become active and ST will be driven low, ensuring full conductivity of the PMOST. The board setup can be found in Fig. 11.

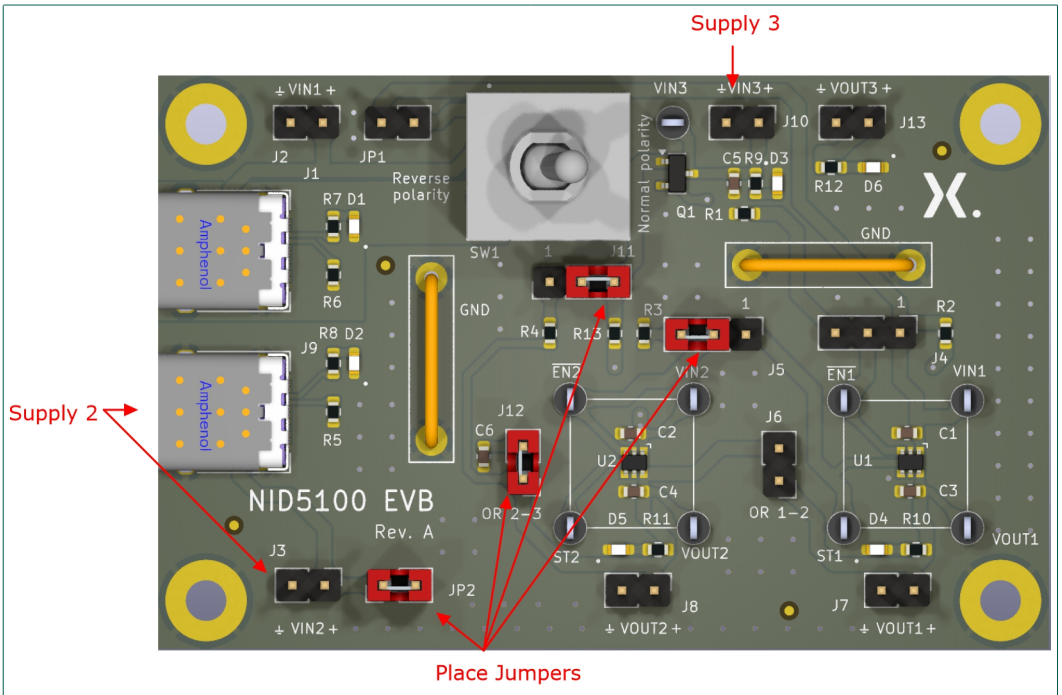


Fig. 11. Board setup for OR-ing between supply 2 and supply 3 using a PMOST

Fig. 12 shows the results when OR-ing between 3.3 V and 5 V. V_{IN3} does not return to 0 V since there is no discharge resistance connected to the gate of Q1.

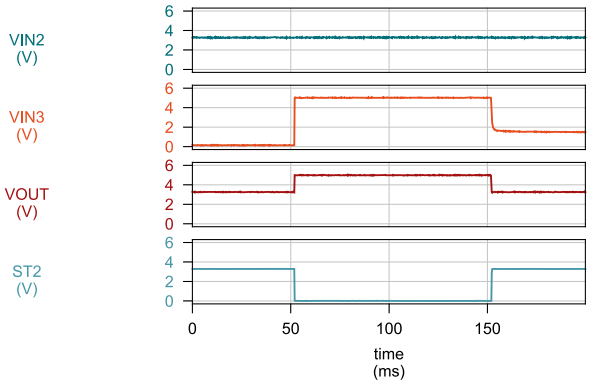


Fig. 12. Oscilloscope traces showing OR-ing between supply 2 and supply 3 using a PMOS transistor

Jumper, test points and supply connections

Table 3 explains the usage of all jumpers present on the evaluation PCB.

Table 4 shows available test points, supply in- and output connections.

Table 3. Jumper usage

Jumper	Default position	Usage
JP1	closed	• Disconnect V_{IN1} • Measure V_{IN1} supply current
JP2	closed	• Disconnect V_{IN2} • Measure V_{IN2} supply current
J4	2-3	• 1-2 disable U1 • 2-3 enable U1
J5	2-3	• 1-2 priority OR with U1 • 2-3 enable U2
J6	closed	OR V_{OUT1} - V_{OUT2}
J11	1-2	• 1-2 Connect U2 ST to V_{OUT2} • 2-3 Enable Q1 by ST of U2
J12	open	OR V_{OUT2} - V_{OUT3}

Table 4. Test points, supply-in and output connections

Test point	Connected to
J1	USB-C supply 1 (V_{IN1})
J2	External supply 1 (V_{IN1})
J3	External supply 2 (V_{IN2})
J7	Output 1 (V_{OUT1})
J8	Output 2 (V_{OUT2})
J9	USB-C supply 2 (V_{IN2})
J10	External supply 3 (V_{IN3})
J13	Output 3 (V_{OUT3})
TP1	V_{IN} U1
TP2	V_{IN} U2
TP3	Enable U1
TP4	Enable U2
TP5	Status indication U1
TP6	Status indication U2
TP7	V_{OUT} U1
TP8	V_{OUT} U2
TP11	V_{IN3}

8. Revision history

Table 5. Revision history

Revision number	Date	Description
UM90040 v.1	20240725	Initial version

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