NXB0101

Dual supply translating transceiver; auto direction sensing; 3-state

Rev. 3 — 23 August 2021 Product data sheet

1. General description

The NXB0101 is a 1-bit, dual supply translating transceiver with auto direction sensing, that enables bidirectional voltage level translation. It features two 1-bit input-output ports (A and B), one output enable input (OE) and two supply pins ($V_{CC(A)}$ and $V_{CC(B)}$). $V_{CC(A)}$ can be supplied at any voltage between 1.2 V and 3.6 V and $V_{CC(B)}$ can be supplied at any voltage between 1.65 V and 5.5 V, making the device suitable for translating between any of the low voltage nodes (1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V and 5.0 V). Pin A and OE are referenced to $V_{CC(A)}$ and pins B is referenced to $V_{CC(B)}$. A LOW level at pin OE causes the outputs to assume a high-impedance OFF-state. This device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

2. Features and benefits

- Wide supply voltage range:
  - $V_{CC(A)}$: 1.2 V to 3.6 V and $V_{CC(B)}$: 1.65 V to 5.5 V
- I_{OFF} circuitry provides partial Power-down mode operation
- Inputs accept voltages up to 5.5 V
- ESD protection:
  - HBM: ANSI/ESDA/Jedec JS-001 Class 2 exceeds 2.5 kV for A port
  - HBM: ANSI/ESDA/Jedec JS-001 Class 3B exceeds 15 kV for B port
  - CDM: ANSI/ESDA/Jedec JS-002 Class C3 exceeds 1.5 kV
- Latch-up performance exceeds 100 mA per JESD 78B Class II
- Multiple package options
- Specified from −40 °C to +85 °C and −40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
NXB0101GW	-40 °C to +125 °C	SC-88	plastic surface-mounted package; 6 leads	SOT363
NXB0101GM	-40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1.45 × 0.5 mm	SOT886
NXB0101GS	-40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 1.0 × 1.0 × 0.35 mm	SOT1202

4. Marking

Table 2. Marking

Type number	Marking code[1]
NXB0101GW	n1
NXB0101GM	n1
NXB0101GS	n1

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

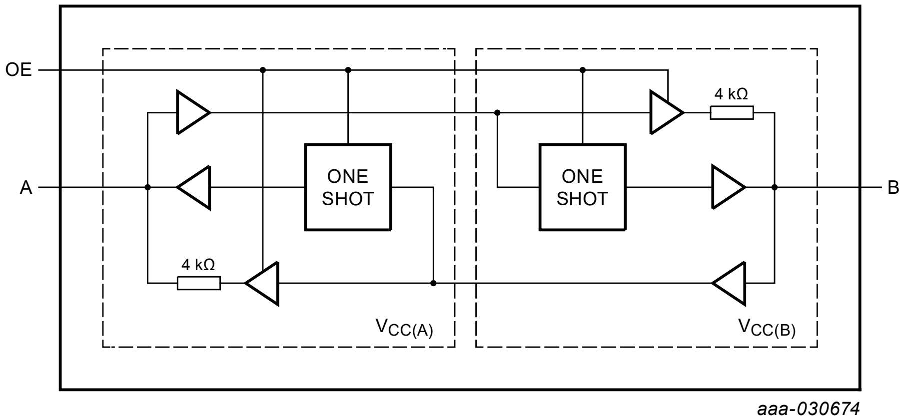


Fig. 1. Functional diagram

6. Pinning information

6.1. Pinning

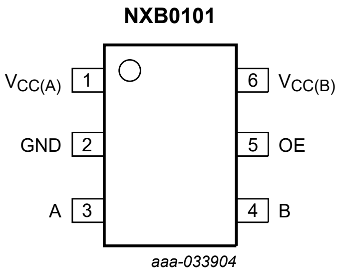


Fig. 2. Pin configuration SOT363 (SC-88)

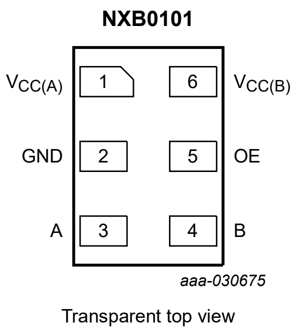


Fig. 3. Pin configuration SOT886 (XSON6)

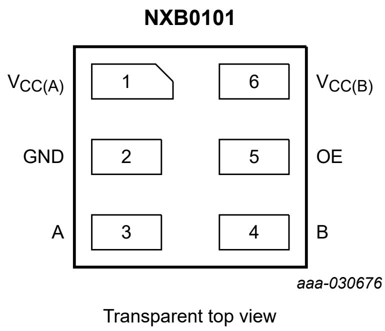


Fig. 4. Pin configuration SOT1202 (XSON6)

6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
$V_{CC(A)}$	1	supply voltage A
GND	2	ground (0 V)
A	3	data input or output (referenced to $V_{CC(A)}$)
B	4	data input or output (referenced to $V_{CC(B)}$)
OE	5	output enable input (active HIGH; referenced to $V_{CC(A)}$)
$V_{CC(B)}$	6	supply voltage B

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Supply voltage		Input	Input/output	
$V_{CC(A)}$ [1]	$V_{CC(B)}$	OE	A	B
1.2 V to 3.6 V	1.65 V to 5.5 V	L	Z	Z
1.2 V to 3.6 V	1.65 V to 5.5 V	H	input or output	output or input
GND	1.65 V to 5.5 V	X	Z	Z
1.2 V to 3.6 V	GND	X	Z	Z

[1] $V_{CC(A)}$ must be less than or equal to $V_{CC(B)}$.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{CC(A)}$	supply voltage A			-0.5	+6.5	V
$V_{CC(B)}$	supply voltage B			-0.5	+6.5	V
V_I	input voltage	OE	[1]	-0.5	+6.5	V
		Power-down or 3-state mode				
		An, Bn	[1]	-0.5	+6.5	V
		Active mode				
		An, Bn	[1] [2] [3]	-0.5	V_{CCI} + 0.5	V
V_O	output voltage	Power-down or 3-state mode				
		A, B	[1]	-0.5	+6.5	V
		Active mode				
		A, B	[1] [3] [4]	-0.5	V_{CCO} + 0.5	V
I_{IK}	input clamping current	V_I < 0 V		-50	-	mA
I_{OK}	output clamping current	V_O < 0 V		-50	-	mA
I_O	output current	V_O = 0 V to V_{CCO}	[4]	-	±50	mA
I_{CC}	supply current	$I_{CC(A)}$ or $I_{CC(B)}$		-	100	mA
I_{GND}	ground current			-100	-	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C	[5]	-	250	mW

[1] The minimum input and minimum output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] V_{CCI} is the supply voltage associated with the input.
[3] V_{CCI} + 0.5 V or $V_{CCO)}$ + 0.5 V should not exceed 6.5 V.
[4] V_{CCO} is the supply voltage associated with the output.
[5] For SOT886 (XSON6) package: P_{tot} derates linearly with 3.3 mW/K above 74 °C.
For SOT1202 (XSON6) package: P_{tot} derates linearly with 3.3 mW/K above 74 °C.
For SOT363 (SC-88) package: P_{tot} derates linearly with 3.7 mW/K above 83 °C.

9. Recommended operating conditions

Table 6. Recommended operating conditions [1] [2]

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		1.2	3.6	V
$V_{CC(B)}$	supply voltage B		1.65	5.5	V
V_I	input voltage	OE	0	5.5	V
		Power-down or 3-state mode			
		A	0	3.6	V
		B	0	5.5	V
		Active mode			
		A, B [3]	0	V_{CCI}	V
V_O	output voltage	Power-down or 3-state mode			
		A	0	3.6	V
		B	0	5.5	V
		Active mode			
		A, B [4]	0	V_{CCO}	V
T_{amb}	ambient temperature		-40	+125	°C
Δt/ΔV	input transition rise and fall rate	$V_{CC(A)}$ = 1.2 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	-	40	ns/V

[1] The A and B sides of an unused I/O pair must be held in the same state, both at V_{CCI} or both at GND.
[2] $V_{CC(A)}$ must be less than or equal to $V_{CC(B)}$.
[3] V_{CCI} is the supply voltage associated with the input.
[4] V_{CCO} is the supply voltage associated with the output.

10. Static characteristics

Table 7. Typical static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); T_{amb} = 25 °C.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	A port; $V_{CC(A)}$ = 1.2 V; I_O = -20 μA	-	1.1	-	V
V_{OL}	LOW-level output voltage	A port; $V_{CC(A)}$ = 1.2 V; I_O = 20 μA	-	0.09	-	V
I_I	input leakage current	OE input; V_I = 0 V to 3.6 V; $V_{CC(A)}$ = 1.2 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	-	-	±1	μA
I_{OZ}	OFF-state output current	A or B port; V_O = 0 V to V_{CCO}; $V_{CC(A)}$ = 1.2 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V [2]	-	-	±1	μA
I_{OFF}	power-off leakage current	A port; V_I or V_O = 0 V to 3.6 V; $V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 0 V to 5.5 V	-	-	±1	μA
		B port; V_I or V_O = 0 V to 5.5 V; $V_{CC(B)}$ = 0 V; $V_{CC(A)}$ = 0 V to 3.6 V	-	-	±1	μA
C_I	input capacitance	OE input; $V_{CC(A)}$ = 1.2 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	-	1.6	-	pF
$C_{I/O}$	input/output capacitance	A port; $V_{CC(A)}$ = 1.2 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	-	4.0	-	pF
		B port; $V_{CC(A)}$ = 1.2 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	-	7.5	-	pF

[1] $V_{CC(A)}$ must be less than or equal to $V_{CC(B)}$.
[2] V_{CCO} is the supply voltage associated with the output.

Table 8. Typical supply current

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); T_{amb} = 25 °C.

$V_{CC(A)}$	$V_{CC(B)}$								Unit
	1.8 V		2.5 V		3.3 V		5.0 V		
	$I_{CC(A)}$	$I_{CC(B)}$	$I_{CC(A)}$	$I_{CC(B)}$	$I_{CC(A)}$	$I_{CC(B)}$	$I_{CC(A)}$	$I_{CC(B)}$	
1.2 V	10	10	10	10	10	20	10	1050	nA
1.5 V	10	10	10	10	10	10	10	650	nA
1.8 V	10	10	10	10	10	10	10	350	nA
2.5 V	-	-	10	10	10	10	10	40	nA
3.3 V	-	-	-	-	10	10	10	10	nA

Table 9. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).[1]

Symbol	Parameter	Conditions		-40 °C to +85 °C		-40 °C to +125 °C		Unit
				Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	A or B port and OE input	[2]					
		$V_{CC(A)}$ = 1.2 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V		$0.65V_{CCI}$	-	$0.65V_{CCI}$	-	V
V_{IL}	LOW-level input voltage	A or B port and OE input	[2]					
		$V_{CC(A)}$ = 1.2 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V		-	$0.35V_{CCI}$	-	$0.35V_{CCI}$	V
V_{OH}	HIGH-level output voltage	A or B port; I_O = -20 μA	[3]					
		A port; $V_{CC(A)}$ = 1.4 V to 3.6 V		V_{CCO} - 0.4	-	V_{CCO} - 0.4	-	V
		B port; $V_{CC(B)}$ = 1.65 V to 5.5 V		V_{CCO} - 0.4	-	V_{CCO} - 0.4	-	V
V_{OL}	LOW-level output voltage	A or B port; I_O = 20 μA	[3]					
		A port; $V_{CC(A)}$ = 1.4 V to 3.6 V		-	0.4	-	0.4	V
		B port; $V_{CC(B)}$ = 1.65 V to 5.5 V		-	0.4	-	0.4	V
I_I	input leakage current	OE input; V_I = 0 V to 3.6 V; $V_{CC(A)}$ = 1.2 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V		-	±2	-	±5	μA
I_{OZ}	OFF-state output current	A or B port; V_O = 0 V or V_{CCO}; $V_{CC(A)}$ = 1.2 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	[3]	-	±2	-	±10	μA
I_{OFF}	power-off leakage current	A port; V_I or V_O = 0 V to 3.6 V; $V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 0 V to 5.5 V		-	±2	-	±10	μA
		B port; V_I or V_O = 0 V to 5.5 V; $V_{CC(B)}$ = 0 V; $V_{CC(A)}$ = 0 V to 3.6 V		-	±2	-	±10	μA

Symbol	Parameter	Conditions		-40 °C to +85 °C		-40 °C to +125 °C		Unit
				Min	Max	Min	Max	
I_{CC}	supply current	V_I = 0 V or V_{CCI}; I_O = 0 A	[2]					
		$I_{CC(A)}$						
		OE = LOW; $V_{CC(A)}$ = 1.4 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V		-	3	-	15	μA
		OE = HIGH; $V_{CC(A)}$ = 1.4 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V		-	3	-	20	μA
		$V_{CC(A)}$ = 3.6 V; $V_{CC(B)}$ = 0 V		-	2	-	15	μA
		$V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 5.5 V		-	-2	-	-15	μA
		$I_{CC(B)}$						
		OE = LOW; $V_{CC(A)}$ = 1.4 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V		-	5	-	15	μA
		OE = HIGH; $V_{CC(A)}$ = 1.4 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V		-	5	-	20	μA
		$V_{CC(A)}$ = 3.6 V; $V_{CC(B)}$ = 0 V		-	-2	-	-15	μA
		$V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 5.5 V		-	2	-	15	μA
		$I_{CC(A)} + I_{CC(B)}$						
		$V_{CC(A)}$ = 1.4 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V		-	8	-	40	μA

[1] $V_{CC(A)}$ must be less than or equal to $V_{CC(B)}$.
[2] V_{CCI} is the supply voltage associated with the input.
[3] V_{CCO} is the supply voltage associated with the output.

11. Dynamic characteristics

Table 10. Typical dynamic characteristics for temperature 25 °C

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 8; for waveforms see Fig. 5, Fig. 6 and Fig. 7.

Symbol [1]	Parameter	Conditions		$V_{CC(B)}$				Unit
				1.8 V	2.5 V	3.3 V	5.0 V	
$V_{CC(A)}$ = 1.2 V; T_{amb} = 25 °C								
t_{pd}	propagation delay	A to B		7.5	6.0	5.5	5.2	ns
		B to A		6.6	5.6	5.1	4.9	ns
t_{en}	enable time	OE to A, B		0.5	0.5	0.5	0.5	μs
t_{dis}	disable time	OE to A; no external load	[2]	8.3	8.3	8.3	8.3	ns
		OE to B; no external load	[2]	10.4	9.4	9.3	8.8	ns
		OE to A		81	69	83	68	ns
		OE to B		81	69	83	68	ns
t_t	transition time	A port		4.3	4.3	4.3	4.4	ns
		B port		2.7	2.1	1.8	1.5	ns
t_W	pulse width	data inputs		15	13	13	13	ns
f_{data}	data rate			70	80	80	80	Mbps

[1] t_{pd} is the same as t_{PLH} and t_{PHL}; t_{en} is the same as t_{PZL} and t_{PZH}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_t is the same as t_{THL} and t_{TLH}
[2] Delay between OE going LOW and when the outputs are actually disabled.

Table 11. Dynamic characteristics for temperature range -40 °C to +85 °C

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 8; for waveforms see Fig. 5, Fig. 6 and Fig. 7.

Symbol [1]	Parameter	Conditions	$V_{CC(B)}$								Unit
			1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	
$V_{CC(A)}$ = 1.5 V ± 0.1 V											
t_{pd}	propagation delay	A to B	1.4	12.9	1.2	10.1	1.1	10.0	0.8	9.9	ns
		B to A	0.9	14.2	0.7	12.0	0.4	11.7	0.3	13.7	ns
t_{en}	enable time	OE to A, B	-	1.0	-	1.0	-	1.0	-	1.0	μs
t_{dis}	disable time	OE to A; no external load [2]	1.0	17.9	1.0	17.9	1.0	17.9	1.0	17.9	ns
		OE to B; no external load [2]	1.0	21.0	1.0	16.6	1.0	15.1	1.0	14.4	ns
		OE to A	-	100	-	100	-	100	-	100	ns
		OE to B	-	150	-	105	-	150	-	105	ns
t_t	transition time	A port	0.9	5.1	0.9	5.1	0.9	5.1	0.9	5.1	ns
		B port	0.9	4.7	0.6	3.2	0.5	2.5	0.4	2.7	ns
t_W	pulse width	data inputs	25	-	25	-	25	-	25	-	ns
f_{data}	data rate		-	40	-	40	-	40	-	40	Mbps
$V_{CC(A)}$ = 1.8 V ± 0.15 V											
t_{pd}	propagation delay	A to B	1.6	11.0	1.4	7.7	1.3	6.8	1.2	6.5	ns
		B to A	1.5	12.0	1.3	8.4	1.0	7.6	0.9	7.1	ns
t_{en}	enable time	OE to A, B	-	1.0	-	1.0	-	1.0	-	1.0	μs
t_{dis}	disable time	OE to A; no external load [2]	1.0	14.7	1.0	14.7	1.0	14.7	1.0	14.7	ns
		OE to B; no external load [2]	1.0	18.2	1.0	14.5	1.0	13.7	1.0	12.7	ns
		OE to A	-	120	-	120	-	120	-	120	ns
		OE to B	-	150	-	105	-	150	-	105	ns
t_t	transition time	A port	0.8	4.1	0.8	4.1	0.8	4.1	0.8	4.1	ns
		B port	0.9	4.7	0.6	3.2	0.5	2.5	0.4	2.7	ns
t_W	pulse width	data inputs	20	-	17	-	17	-	17	-	ns
f_{data}	data rate		-	49	-	60	-	60	-	60	Mbps
$V_{CC(A)}$ = 2.5 V ± 0.2 V											
t_{pd}	propagation delay	A to B	-	-	1.1	6.3	1.0	5.2	0.9	4.7	ns
		B to A	-	-	1.2	6.6	1.1	5.1	0.9	4.4	ns
t_{en}	enable time	OE to A, B	-	-	-	1.0	-	1.0	-	1.0	μs
t_{dis}	disable time	OE to A; no external load [2]	-	-	1.0	9.7	1.0	9.7	1.0	9.7	ns
		OE to B; no external load [2]	-	-	1.0	12.9	1.0	12.0	1.0	11.0	ns
		OE to A	-	-	-	85	-	85	-	85	ns
		OE to B	-	-	-	105	-	150	-	100	ns
t_t	transition time	A port	-	-	0.7	3.0	0.7	3.0	0.7	3.0	ns
		B port	-	-	0.7	3.2	0.5	2.5	0.4	2.7	ns
t_W	pulse width	data inputs	-	-	12	-	10	-	10	-	ns
f_{data}	data rate		-	-	-	85	-	100	-	100	Mbps

Symbol [1]	Parameter	Conditions	$V_{CC(B)}$								Unit
			1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	
$V_{CC(A)}$ = 3.3 V ± 0.3 V											
t_{pd}	propagation delay	A to B	-	-	-	-	0.9	4.7	0.8	4.0	ns
		B to A	-	-	-	-	1.0	4.9	0.9	3.8	ns
t_{en}	enable time	OE to A, B	-	-	-	-	-	1.0	-	1.0	μs
t_{dis}	disable time	OE to A; no external load [2]	-	-	-	-	1.0	9.4	1.0	9.4	ns
		OE to B; no external load [2]	-	-	-	-	1.0	11.3	1.0	10.4	ns
		OE to A	-	-	-	-	-	125	-	125	ns
		OE to B	-	-	-	-	-	150	-	100	ns
t_t	transition time	A port	-	-	-	-	0.7	2.5	0.7	2.5	ns
		B port	-	-	-	-	0.5	2.5	0.4	2.7	ns
t_W	pulse width	data inputs	-	-	-	-	10	-	10	-	ns
f_{data}	data rate		-	-	-	-	-	100	-	100	Mbps

[1] t_{pd} is the same as t_{PLH} and t_{PHL}; t_{en} is the same as t_{PZL} and t_{PZH}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_t is the same as t_{THL} and t_{TLH}

[2] Delay between OE going LOW and when the outputs are actually disabled.

Table 12. Dynamic characteristics for temperature range -40 °C to +125 °C

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 8; for waveforms see Fig. 5, Fig. 6 and Fig. 7.

Symbol [1]	Parameter	Conditions	$V_{CC(B)}$								Unit
			1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	
$V_{CC(A)}$ = 1.5 V ± 0.1 V											
t_{pd}	propagation delay	A to B	1.4	15.9	1.2	13.1	1.1	13.0	0.8	12.9	ns
		B to A	0.9	17.2	0.7	15.0	0.4	14.7	0.3	16.7	ns
t_{en}	enable time	OE to A, B	-	1.0	-	1.0	-	1.0	-	1.0	μs
t_{dis}	disable time	OE to A; no external load [2]	1.0	18.3	1.0	18.3	1.0	18.3	1.0	18.3	ns
		OE to B; no external load [2]	1.0	21.8	1.0	17.7	1.0	16.1	1.0	15.2	ns
		OE to A	-	105	-	105	-	105	-	105	ns
		OE to B	-	155	-	110	-	155	-	105	ns
t_t	transition time	A port	0.9	7.1	0.9	7.1	0.9	7.1	0.9	7.1	ns
		B port	0.9	6.5	0.6	5.2	0.5	4.8	0.4	4.7	ns
t_W	pulse width	data inputs	25	-	25	-	25	-	25	-	ns
f_{data}	data rate		-	40	-	40	-	40	-	40	Mbps

Symbol [1]	Parameter	Conditions	$V_{CC(B)}$								Unit
			1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	
$V_{CC(A)}$ = 1.8 V ± 0.15 V											
t_{pd}	propagation delay	A to B	1.6	14.0	1.4	10.7	1.3	9.8	1.2	9.5	ns
		B to A	1.5	15.0	1.3	11.4	1.0	10.6	0.9	10.1	ns
t_{en}	enable time	OE to A, B	-	1.0	-	1.0	-	1.0	-	1.0	μs
t_{dis}	disable time	OE to A; no external load [2]	1.0	15.0	1.0	15.0	1.0	15.0	1.0	15.0	ns
		OE to B; no external load [2]	1.0	19.8	1.0	15.3	1.0	14.5	1.0	13.5	ns
		OE to A	-	125	-	125	-	125	-	125	ns
		OE to B	-	150	-	105	-	150	-	105	ns
t_t	transition time	A port	0.8	6.2	0.8	6.1	0.8	6.1	0.8	6.1	ns
		B port	0.9	5.8	0.6	5.2	0.5	4.8	0.4	4.7	ns
t_W	pulse width	data inputs	22	-	19	-	19	-	19	-	ns
f_{data}	data rate		-	45	-	55	-	55	-	55	Mbps
$V_{CC(A)}$ = 2.5 V ± 0.2 V											
t_{pd}	propagation delay	A to B	-	-	1.1	9.3	1.0	8.2	0.9	7.7	ns
		B to A	-	-	1.2	9.6	1.1	8.1	0.9	7.4	ns
t_{en}	enable time	OE to A, B	-	-	-	1.0	-	1.0	-	1.0	μs
t_{dis}	disable time	OE to A; no external load [2]	-	-	1.0	10.1	1.0	10.1	1.0	10.1	ns
		OE to B; no external load [2]	-	-	1.0	13.5	1.0	12.7	1.0	11.7	ns
		OE to A	-	-	-	85	-	85	-	85	ns
		OE to B	-	-	-	105	-	150	-	100	ns
t_t	transition time	A port	-	-	0.7	5.0	0.7	5.0	0.7	5.0	ns
		B port	-	-	0.7	4.6	0.5	4.8	0.4	4.7	ns
t_W	pulse width	data inputs	-	-	14	-	13	-	10	-	ns
f_{data}	data rate		-	-	-	75	-	80	-	100	Mbps
$V_{CC(A)}$ = 3.3 V ± 0.3 V											
t_{pd}	propagation delay	A to B	-	-	-	-	0.9	7.7	0.8	7.0	ns
		B to A	-	-	-	-	1.0	7.9	0.9	6.8	ns
t_{en}	enable time	OE to A, B	-	-	-	-	-	1.0	-	1.0	μs
t_{dis}	disable time	OE to A; no external load [2]	-	-	-	-	1.0	9.9	1.0	9.9	ns
		OE to B; no external load [2]	-	-	-	-	1.0	12.1	1.0	10.9	ns
		OE to A	-	-	-	-	-	125	-	125	ns
		OE to B	-	-	-	-	-	150	-	150	ns
t_t	transition time	A port	-	-	-	-	0.7	4.5	0.7	4.5	ns
		B port	-	-	-	-	0.5	4.1	0.4	4.7	ns
t_W	pulse width	data inputs	-	-	-	-	10	-	10	-	ns
f_{data}	data rate		-	-	-	-	-	100	-	100	Mbps

[1] t_{pd} is the same as t_{PLH} and t_{PHL}; t_{en} is the same as t_{PZL} and t_{PZH}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_t is the same as t_{THL} and t_{TLH}

[2] Delay between OE going LOW and when the outputs are actually disabled.

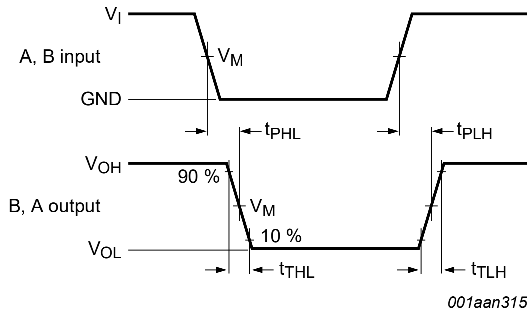
Table 13. Typical power dissipation capacitance

Voltages are referenced to GND (ground = 0 V). [1] [2]

Symbol	Parameter	Conditions	$V_{CC(A)}$							Unit
			1.2 V	1.2 V	1.5 V	1.8 V	2.5 V	2.5 V	3.3 V	
			$V_{CC(B)}$							
			1.8 V	5.0 V	1.8 V	1.8 V	2.5 V	5.0 V	3.3 V to 5.0 V	
T_{amb} = 25 °C										
C_{PD}	power dissipation capacitance	outputs enabled; OE = $V_{CC(A)}$								
		A port: (direction A to B)	6	5	6	6	6	5	5	pF
		A port: (direction B to A)	8	8	8	8	8	8	8	pF
		B port: (direction A to B)	26	30	26	26	27	30	30	pF
		B port: (direction B to A)	23	28	22	22	22	26	26	pF
		outputs disabled; OE = GND								
		A port: (direction A to B)	0.05	0.05	0.05	0.09	0.08	0.08	0.06	pF
		A port: (direction B to A)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	pF
		B port: (direction A to B)	0.00	0.02	0.00	0.00	0.00	0.00	0.00	pF
		B port: (direction B to A)	0.06	0.09	0.06	0.06	0.06	0.07	0.07	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}{}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}{}^2 \times f_o)$ where:
f_i = input frequency in MHz; f_o = output frequency in MHz; C_L = load capacitance in pF;
V_{CC} = supply voltage in V; N = number of inputs switching; $\Sigma(C_L \times V_{CC}{}^2 \times f_o)$ = sum of the outputs.
[2] f_i = 10 MHz; V_I = GND to V_{CC}; $t_r = t_f$ = 1 ns; C_L = 0 pF; $R_L = \infty\ \Omega$.

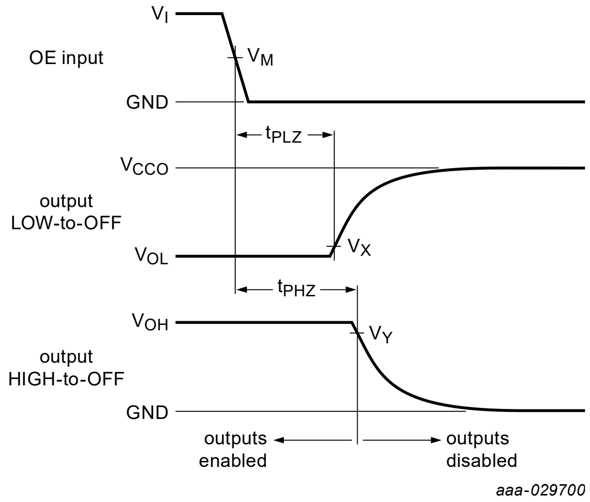
11.1. Waveforms and test circuit



Measurement points are given in Table 14.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 5. The data input (An, Bn) to data output (Bn, An) propagation delay times

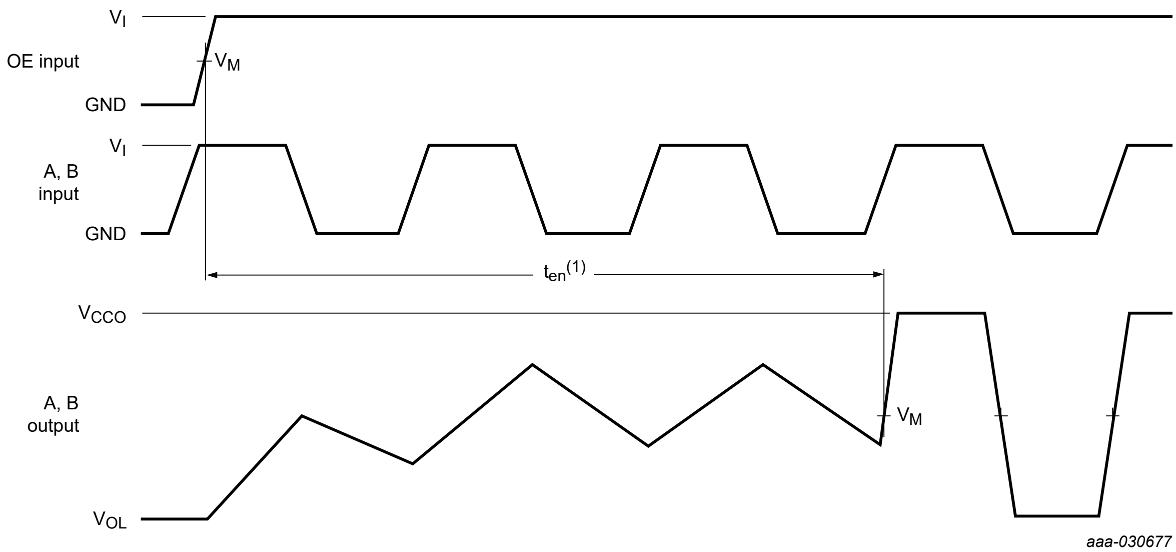


Measurement points are given in Table 14.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

V_{CCO} is the supply voltage associated with the output.

Fig. 6. Disable times



(1) The enable time (t_{en}) indicates the amount of time the user must allow for one one-shot circuitry to become operational after OE is taken HIGH. See also Section 12.6

Measurement points are given in Table 14.

V_{OL} is a typical output voltage level that occur with the output load.

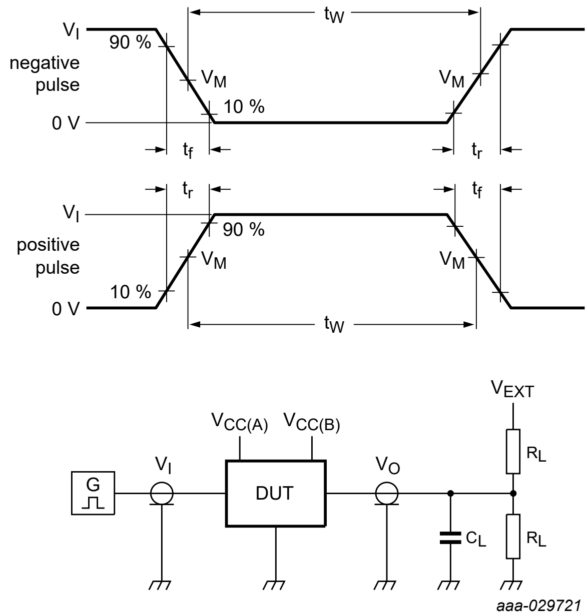
V_{CCO} is the supply voltage associated with the output.

Fig. 7. Enable times

Table 14. Measurement points [1]

Supply voltage	Input	Output		
V_{CCO}	V_M	V_M	V_X	V_Y
1.2 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.1 V	V_{OH} - 0.1 V
1.5 V ± 0.1 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.1 V	V_{OH} - 0.1 V
1.8 V ± 0.15 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.15 V	V_{OH} - 0.15 V
2.5 V ± 0.2 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.15 V	V_{OH} - 0.15 V
3.3 V ± 0.3 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.3 V	V_{OH} - 0.3 V
5.0 V ± 0.5 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.3 V	V_{OH} - 0.3 V

[1] V_{CCI} is the supply voltage associated with the input and V_{CCO} is the supply voltage associated with the output.



Test data is given in Table 15.
All input pulses are supplied by generators having the following characteristics:
PRR ≤ 10 MHz; Z_O = 50 Ω; dV/dt ≥ 1.0 V/ns.
R_L = Load resistance.
C_L = Load capacitance including jig and probe capacitance.
V_{EXT} = External voltage for measuring switching times.

Fig. 8. Test circuit for measuring switching times

Table 15. Test data

Supply voltage		Input		Load		V_{EXT}			
$V_{CC(A)}$	$V_{CC(B)}$	V_I [1]	Δt/ΔV	C_L	R_L [2]	t_{PLH}, t_{PHL}	t_{en}	t_{PHZ}	t_{PLZ} [3]
1.2 V to 3.6 V	1.65 V to 5.5 V	V_{CCI}	≤ 1.0 ns/V	15 pF	50 kΩ, 1 MΩ	open	open	open	$2V_{CCO}$

[1] V_{CCI} is the supply voltage associated with the input.
[2] For measuring data rate, pulse width, propagation delay, output rise and fall time and enable time, R_L = 1 MΩ. For measuring disable time, R_L = 50 kΩ.
[3] V_{CCO} is the supply voltage associated with the output.

12. Application information

12.1. Applications

Voltage level-translation applications. The NXB0101 can be used to interface between devices or systems operating at different supply voltages. See Fig. 9 for a typical operating circuit using the NXB0101.

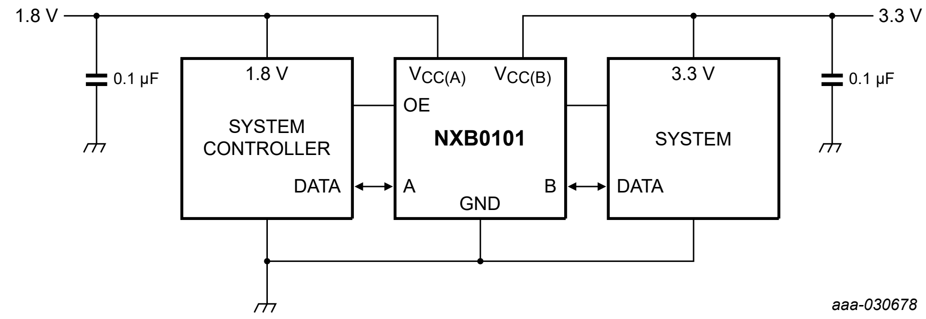


Fig. 9. Typical operating circuit

12.2. Architecture

The architecture of the NXB0101 is shown in Fig. 10. The device does not require an extra input signal to control the direction of data flow from A to B or from B to A. In a static state, the output drivers of the NXB0101 can maintain a defined output level, but the output architecture is designed to be weak, so that they can be overdriven by an external driver when data on the bus starts flowing in the opposite direction. The output one shots detect rising or falling edges on the A or B ports. During a rising edge, the one shots turn on the PMOS transistors (T1, T3) for a short duration, accelerating the low-to-high transition. Similarly, during a falling edge, the one shots turn on the NMOS transistors (T2, T4) for a short duration, accelerating the high-to-low transition. During output transitions the typical output impedance is 70 Ω at V_{CCO} = 1.2 V to 1.8 V, 50 Ω at V_{CCO} = 1.8 V to 3.3 V and 40 Ω at V_{CCO} = 3.3 V to 5.0 V.

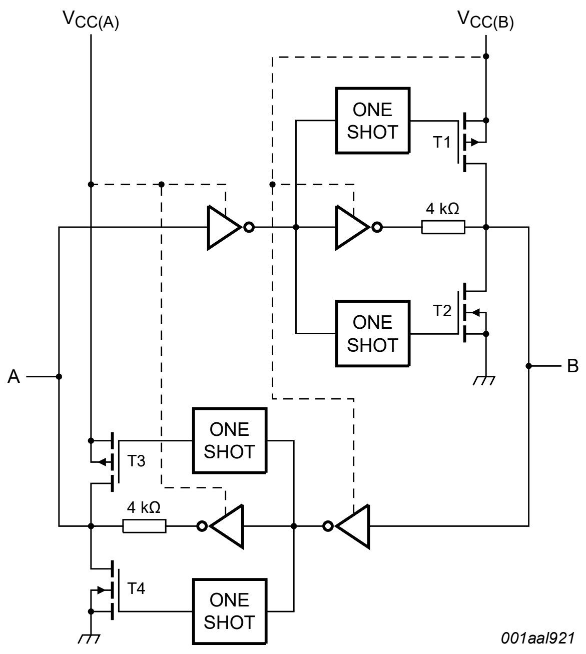
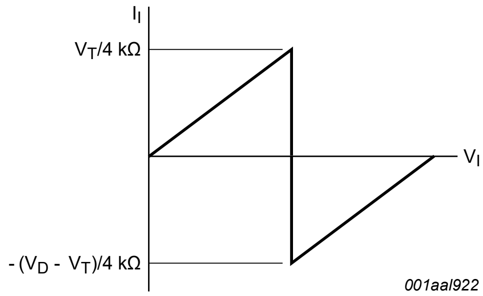


Fig. 10. Architecture of NXB0101 I/O cell (one channel)

12.3. Input driver requirements

For correct operation, the device driving the data I/Os of the NXB0101 must have a minimum drive capability of ±2 mA. See Fig. 11 for a plot of typical input current versus input voltage.



V_T: input threshold voltage of the NXB0101 (typically V_{CCI} / 2).

V_D: supply voltage of the external driver.

Fig. 11. Typical input current versus input voltage graph

12.4. Output load considerations

The maximum lumped capacitive load that can be driven is dependant upon the one-shot pulse duration. In cases with very heavy capacitive loading there is a risk that the output will not reach the positive rail within the one-shot pulse duration.To avoid excessive capacitive loading and to ensure correct triggering of the one-shot it's recommended to use short trace lengths and low capacitance connectors on NXS0101 PCB layouts. To ensure low impedance termination and avoid output signal oscillations and one-shot re-triggering, the length of the PCB trace should be such that the round trip delay of any reflection is within the one-shot pulse duration.

12.5. Power up

During operation $V_{CC(A)}$ must never be higher than $V_{CC(B)}$, however during power-up $V_{CC(A)} \geq V_{CC(B)}$ does not damage the device, so either power supply can be ramped up first. There is no special power-up sequencing required. The NXB0101 includes circuitry that disables all output ports when either $V_{CC(A)}$ or $V_{CC(B)}$ is switched off.

12.6. Enable and disable

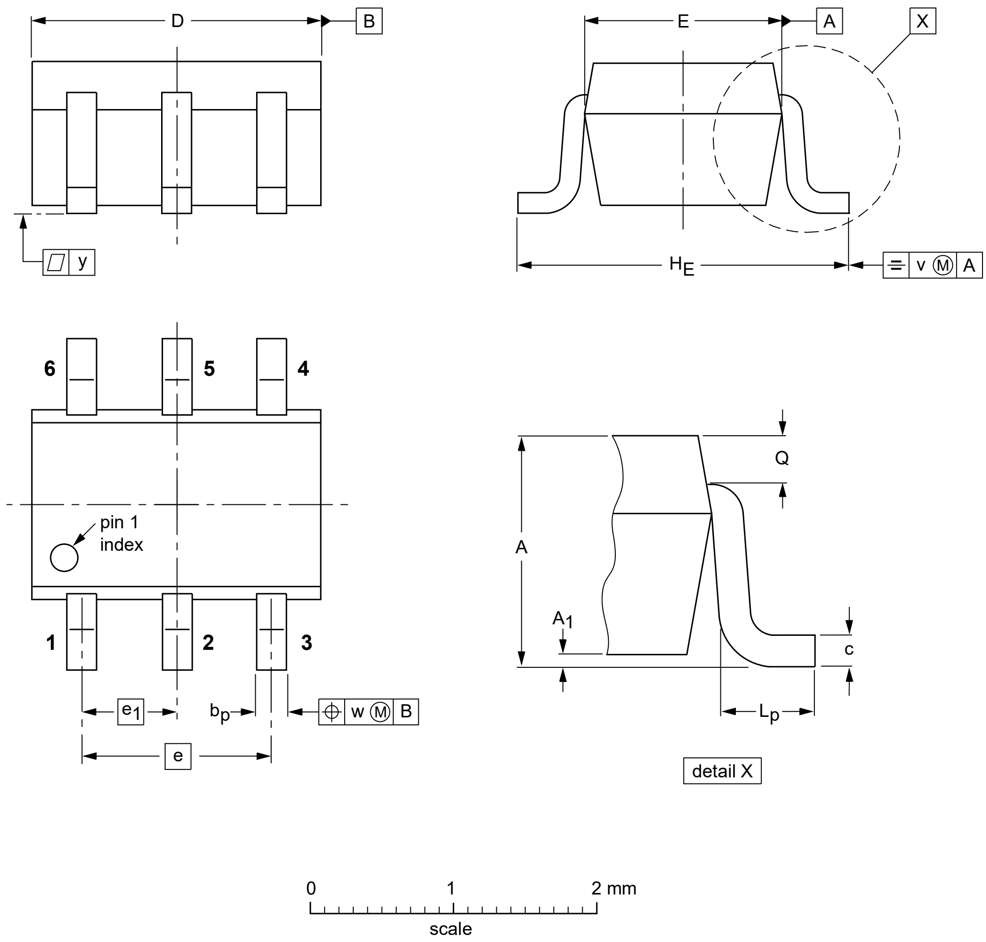
An output enable input (OE) is used to disable the device. Setting OE = LOW causes all I/Os to assume the high-impedance OFF-state. The disable time (t_{dis} with no external load) indicates the delay between when OE goes LOW and when outputs actually become disabled. The enable time (t_{en}) indicates the amount of time the user must allow for one one-shot circuitry to become operational after OE is taken HIGH. To ensure the high-impedance OFF-state during power-up or power-down, pin OE should be tied to GND through a pull-down resistor, the minimum value of the resistor is determined by the current-sourcing capability of the driver.

12.7. Pull-up or pull-down resistors on I/O lines

As mentioned previously the NXB0101 is designed with low static drive strength to drive capacitive loads of up to 70 pF. To avoid output contention issues, any pull-up or pull-down resistors used must be kept higher than 50 kΩ. For this reason the NXB0101 is not recommended for use in open drain driver applications such as 1-Wire or I^2C. For these applications, the NXS0101 level translator is recommended.

13. Package outline

Plastic surface-mounted package; 6 leads **SOT363**



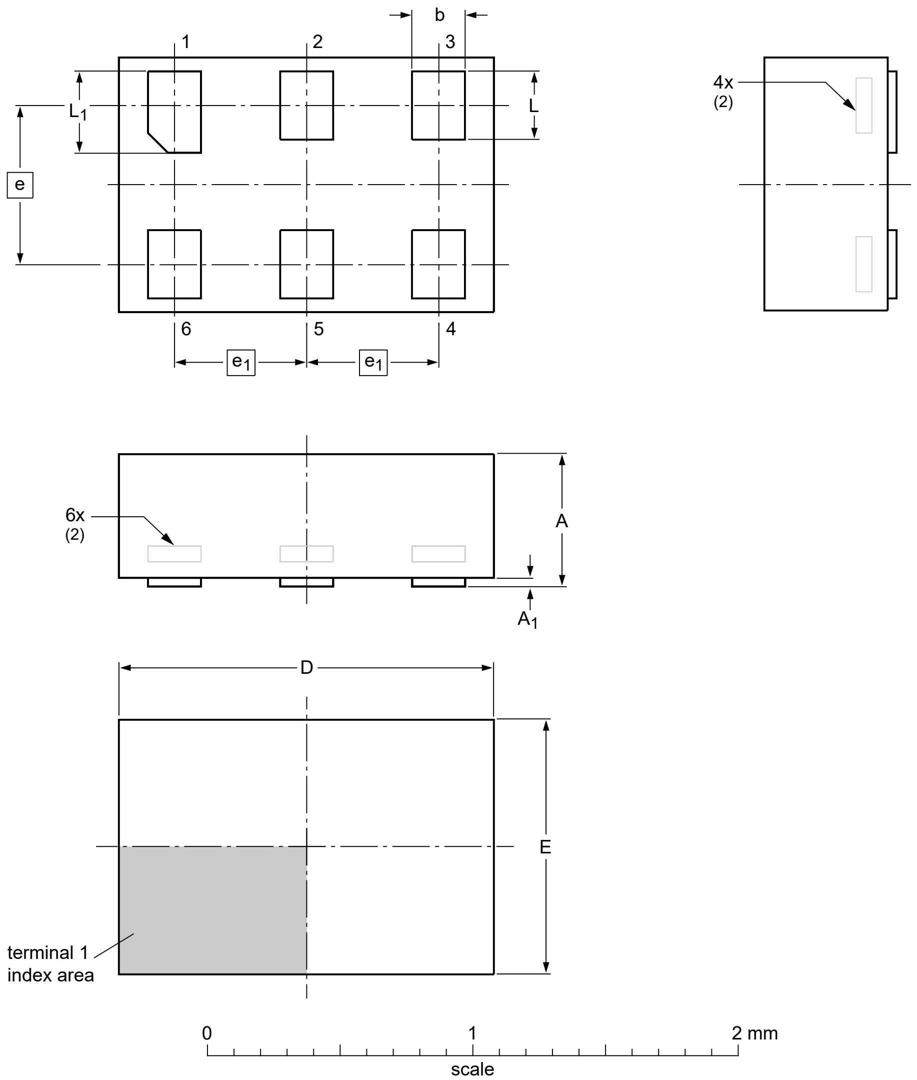
DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT363			SC-88			~~04-11-08~~ 06-03-16

Fig. 12. Package outline SOT363 (SC-88)

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm SOT886



Dimensions (mm are the original dimensions)

Unit		A(1)	A_1	b	D	E	e	e_1	L	L_1
mm	max	0.5	0.04	0.25	1.50	1.05			0.35	0.40
	nom			0.20	1.45	1.00	0.6	0.5	0.30	0.35
	min			0.17	1.40	0.95			0.27	0.32

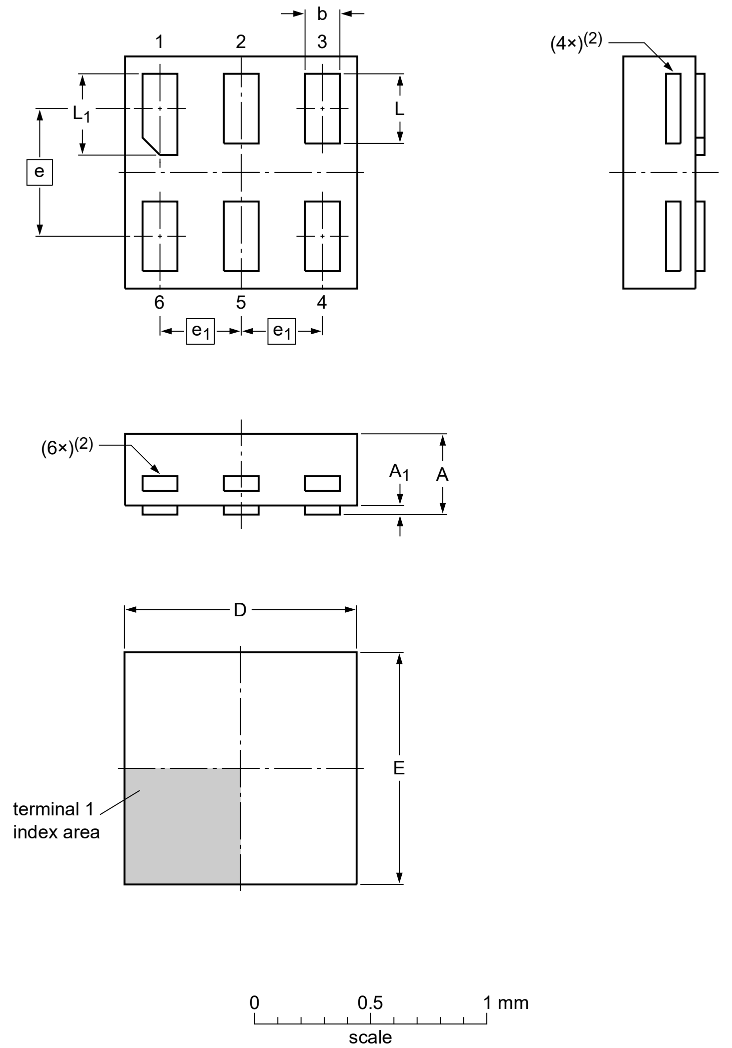
Notes
1. Including plating thickness.
2. Can be visible in some manufacturing processes.

sot886_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT886		MO-252				~~04-07-22~~ 12-01-05

Fig. 13. Package outline SOT886 (XSON6)

XSON6: extremely thin small outline package; no leads; 6 terminals; body 1.0 x 1.0 x 0.35 mm **SOT1202**



Dimensions

Unit		A(1)	A1	b	D	E	e	e1	L	L1
mm	max	0.35	0.04	0.20	1.05	1.05			0.35	0.40
	nom			0.15	1.00	1.00	0.55	0.35	0.30	0.35
	min			0.12	0.95	0.95			0.27	0.32

Note
1. Including plating thickness.
2. Visible depending upon used manufacturing technology.

sot1202_po

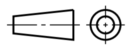
Outline version	References IEC	JEDEC	JEITA		European projection	Issue date
SOT1202						~~10-04-02~~ 10-04-06

Fig. 14. Package outline SOT1202 (XSON6)

14. Abbreviations

Table 16. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	Electro Static Discharge
HBM	Human Body Model
MM	Machine Model

15. Revision history

Table 17. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NXB0101 v.3	20210823	Product data sheet	-	NXB0101 v.2
Modifications:	• Type number NXB0101GW (SOT363-1/SC-88) added.			
NXB0101 v.2	20201113	Product data sheet	-	NXB0101 v.1.1
Modifications:	• Table 11 and Table 12: Disable times updated.			
NXB0101 v.1.1	20200406	Product data sheet	-	-

16. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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Date of release: 23 August 2021