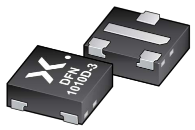


PBHV9515QA

150 V, 500 mA PNP high-voltage low VCEsat (BISS) transistor

19 November 2015 — Product data sheet

1. General description

PNP high-voltage low V_{CEsat} Breakthrough In Small Signal (BISS) transistor in a leadless ultra small DFN1010D-3 (SOT1215) Surface-Mounted Device (SMD) plastic package with visible and solderable side pads.

NPN complement: PBHV8515QA.

2. Features and benefits

- High voltage
- Low collector-emitter saturation voltage V_{CEsat}
- High collector current capability I_C and I_{CM}
- High collector current gain (h_{FE}) at high I_C
- Low package height of 0.37 mm
- AEC-Q101 qualified
- Suitable for Automatic Optical Inspection (AOI) of solder joint

3. Applications

- LED driver for LED chain module
- High Intensity Discharge (HID) front lighting
- Automotive motor management
- Switch Mode Power Supply (SMPS)

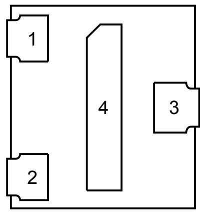
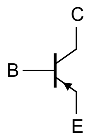
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CEO}	collector-emitter voltage	open base		-	-	-150	V
I_C	collector current			-	-	-500	mA
h_{FE}	DC current gain	V_{CE} = -10 V; I_C = -100 mA; pulsed; $t_p \leq 300$ µs; $\delta \leq 0.02$; T_{amb} = 25 °C		100	200	-	

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	B	base	 Transparent top view **DFN1010D-3 (SOT1215)**	 sym132
2	E	emitter		
3	C	collector		
4	C	collector		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PBHV9515QA	DFN1010D-3	DFN1010D-3: plastic thermal enhanced ultra thin small outline package; no leads; 3 terminals; body 1.1 x 1.0 x 0.37 mm	SOT1215

7. Marking

Table 4. Marking codes

Type number	Marking code
PBHV9515QA	00 01 11

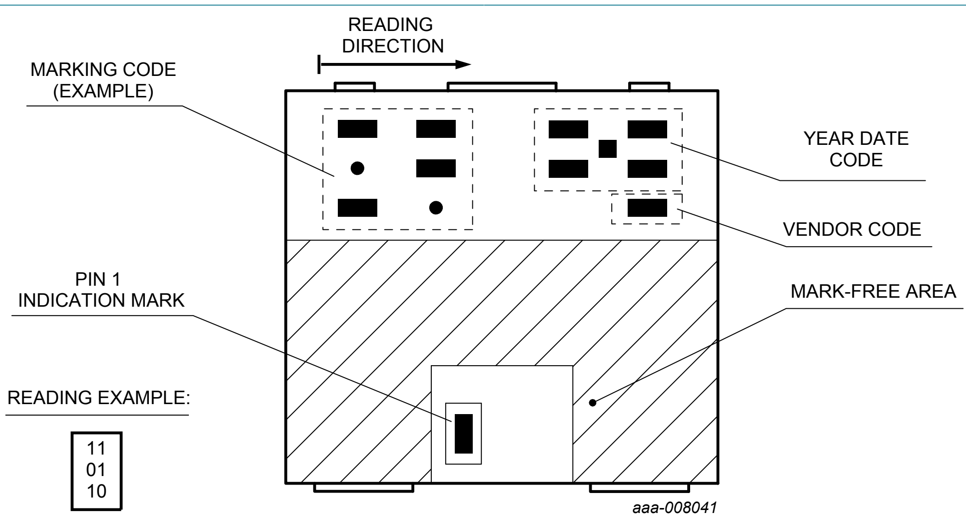


Fig. 1. DFN1010D-3 (SOT1215) binary marking code description

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CBO}	collector-base voltage	open emitter		-	-150	V
V_{CEO}	collector-emitter voltage	open base		-	-150	V
V_{EBO}	emitter-base voltage	open collector		-	-6	V
I_C	collector current			-	-500	mA
I_{CM}	peak collector current	single pulse; $t_p \leq 1$ ms		-	-1	A
I_{BM}	peak base current			-	-200	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[1]	-	325	mW
			[2]	-	600	mW
			[3]	-	740	mW
			[4]	-	540	mW
			[5]	-	1	W
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C

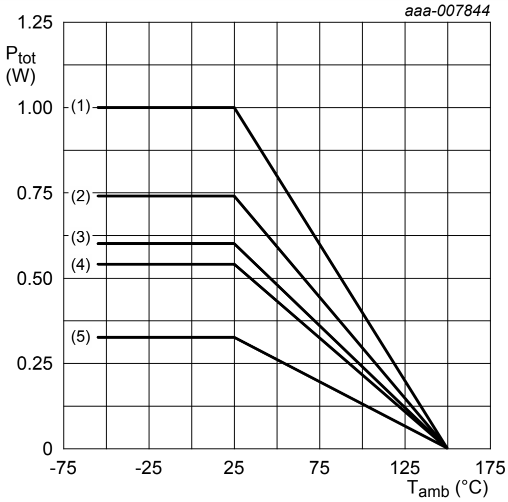
[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm^2.

[3] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 6 cm^2.

[4] Device mounted on an FR4 PCB, 4-layer copper, tin-plated and standard footprint.

[5] Device mounted on an FR4 PCB, 4-layer copper, tin-plated, mounting pad for collector 1 cm^2.



(1) FR4 PCB, 4-layer copper, 1 cm^2

(2) FR4 PCB, single-sided copper, 6 cm^2

(3) FR4 PCB, single-sided copper, 1 cm^2

(4) FR4 PCB, 4-layer copper, standard footprint

(5) FR4 PCB, single-sided copper, standard footprint

Fig. 2. Power derating curves

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	385	K/W
			[2]	-	-	209	K/W
			[3]	-	-	169	K/W
			[4]	-	-	232	K/W
			[5]	-	-	125	K/W

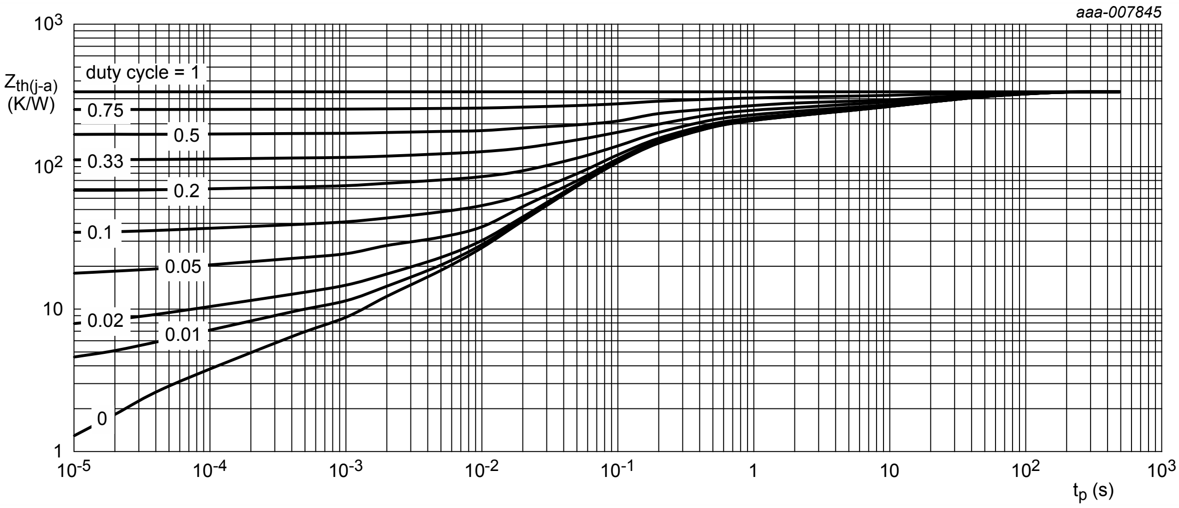
[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm^2.

[3] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 6 cm^2.

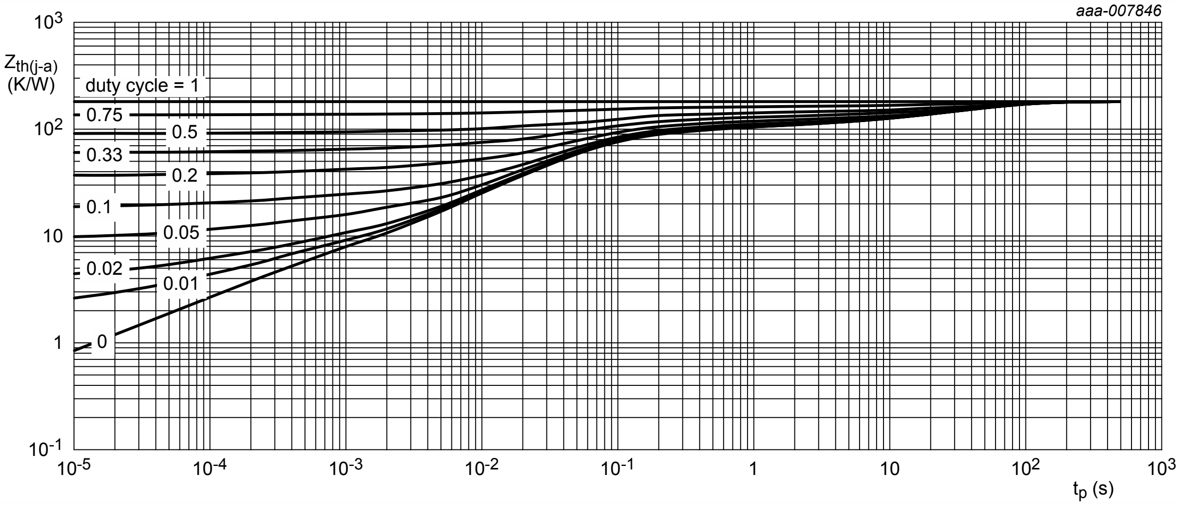
[4] Device mounted on an FR4 PCB, 4-layer copper, tin-plated and standard footprint.

[5] Device mounted on an FR4 PCB, 4-layer copper, tin-plated, mounting pad for collector 1 cm^2.



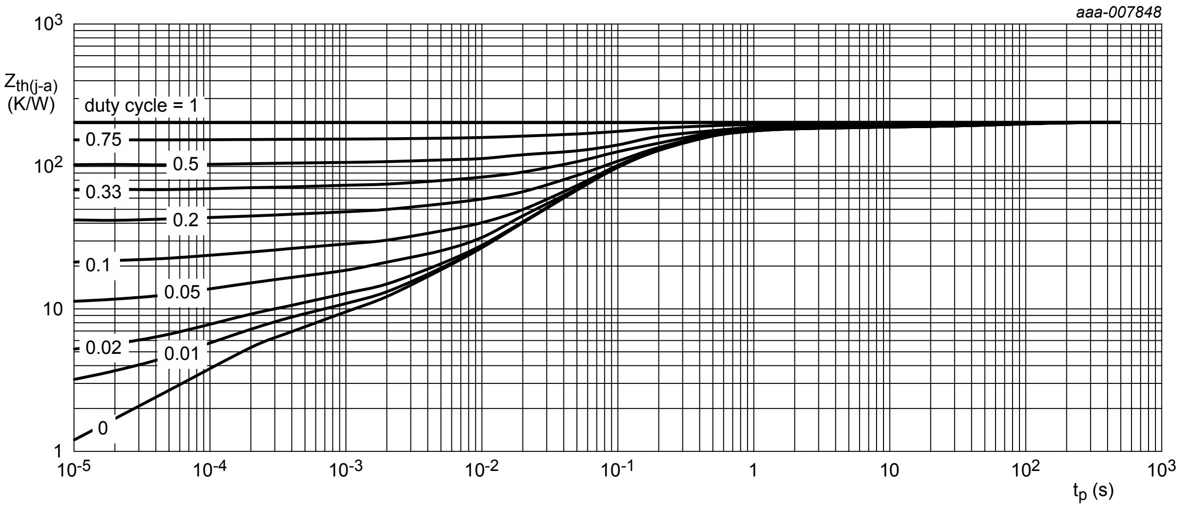
FR4 PCB, single-sided copper, standard footprint

Fig. 3. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



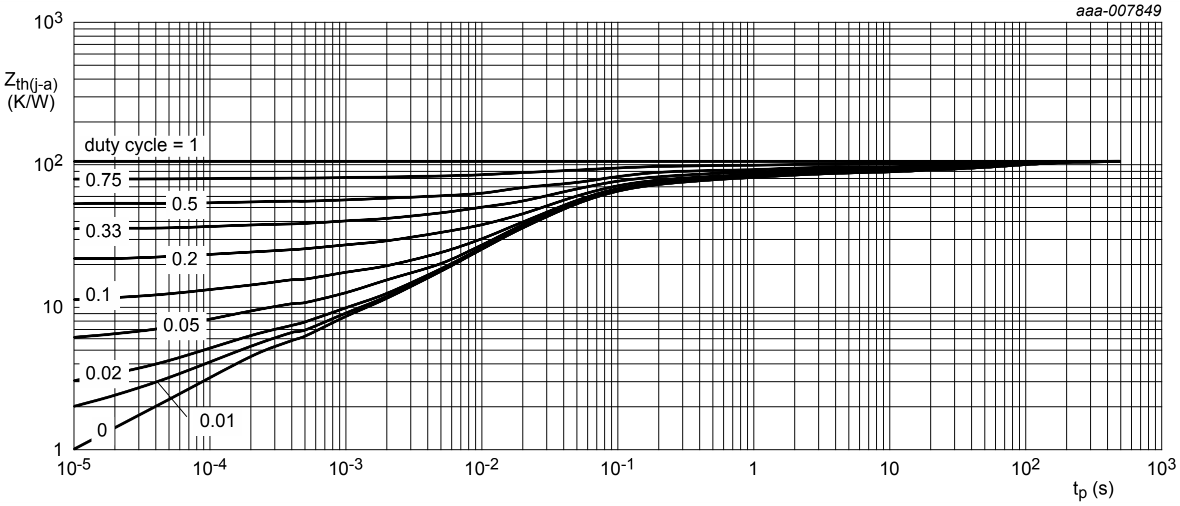
FR4 PCB, single-sided copper, 1 cm^2

Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, 4-layer copper, standard footprint

Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, 4-layer copper, 1 cm²

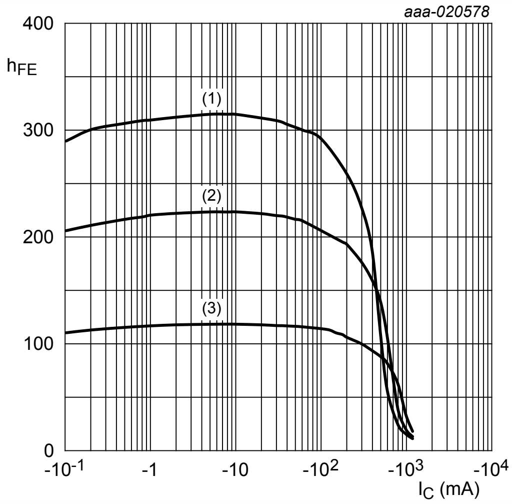
Fig. 6. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

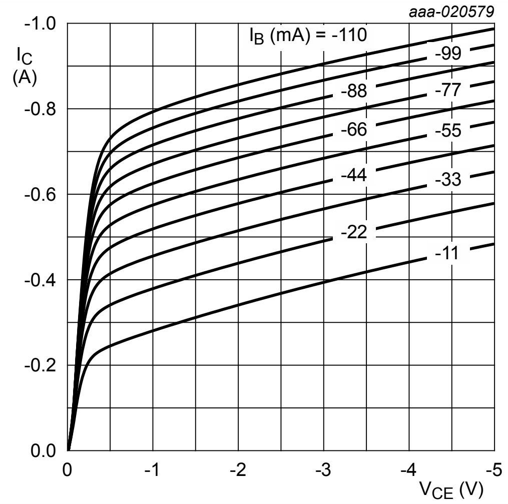
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{CBO}	collector-base cut-off current	V_{CB} = -120 V; I_E = 0 A; T_{amb} = 25 °C		-	-	-100	nA
		V_{CB} = -120 V; I_E = 0 A; T_j = 150 °C		-	-	-10	µA
I_{CES}	collector-emitter cut-off current	V_{CE} = -120 V; V_{BE} = 0 V; T_{amb} = 25 °C		-	-	-100	nA
I_{EBO}	emitter-base cut-off current	V_{EB} = -5 V; I_C = 0 A; T_{amb} = 25 °C		-	-	-100	nA
h_{FE}	DC current gain	V_{CE} = -10 V; I_C = -50 mA; pulsed; t_p ≤ 300 µs; δ ≤ 0.02; T_{amb} = 25 °C		100	210	-	
		V_{CE} = -10 V; I_C = -100 mA; pulsed; t_p ≤ 300 µs; δ ≤ 0.02; T_{amb} = 25 °C		100	200	-	
		V_{CE} = -10 V; I_C = -200 mA; pulsed; t_p ≤ 300 µs; δ ≤ 0.02; T_{amb} = 25 °C		100	190	-	
		V_{CE} = -10 V; I_C = -500 mA; pulsed; t_p ≤ 300 µs; δ ≤ 0.02; T_{amb} = 25 °C		70	135	-	
V_{CEsat}	collector-emitter saturation voltage	I_C = -50 mA; I_B = -5 mA; T_{amb} = 25 °C		-	-65	-110	mV
		I_C = -100 mA; I_B = -10 mA; pulsed; t_p ≤ 300 µs; δ ≤ 0.02; T_{amb} = 25 °C		-	-80	-140	mV
		I_C = -100 mA; I_B = -20 mA; pulsed; t_p ≤ 300 µs; δ ≤ 0.02; T_{amb} = 25 °C		-	-60	-110	mV
		I_C = -200 mA; I_B = -40 mA; pulsed; t_p ≤ 300 µs; δ ≤ 0.02; T_{amb} = 25 °C		-	-90	-160	mV
		I_C = -500 mA; I_B = -100 mA; pulsed; t_p ≤ 300 µs; δ ≤ 0.02; T_{amb} = 25 °C		-	-180	-300	mV
V_{BEsat}	base-emitter saturation voltage			-	-0.95	-1.2	V
t_d	delay time	V_{CC} = -10 V; I_C = -100 mA; I_{Bon} = -20 mA; I_{Boff} = 20 mA; T_{amb} = 25 °C		-	14	-	ns
t_r	rise time			-	46	-	ns
t_{on}	turn-on time			-	60	-	ns
t_s	storage time			-	455	-	ns
t_f	fall time			-	105	-	ns
t_{off}	turn-off time			-	560	-	ns
f_T	transition frequency	V_{CE} = -10 V; I_C = -10 mA; f = 100 MHz; T_{amb} = 25 °C		-	75	-	MHz
C_c	collector capacitance	V_{CB} = -20 V; I_E = 0 A; i_e = 0 A; f = 1 MHz; T_{amb} = 25 °C		-	4.7	-	pF

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
C_e	emitter capacitance	V_{EB} = -0.5 V; I_C = 0 A; i_c = 0 A; f = 1 MHz; T_{amb} = 25 °C		-	90	-	pF



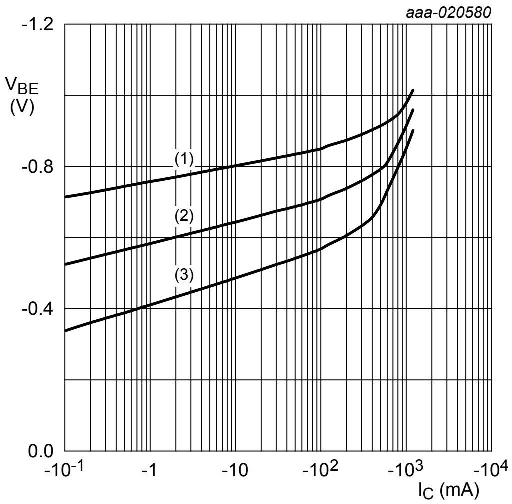
V_{CE} = -10 V
(1) T_{amb} = 100 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = -55 °C

Fig. 7. DC current gain as a function of collector current; typical values



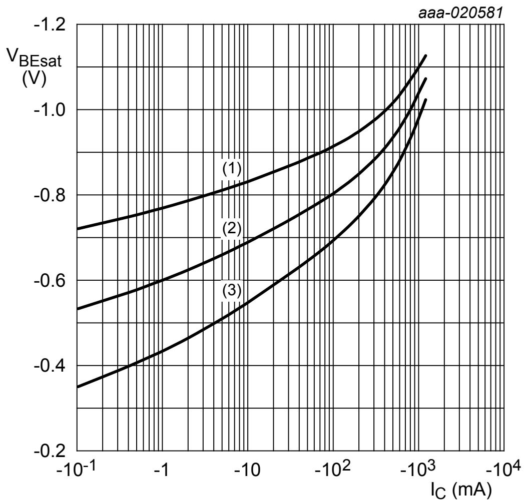
T_{amb} = 25 °C

Fig. 8. Collector current as a function of collector-emitter voltage; typical values



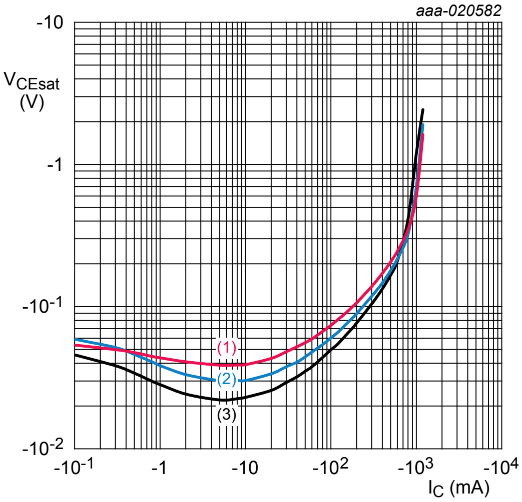
V_{CE} = -10 V
(1) T_{amb} = -55 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 100 °C

Fig. 9. Base-emitter voltage as a function of collector current; typical values



I_C/I_B = 5
(1) T_{amb} = −55 °C
(2) T_{amb} = 25 °C
(3) T_{amb}= 100 °C

Fig. 10. Base-emitter saturation voltage as a function of collector current; typical values



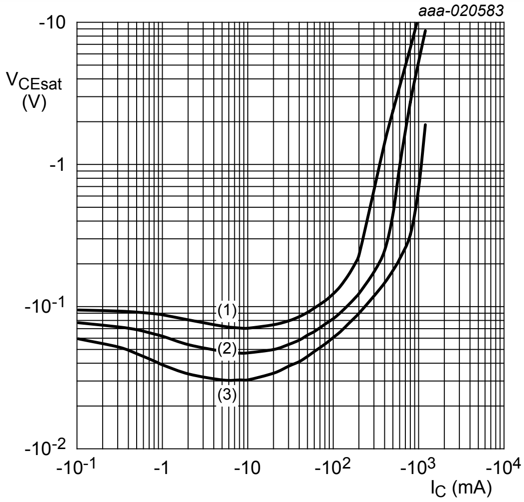
$I_C/I_B = 5$

(1) T_{amb} = 100 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −55 °C

Fig. 11. Collector-emitter saturation voltage as a function of collector current; typical values



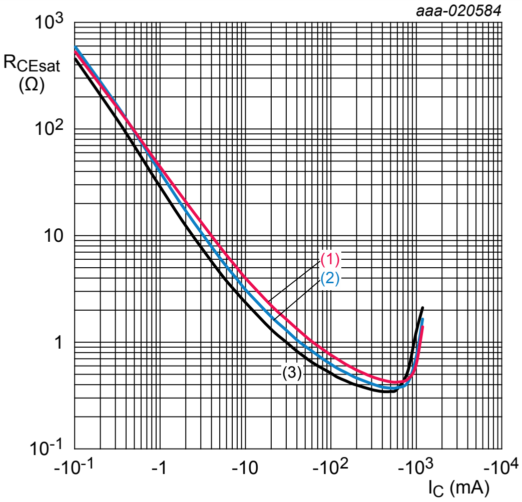
T_{amb} = 25 °C

(1) $I_C/I_B = 20$

(2) $I_C/I_B = 10$

(3) $I_C/I_B = 5$

Fig. 12. Collector-emitter saturation voltage as a function of collector current; typical values



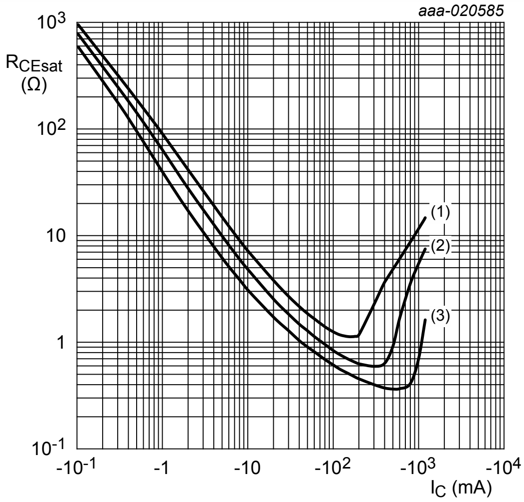
$I_C/I_B = 5$

(1) T_{amb} = 100 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −55 °C

Fig. 13. Collector-emitter saturation resistance as a function of collector current; typical values



T_{amb} = 25 °C

(1) $I_C/I_B = 20$

(2) $I_C/I_B = 10$

(3) $I_C/I_B = 5$

Fig. 14. Collector-emitter saturation resistance as a function of collector current; typical values

11. Test information

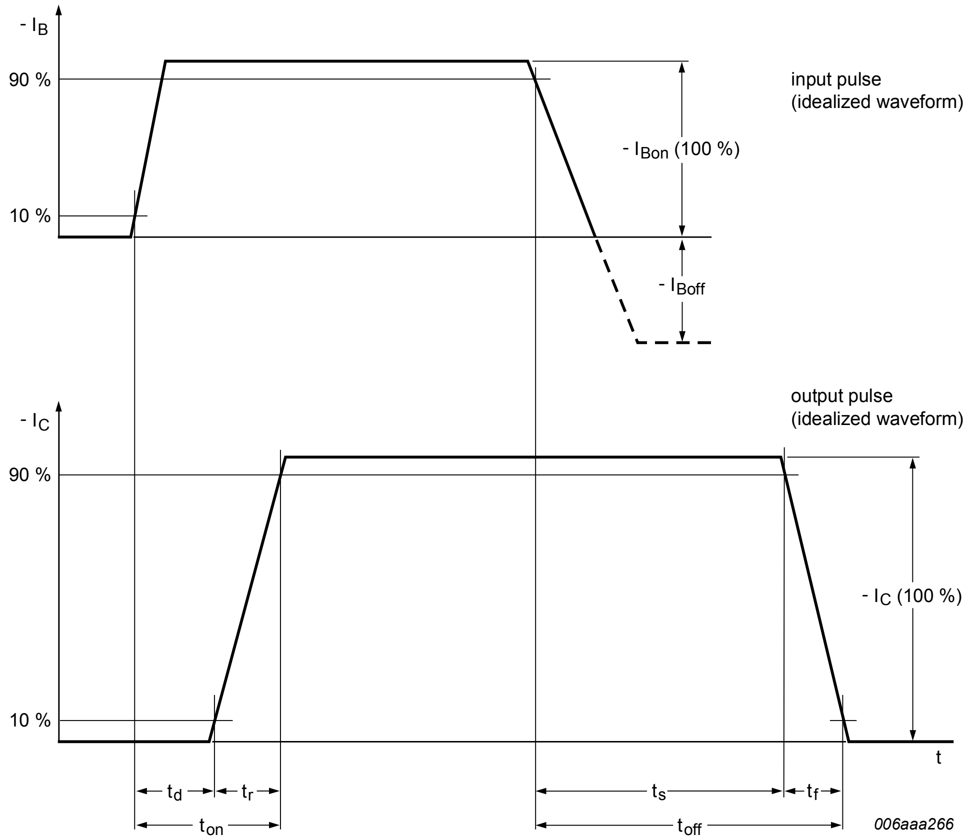


Fig. 15. BISS transistor switching time definition

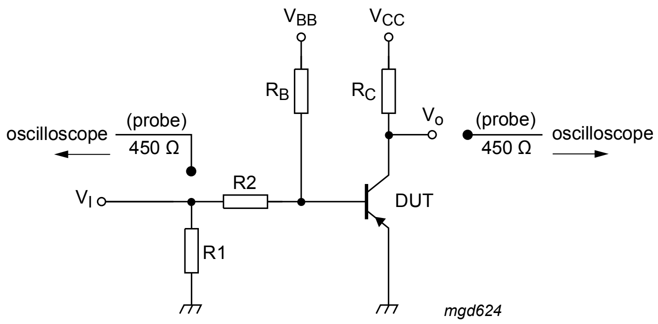


Fig. 16. Test circuit for switching times

11.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

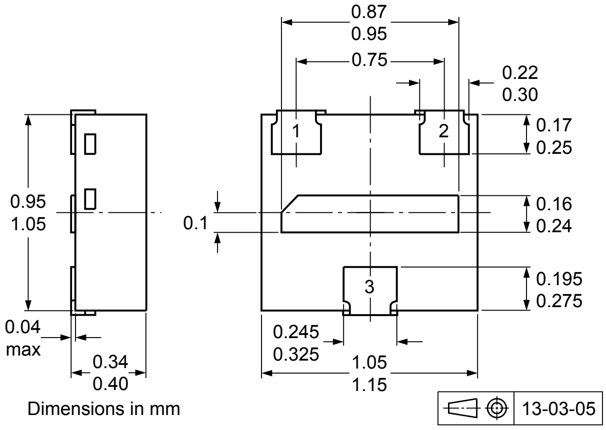


Fig. 17. Package outline DFN1010D-3 (SOT1215)

13. Soldering

Footprint information for reflow soldering of DFN1010D-3 package SOT1215

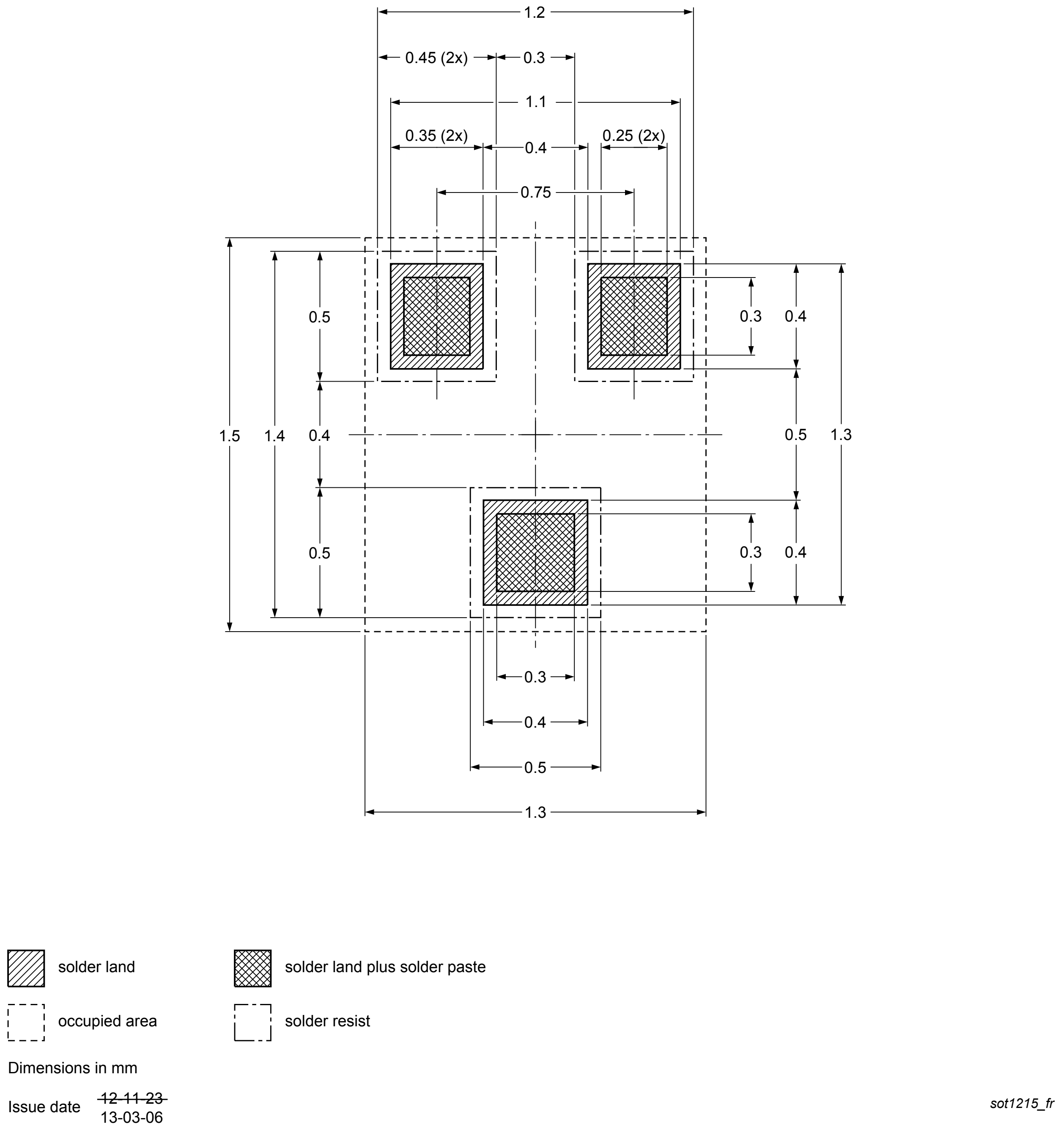


Fig. 18. Reflow soldering footprint for DFN1010D-3 (SOT1215)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PBHV9515QA v.1	20151119	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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16. Contents

Date of release: 19 November 2015