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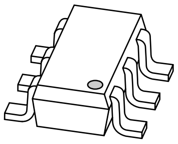


PBSS4160DS

60 V, 1 A NPN/NPN low V_{CEsat} (BISS) transistor

Rev. 04 — 11 December 2009 Product data sheet

1. Product profile

1.1 General description

NPN/NPN low V_{CEsat} Breakthrough In Small Signal (BISS) transistor pair in a SOT457 (SC-74) Surface Mounted Device (SMD) plastic package.

PNP/PNP complement: PBSS5160DS.

1.2 Features

- Low collector-emitter saturation voltage V_{CEsat}
- High collector current capability: I_C and I_{CM}
- High collector current gain (h_{FE}) at high I_C
- High efficiency due to less heat generation
- Smaller required Printed-Circuit Board (PCB) area than for conventional transistors

1.3 Applications

- Dual low power switches (e.g. motors, fans)
- Automotive applications

1.4 Quick reference data

Table 1. Quick reference data

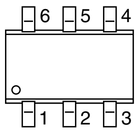
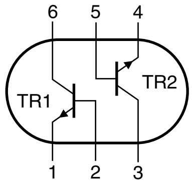
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
V_{CEO}	collector-emitter voltage	open base		-	-	60	V
I_C	collector current		[1]	-	-	1	A
I_{CM}	peak collector current	single pulse; $t_p \leq 1$ ms		-	-	2	A
R_{CEsat}	collector-emitter saturation resistance	$I_C = 1$ A; $I_B = 100$ mA	[2]	-	200	250	mΩ

[1] Device mounted on a ceramic PCB, Al_2O_3, standard footprint.

[2] Pulse test: $t_p \leq 300$ μs; $\delta \leq 0.02$.

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Symbol
1	emitter TR1		
2	base TR1		
3	collector TR2		
4	emitter TR2		
5	base TR2		
6	collector TR1		sym020

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PBSS4160DS	SC-74	plastic surface mounted package (TSOP6); 6 leads	SOT457

4. Marking

Table 4. Marking codes

Type number	Marking code
PBSS4160DS	B8

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Per transistor					
V_{CBO}	collector-base voltage	open emitter	-	80	V
V_{CEO}	collector-emitter voltage	open base	-	60	V
V_{EBO}	emitter-base voltage	open collector	-	5	V
I_C	collector current	[1]	-	0.87	A
		[2]	-	1	A
		[3]	-	1	A
I_{CM}	peak collector current	single pulse; $t_p \leq 1$ ms	-	2	A
I_B	base current		-	300	mA
I_{BM}	peak base current	single pulse; $t_p \leq 1$ ms	-	1	A

Table 5. Limiting values *...continued*

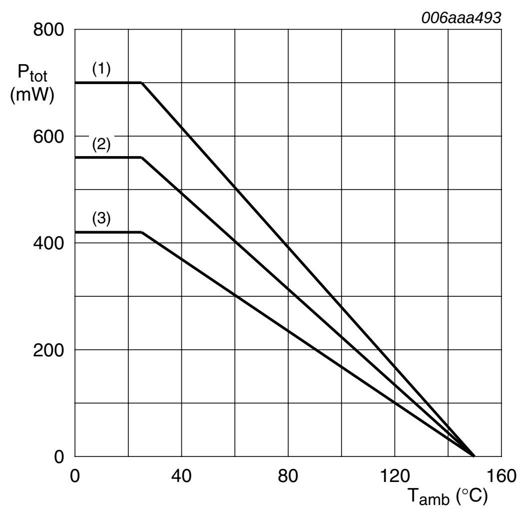
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[1]	-	290	mW
			[2]	-	370	mW
			[3]	-	450	mW
Per device						
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[1]	-	420	mW
			[2]	-	560	mW
			[3]	-	700	mW
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			−65	+150	°C
T_{stg}	storage temperature			−65	+150	°C

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm^2.

[3] Device mounted on a ceramic PCB, Al_2O_3, standard footprint.



(1) Ceramic PCB, Al_2O_3, standard footprint

(2) FR4 PCB, mounting pad for collector 1 cm^2

(3) FR4 PCB, standard footprint

Fig 1. Power derating curves

6. Thermal characteristics

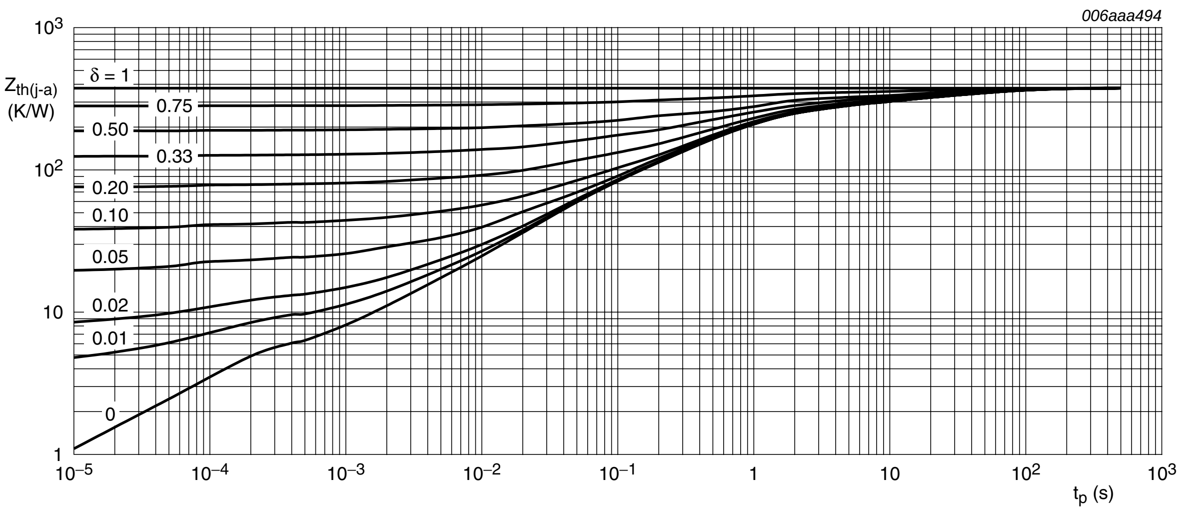
Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	431	K/W
			[2]	-	-	338	K/W
			[3]	-	-	278	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	-	105	K/W
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	298	K/W
			[2]	-	-	223	K/W
			[3]	-	-	179	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

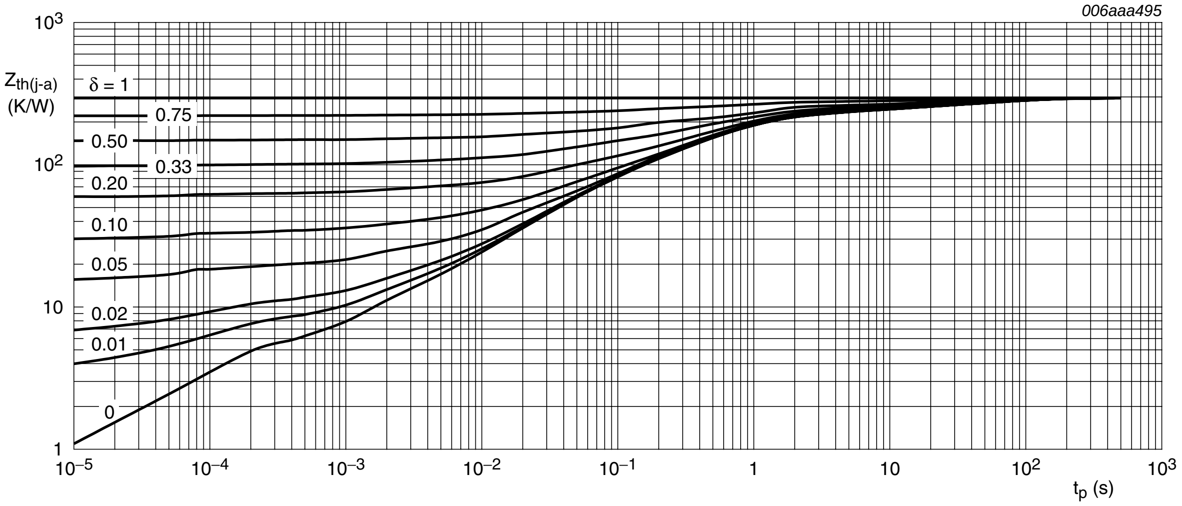
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm^2.

[3] Device mounted on a ceramic PCB, Al_2O_3, standard footprint.



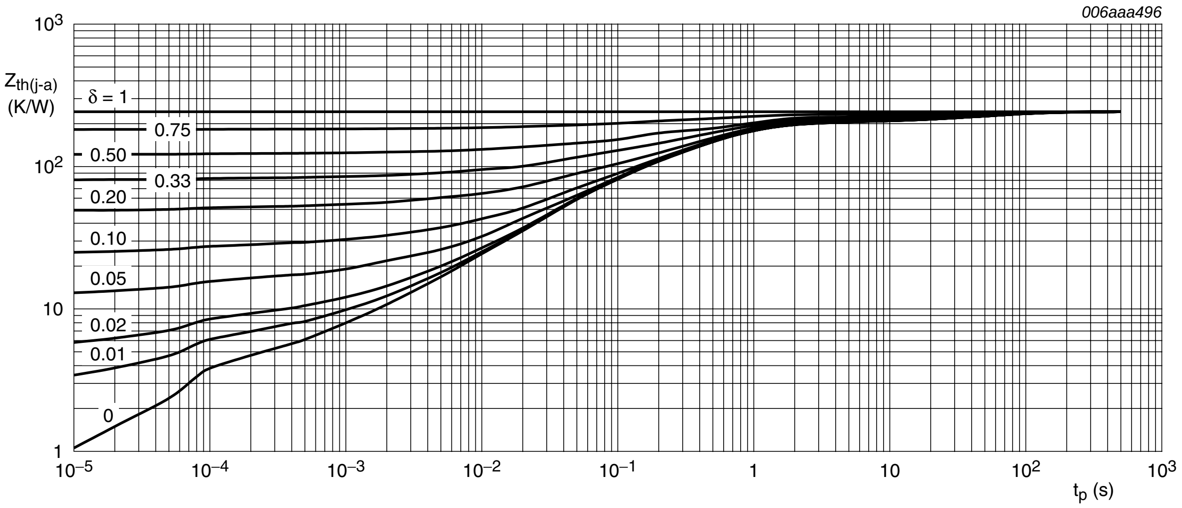
FR4 PCB, standard footprint

Fig 2. Transient thermal impedance from junction to ambient as a function of pulse time; typical values



FR4 PCB, mounting pad for collector 1 cm^2

Fig 3. Transient thermal impedance from junction to ambient as a function of pulse time; typical values



Ceramic PCB, Al_2O_3, standard footprint

Fig 4. Transient thermal impedance from junction to ambient as a function of pulse time; typical values

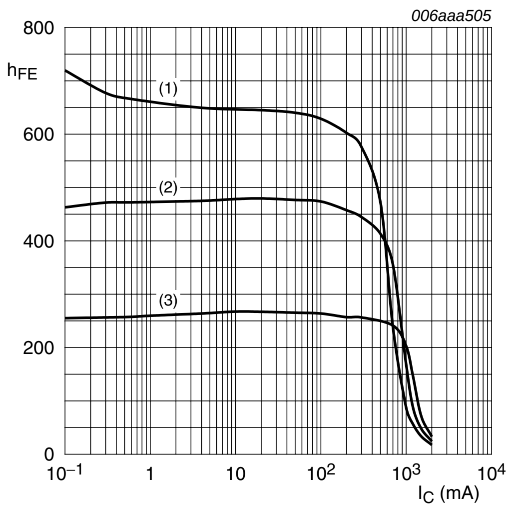
7. Characteristics

Table 7. Characteristics

T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
I_{CBO}	collector-base cut-off current	V_{CB} = 60 V; I_E = 0 A		-	-	100	nA
		V_{CB} = 60 V; I_E = 0 A; T_j = 150 °C		-	-	50	μA
I_{CES}	collector-emitter cut-off current	V_{CE} = 60 V; V_{BE} = 0 V		-	-	100	nA
I_{EBO}	emitter-base cut-off current	V_{EB} = 5 V; I_C = 0 A		-	-	100	nA
h_{FE}	DC current gain	V_{CE} = 5 V; I_C = 1 mA		250	500	-	
		V_{CE} = 5 V; I_C = 500 mA	[1]	200	420	-	
		V_{CE} = 5 V; I_C = 1 A	[1]	100	180	-	
V_{CEsat}	collector-emitter saturation voltage	I_C = 100 mA; I_B = 1 mA		-	90	110	mV
		I_C = 500 mA; I_B = 50 mA		-	115	140	mV
		I_C = 1 A; I_B = 100 mA	[1]	-	200	250	mV
R_{CEsat}	collector-emitter saturation resistance	I_C = 1 A; I_B = 100 mA	[1]	-	200	250	mΩ
V_{BEsat}	base-emitter saturation voltage	I_C = 1 A; I_B = 50 mA	[1]	-	0.95	1.1	V
V_{BEon}	base-emitter turn-on voltage	V_{CE} = 5 V; I_C = 1 A	[1]	-	0.82	0.9	V
t_d	delay time	I_C = 0.5 A; I_{Bon} = 25 mA; I_{Boff} = −25 mA		-	11	-	ns
t_r	rise time			-	78	-	ns
t_{on}	turn-on time			-	90	-	ns
t_s	storage time			-	340	-	ns
t_f	fall time			-	160	-	ns
t_{off}	turn-off time			-	500	-	ns
f_T	transition frequency	V_{CE} = 10 V; I_C = 50 mA; f = 100 MHz		150	220	-	MHz
C_c	collector capacitance	V_{CB} = 10 V; I_E = i_e = 0 A; f = 1 MHz		-	5.5	10	pF

[1] Pulse test: $t_p \leq 300$ μs; $\delta \leq 0.02$.



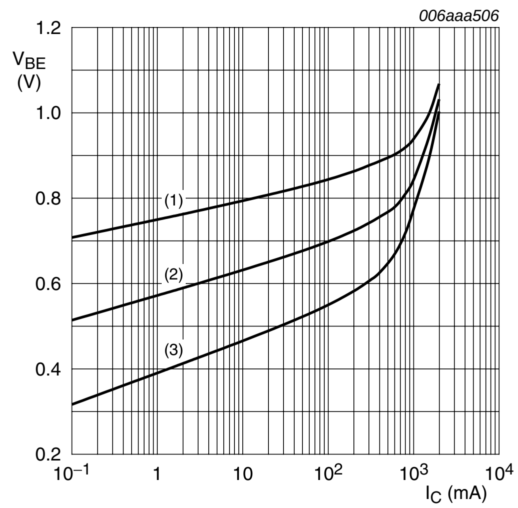
V_{CE} = 5 V

(1) T_{amb} = 100 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −55 °C

Fig 5. DC current gain as a function of collector current; typical values



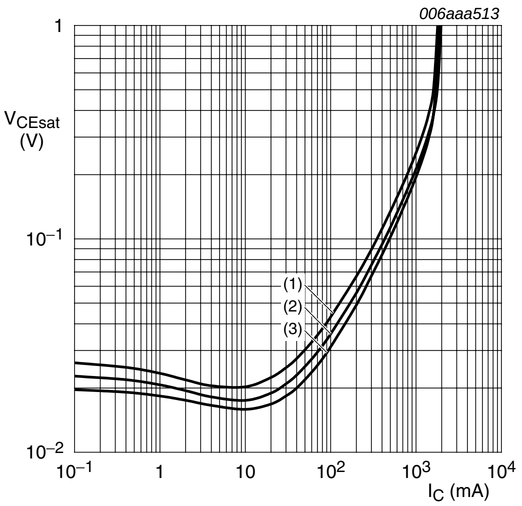
V_{CE} = 5 V

(1) T_{amb} = −55 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = 100 °C

Fig 6. Base-emitter voltage as a function of collector current; typical values



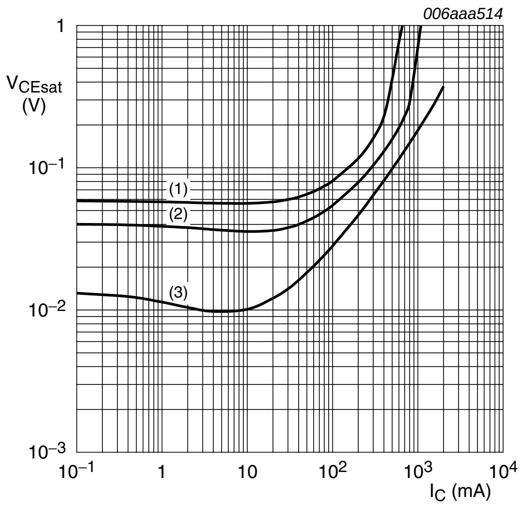
I_C/I_B = 20

(1) T_{amb} = 100 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −55 °C

Fig 7. Collector-emitter saturation voltage as a function of collector current; typical values



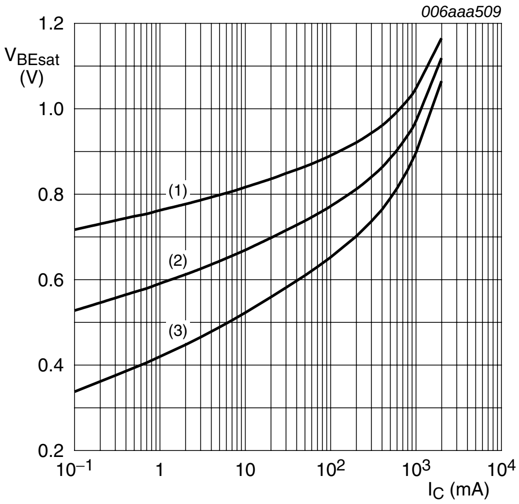
T_{amb} = 25 °C

(1) I_C/I_B = 100

(2) I_C/I_B = 50

(3) I_C/I_B = 10

Fig 8. Collector-emitter saturation voltage as a function of collector current; typical values



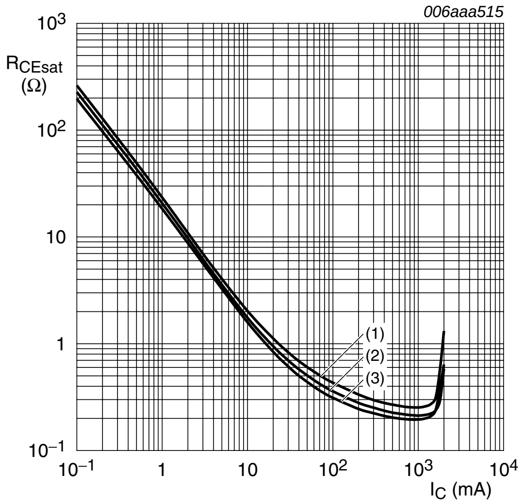
$I_C/I_B = 20$

(1) $T_{amb} = -55$ °C

(2) $T_{amb} = 25$ °C

(3) $T_{amb} = 100$ °C

Fig 9. Base-emitter saturation voltage as a function of collector current; typical values



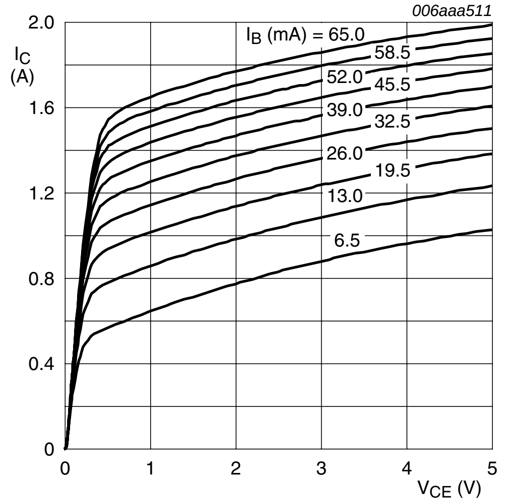
$I_C/I_B = 20$

(1) $T_{amb} = 100$ °C

(2) $T_{amb} = 25$ °C

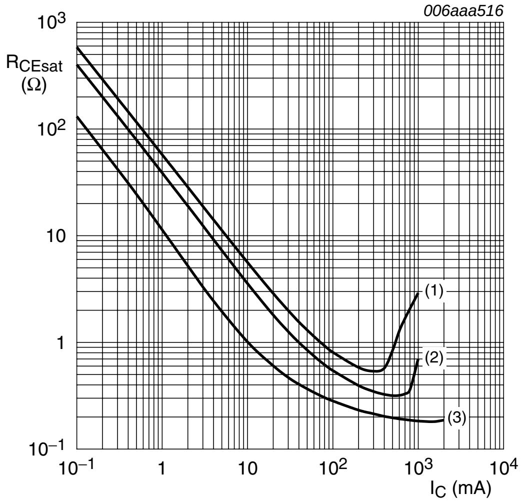
(3) $T_{amb} = -55$ °C

Fig 10. Collector-emitter saturation resistance as a function of collector current; typical values



$T_{amb} = 25$ °C

Fig 11. Collector current as a function of collector-emitter voltage; typical values



$T_{amb} = 25$ °C

(1) $I_C/I_B = 100$

(2) $I_C/I_B = 50$

(3) $I_C/I_B = 10$

Fig 12. Collector-emitter saturation resistance as a function of collector current; typical values

8. Test information

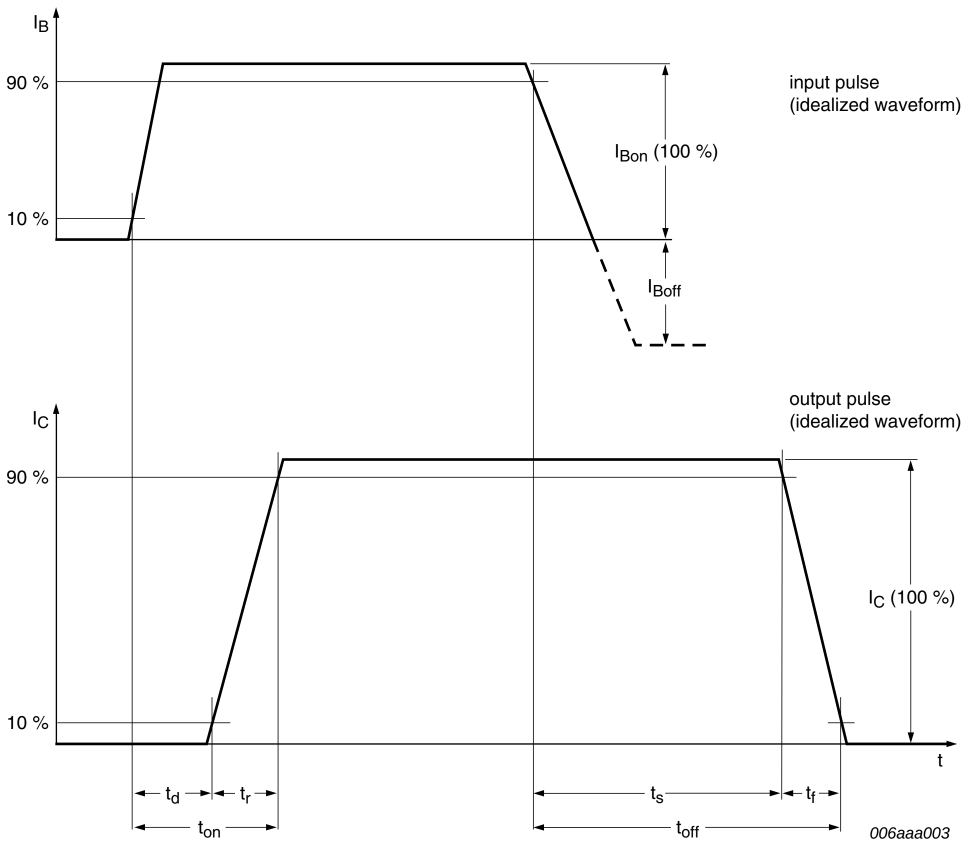
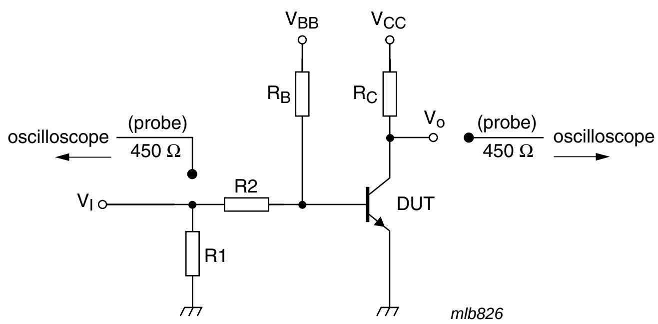


Fig 13. BISS transistor switching time definition



I_C = 0.5 A; I_{Bon} = 25 mA; I_{Boff} = −25 mA; R1 = open; R2 = 100 Ω; R_B = 300 Ω; R_C = 20 Ω

Fig 14. Test circuit for switching times

9. Package outline

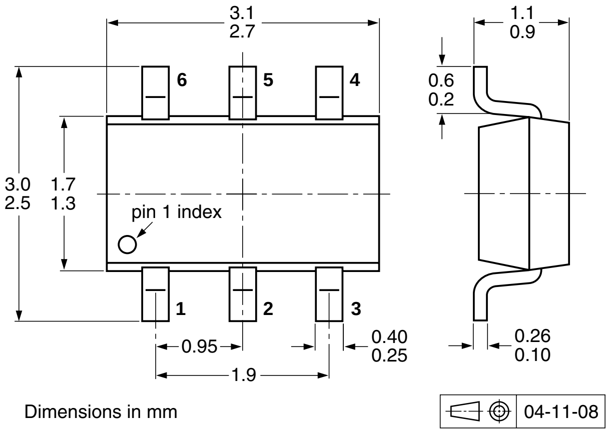


Fig 15. Package outline SOT457 (SC-74)

10. Packing information

Table 8. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code.[1]

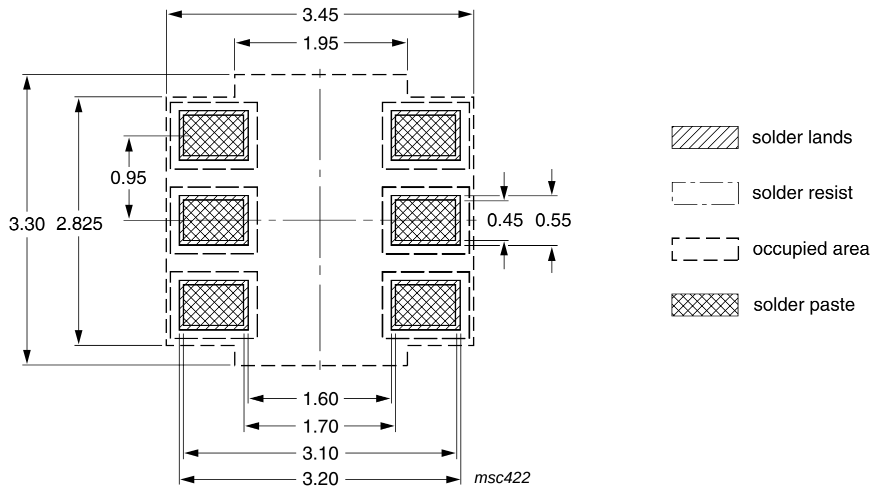
Type number	Package	Description	Packing quantity	
			3000	**10000**
PBSS4160DS	SOT457	4 mm pitch, 8 mm tape and reel; T1 [2]	-115	-135
		4 mm pitch, 8 mm tape and reel; T2 [3]	-125	-165

[1] For further information and the availability of packing methods, see Section 14.

[2] T1: normal taping

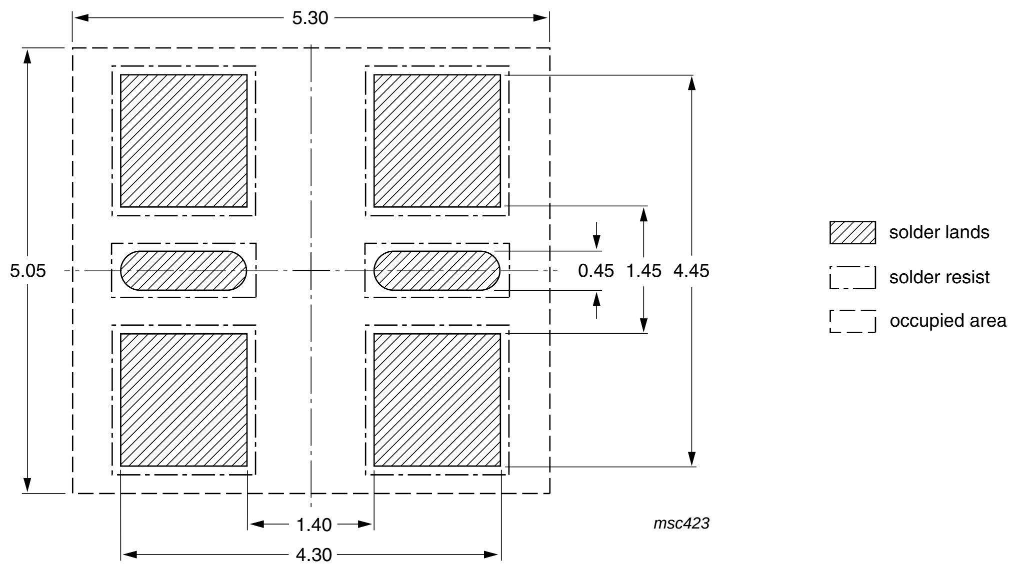
[3] T2: reverse taping

11. Soldering



Dimensions in mm

Fig 16. Reflow soldering footprint



Dimensions in mm

Fig 17. Wave soldering footprint

12. Revision history

Table 9. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PBSS4160DS_4	20091211	Product data sheet	-	PBSS4160DS_3
Modifications:	• This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content. • Figure 17 "Wave soldering footprint": updated			
PBSS4160DS_3	20060209	Product data sheet	-	PBSS4160DS_2
PBSS4160DS_2	20050627	Product data sheet	-	PBSS4160DS_1
PBSS4160DS_1	20040426	Objective data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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15. Contents

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