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Kind regards,

Team Nexperia



PBSS4220V

20 V, 2 A NPN low V_{CEsat} (BISS) transistor Rev. 02 — 11 December 2009

Product data sheet

Product profile 1.

1.1 General description

NPN low V_{CEsat} Breakthrough In Small Signal (BISS) transistor in a SOT666 Surface Mounted Device (SMD) plastic package.

PNP complement: PBSS5220V.

1.2 Features

- Low collector-emitter saturation voltage V_{CEsat}
- High collector current capability: I_C and I_{CM}
- High collector current gain (h_{FE}) at high I_C
- High efficiency due to less heat generation
- Smaller required Printed-Circuit Board (PCB) area than for conventional transistors

1.3 Applications

- DC-to-DC conversion
- MOSFET gate driving
- Motor control
- Charging circuits
- Low power switches (e.g. motors, fans)
- Portable applications

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{CEO}	collector-emitter voltage	open base	-	-	20	V
I _C	collector current		-	-	2	Α
I _{CM}	peak collector current	$t_p \leq 300~\mu s$	-	-	4	Α
R _{CEsat}	collector-emitter saturation resistance	$I_C = 1 A;$ $I_B = 100 \text{ mA}$	[1] -	140	175	mΩ

^[1] Pulse test: $t_p \le 300~\mu s;~\delta \le 0.02.$



20 V, 2 A NPN low V_{CEsat} (BISS) transistor

2. **Pinning information**

Table 2. **Pinning**

	3	
Pin	Description	Simplified outline Symbol
1	collector	
2	collector	6 5 4 1, 2, 5, 6
3	base	3 —
4	emitter	
5	collector	4 1 2 2 sym014
6	collector	1 2 3 symu14

3. **Ordering information**

Table 3. **Ordering information**

Type number	Package		
	Name	Description	Version
PBSS4220V	-	plastic surface mounted package; 6 leads	SOT666

Marking 4.

Table 4. Marking codes

Type number	Marking code
PBSS4220V	N6

Limiting values 5.

Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CBO}	collector-base voltage	open emitter	-	20	V
V_{CEO}	collector-emitter voltage	open base	-	20	V
V_{EBO}	emitter-base voltage	open collector	-	5	V
I _C	collector current		-	2	Α
I _{CM}	peak collector current	$t_p \leq 300~\mu s$	-	4	Α
I _B	base current		-	0.3	Α
I _{BM}	peak base current	$t_p \leq 300~\mu s$	-	0.6	Α
P _{tot}	total power dissipation	$T_{amb} \le 25 ^{\circ}C$	<u>[1][4]</u> _	0.3	W
			[2][4]	0.5	W
			[3][4]	0.9	W
T _i	junction temperature		-	150	°C

20 V, 2 A NPN low V_{CEsat} (BISS) transistor

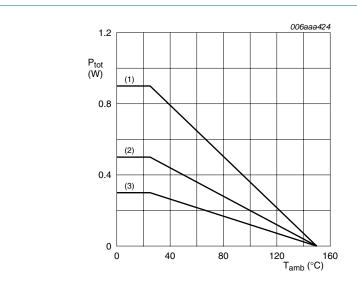
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Table 5. Limiting values ...continued

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
T _{amb}	ambient temperature		-65	+150	°C
T _{stg}	storage temperature		-65	+150	°C

- Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint. [1]
- Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm². [2]
- Device mounted on a ceramic PCB, Al₂O₃, standard footprint. [3]
- Reflow soldering is the only recommended soldering method.



- (1) Ceramic PCB, Al₂O₃, standard footprint
- (2) FR4 PCB, mounting pad for collector 1 cm²
- (3) FR4 PCB, standard footprint

Fig 1. **Power derating curves**

20 V, 2 A NPN low V_{CEsat} (BISS) transistor

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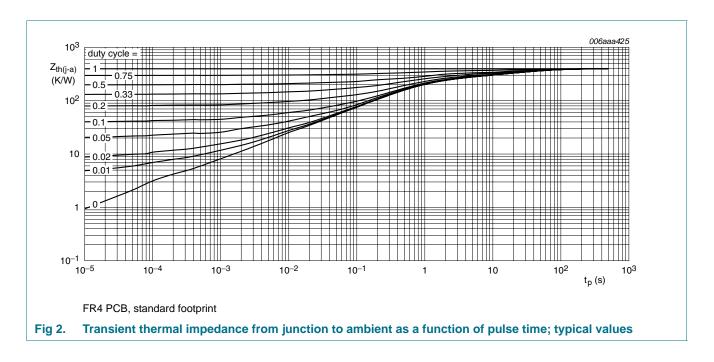
Thermal characteristics 6.

Product data sheet

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
$R_{th(j-a)}$	thermal resistance from	tion to ambient	[1][4]	-	-	410	K/W
junction to ambient	junction to ambient		[2][4]	-	-	250	K/W
			[3][4]	-	-	140	K/W
R _{th(j-sp)}	thermal resistance from junction to solder point			-	-	80	K/W

- Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm². [2]
- Device mounted on a ceramic PCB, Al₂O₃, standard footprint.
- Reflow soldering is the only recommended soldering method.



20 V, 2 A NPN low V_{CEsat} (BISS) transistor

7. **Characteristics**

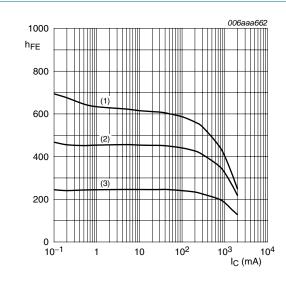
Characteristics

 $T_{amb} = 25$ °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Тур	Max	Uni
I _{CBO}	collector-base cut-off	$V_{CB} = 20 \text{ V}; I_{E} = 0 \text{ A}$		-	-	0.1	μΑ
	current	$V_{CB} = 20 \text{ V}; I_E = 0 \text{ A};$ $T_j = 150 ^{\circ}\text{C}$		-	-	50	μА
I _{CES}	collector-emitter cut-off current	$V_{CE} = 20 \text{ V}; V_{BE} = 0 \text{ V}$		-	-	0.1	μΑ
I _{EBO}	emitter-base cut-off current	$V_{EB} = 5 \text{ V}; I_{C} = 0 \text{ A}$		-	-	0.1	μА
h _{FE} DC current gain		$V_{CE} = 2 \text{ V}; I_{C} = 1 \text{ mA}$		220	480	-	
		$V_{CE} = 2 \text{ V}; I_{C} = 100 \text{ mA}$		220	440	-	
		$V_{CE} = 2 \text{ V}; I_{C} = 500 \text{ mA}$	<u>[1]</u>	220	410	-	
		V _{CE} = 2 V; I _C = 1 A	<u>[1]</u>	200	360	-	
		V _{CE} = 2 V; I _C = 2 A	<u>[1]</u>	120	220	-	
V_{CEsat}	collector-emitter	$I_C = 100 \text{ mA}; I_B = 1 \text{ mA}$		-	35	55	mV
	saturation voltage	$I_C = 500 \text{ mA}; I_B = 50 \text{ mA}$	<u>[1]</u>	-	70	95	mV
		$I_C = 1 A$; $I_B = 50 \text{ mA}$	<u>[1]</u>	-	145	180	mV
		$I_C = 1 A$; $I_B = 100 \text{ mA}$	<u>[1]</u>	-	140	175	mV
		$I_C = 2 \text{ A}; I_B = 100 \text{ mA}$	<u>[1]</u>	-	275	355	mV
		$I_C = 2 \text{ A}; I_B = 200 \text{ mA}$	<u>[1]</u>	-	270	350	mV
R _{CEsat}	collector-emitter saturation resistance	$I_C = 1 A; I_B = 100 \text{ mA}$	[1]	-	140	175	mΩ
V _{BEsat}	base-emitter saturation	$I_C = 1 A$; $I_B = 50 \text{ mA}$	<u>[1]</u>	-	0.95	1.1	V
	voltage	$I_C = 1 A$; $I_B = 100 \text{ mA}$	<u>[1]</u>	-	1	1.2	V
V_{BEon}	base-emitter turn-on voltage	$V_{CE} = 5 \text{ V}; I_{C} = 1 \text{ A}$		-	0.8	1.1	V
t _d	delay time	$I_C = 1 A$; $I_{Bon} = 50 \text{ mA}$;		-	9	-	ns
t _r	rise time	$I_{Boff} = -50 \text{ mA}$		-	29	-	ns
t _{on}	turn-on time			-	38	-	ns
ts	storage time			-	200	-	ns
t _f	fall time			-	40	-	ns
t _{off}	turn-off time			-	240	-	ns
f _T	transition frequency	$V_{CE} = 10 \text{ V}; I_{C} = 50 \text{ mA};$ f = 100 MHz		-	210	-	МН
C _c	collector capacitance	$V_{CB} = 10 \text{ V}; I_E = i_e = 0 \text{ A};$ f = 1 MHz		-	11	-	pF

^[1] Pulse test: $t_p \leq 300~\mu s;~\delta \leq 0.02.$

20 V, 2 A NPN low V_{CEsat} (BISS) transistor



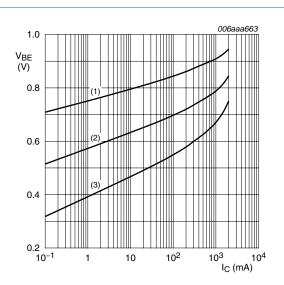
$$V_{CE} = 2 V$$

(1)
$$T_{amb} = 100 \, ^{\circ}C$$

(2)
$$T_{amb} = 25 \, ^{\circ}C$$

(3)
$$T_{amb} = -55 \, ^{\circ}C$$

Fig 3. DC current gain as a function of collector current; typical values



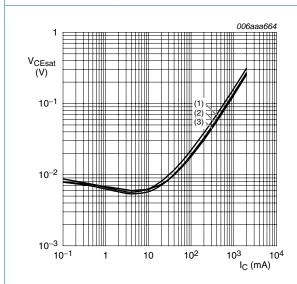
$$V_{CE} = 5 V$$

(1)
$$T_{amb} = -55 \, ^{\circ}C$$

(2)
$$T_{amb} = 25 \, ^{\circ}C$$

(3)
$$T_{amb} = 100 \, ^{\circ}C$$

Fig 4. Base-emitter voltage as a function of collector current; typical values



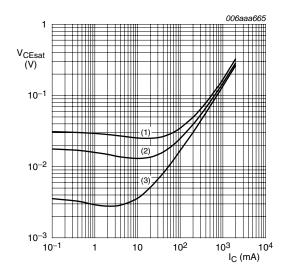
$$I_{\rm C}/I_{\rm B}=20$$

(1)
$$T_{amb} = 100 \, ^{\circ}C$$

(2)
$$T_{amb} = 25 \, ^{\circ}C$$

(3)
$$T_{amb} = -55 \, ^{\circ}C$$

Fig 5. Collector-emitter saturation voltage as a function of collector current; typical values



$$T_{amb} = 25 \, ^{\circ}C$$

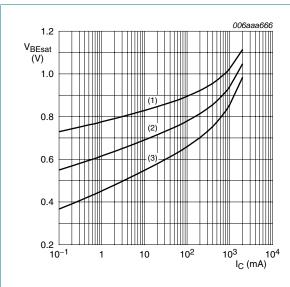
(1)
$$I_C/I_B = 100$$

(2)
$$I_C/I_B = 50$$

(3)
$$I_C/I_B = 10$$

Fig 6. Collector-emitter saturation voltage as a function of collector current; typical values

20 V, 2 A NPN low V_{CEsat} (BISS) transistor



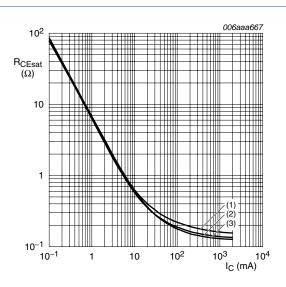
$$I_{\rm C}/I_{\rm B} = 20$$

(1)
$$T_{amb} = -55 \, ^{\circ}C$$

(2)
$$T_{amb} = 25 \, ^{\circ}C$$

(3)
$$T_{amb} = 100 \, ^{\circ}C$$

Fig 7. Base-emitter saturation voltage as a function of collector current; typical values



$$I_{\rm C}/I_{\rm B} = 20$$

(1)
$$T_{amb} = 100 \, ^{\circ}C$$

(2)
$$T_{amb} = 25 \, ^{\circ}C$$

(3)
$$T_{amb} = -55 \, ^{\circ}C$$

Fig 8. Collector-emitter saturation resistance as a function of collector current; typical values

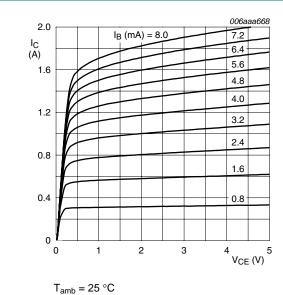
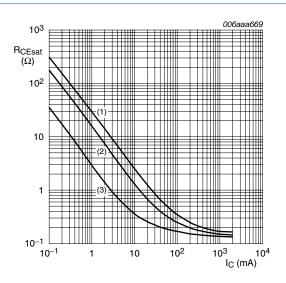


Fig 9. Collector current as a function of collector-emitter voltage; typical values



$$T_{amb} = 25 \, ^{\circ}C$$

(1)
$$I_C/I_B = 100$$

(2)
$$I_C/I_B = 50$$

(3)
$$I_C/I_B = 10$$

Fig 10. Collector-emitter saturation resistance as a function of collector current; typical values

20 V, 2 A NPN low V_{CEsat} (BISS) transistor

8. Test information

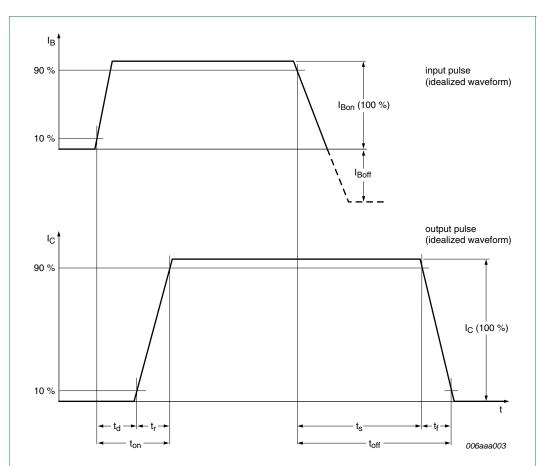
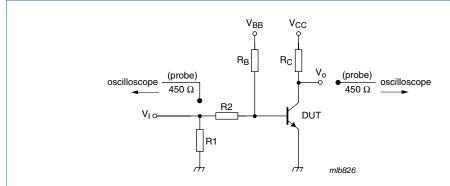


Fig 11. BISS transistor switching time definition

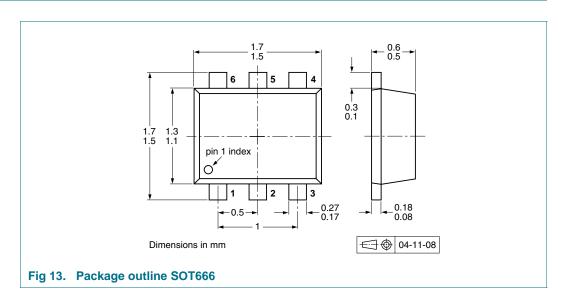


 I_C = 1 A; I_{Bon} = 50 mA; I_{Boff} = –50 mA; R1 = open; R2 = 45 Ω ; R_B = 145 Ω ; R_C = 10 Ω

Fig 12. Test circuit for switching times

20 V, 2 A NPN low V_{CEsat} (BISS) transistor

9. Package outline



10. Packing information

Table 8. Packing methods

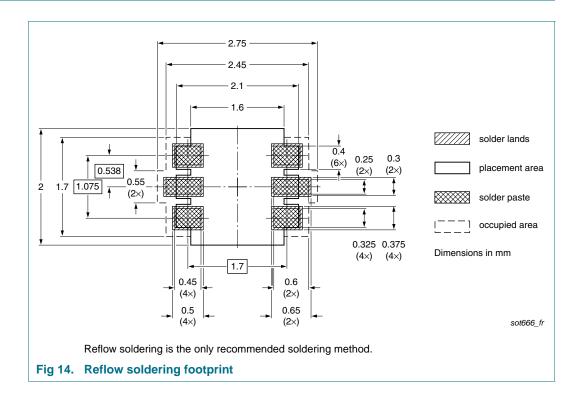
The indicated -xxx are the last three digits of the 12NC ordering code.[1]

Type number	Package	Description	Packing 6	quantity
			4000	8000
PBSS4220V	SOT666	2 mm pitch, 8 mm tape and reel	-	-315
		4 mm pitch, 8 mm tape and reel	-115	-

^[1] For further information and the availability of packing methods, see Section 14.

20 V, 2 A NPN low V_{CEsat} (BISS) transistor

11. Soldering



20 V, 2 A NPN low V_{CEsat} (BISS) transistor

12. Revision history

Table 9. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PBSS4220V_2	20091211	Product data sheet	-	PBSS4220V_1
Modifications:	 This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content. 			
	 Figure 14 "R 	eflow soldering footprint": u	ıpdated	
PBSS4220V_1	20060206	Product data sheet	-	-

20 V, 2 A NPN low V_{CEsat} (BISS) transistor

13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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