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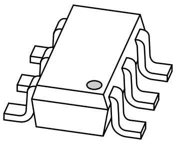


# PBSS5160DS

## 60 V, 1 A PNP/PNP low $V_{CEsat}$ (BISS) transistor

Rev. 03 — 9 October 2008 **Product data sheet**

## 1. Product profile

### 1.1 General description

PNP/PNP low $V_{CEsat}$ Breakthrough In Small Signal (BISS) transistor pair in a small SOT457 (SC-74) Surface-Mounted Device (SMD) plastic package.

NPN complement: PBSS4160DS.

### 1.2 Features

- Low collector-emitter saturation voltage $V_{CEsat}$
- High collector current capability $I_C$ and $I_{CM}$
- High collector current gain ($h_{FE}$) at high $I_C$
- High efficiency due to less heat generation
- Smaller required Printed-Circuit Board (PCB) area than for conventional transistors

### 1.3 Applications

- Dual low power switches (e.g. motors, fans)
- Automotive applications

### 1.4 Quick reference data

**Table 1. Quick reference data**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{CEO}$ | collector-emitter voltage | open base | | - | - | –60 | V |
| $I_C$ | collector current | | [1] | - | - | –1 | A |
| $I_{CM}$ | peak collector current | single pulse; $t_p \leq 1$ ms | | - | - | –2 | A |
| $R_{CEsat}$ | collector-emitter saturation resistance | $I_C = -1$ A; $I_B = -100$ mA | [2] | - | 250 | 330 | mΩ |

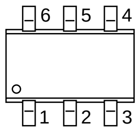
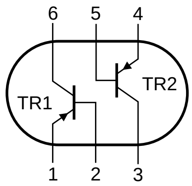
[1] Device mounted on a ceramic PCB, $Al_2O_3$, standard footprint.

[2] Pulse test: $t_p \leq 300$ µs; $\delta \leq 0.02$.

founded by Philips

## 2. Pinning information

**Table 2. Pinning**

| Pin | Description | Simplified outline | Graphic symbol |
|---|---|---|---|
| 1 | emitter TR1 |  |  sym018 |
| 2 | base TR1 | | |
| 3 | collector TR2 | | |
| 4 | emitter TR2 | | |
| 5 | base TR2 | | |
| 6 | collector TR1 | | |

## 3. Ordering information

**Table 3. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| PBSS5160DS | SC-74 | plastic surface-mounted package (TSOP6); 6 leads | SOT457 |

## 4. Marking

**Table 4. Marking codes**

| Type number | Marking code |
|---|---|
| PBSS5160DS | A5 |

## 5. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| **Per transistor** | | | | | | |
| $V_{CBO}$ | collector-base voltage | open emitter | | - | –80 | V |
| $V_{CEO}$ | collector-emitter voltage | open base | | - | –60 | V |
| $V_{EBO}$ | emitter-base voltage | open collector | | - | –5 | V |
| $I_C$ | collector current | | [1] | - | –0.77 | A |
| | | | [2] | - | –0.9 | A |
| | | | [3] | - | –1 | A |
| $I_{CM}$ | peak collector current | single pulse; $t_p \leq 1$ ms | | - | –2 | A |
| $I_B$ | base current | | | - | –300 | mA |
| $I_{BM}$ | peak base current | single pulse; $t_p \leq 1$ ms | | - | –1 | A |

**Table 5. Limiting values** *...continued*

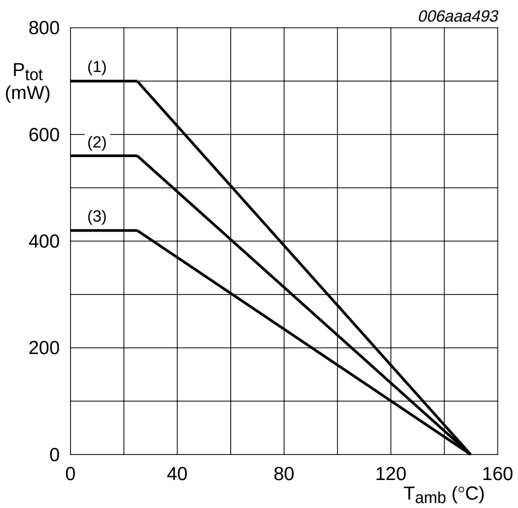
*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $P_{tot}$ | total power dissipation | $T_{amb} \leq 25$ °C | [1] | - | 290 | mW |
| | | | [2] | - | 370 | mW |
| | | | [3] | - | 450 | mW |
| **Per device** | | | | | | |
| $P_{tot}$ | total power dissipation | $T_{amb} \leq 25$ °C | [1] | - | 420 | mW |
| | | | [2] | - | 560 | mW |
| | | | [3] | - | 700 | mW |
| $T_j$ | junction temperature | | | - | 150 | °C |
| $T_{amb}$ | ambient temperature | | | –65 | +150 | °C |
| $T_{stg}$ | storage temperature | | | –65 | +150 | °C |

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 $cm^2$.

[3] Device mounted on a ceramic PCB, $Al_2O_3$, standard footprint.




(1) Ceramic PCB, $Al_2O_3$, standard footprint

(2) FR4 PCB, mounting pad for collector 1 $cm^2$

(3) FR4 PCB, standard footprint

**Fig 1. Power derating curves**

# 6. Thermal characteristics

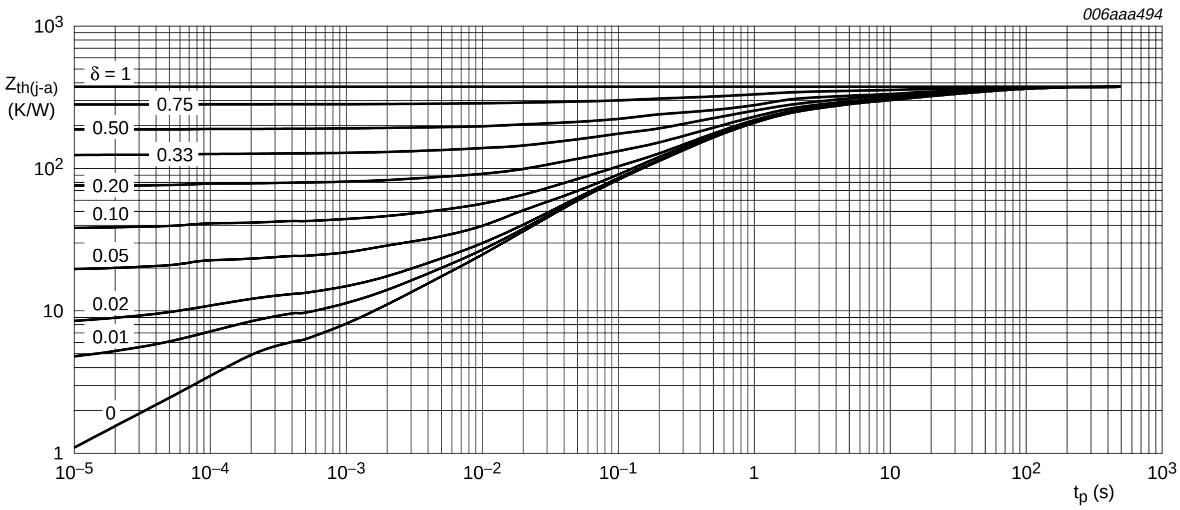
**Table 6. Thermal characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Per transistor** | | | | | | | |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | [1] | - | - | 431 | K/W |
| | | | [2] | - | - | 338 | K/W |
| | | | [3] | - | - | 278 | K/W |
| $R_{th(j-sp)}$ | thermal resistance from junction to solder point | | | - | - | 105 | K/W |
| **Per device** | | | | | | | |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | [1] | - | - | 298 | K/W |
| | | | [2] | - | - | 223 | K/W |
| | | | [3] | - | - | 179 | K/W |

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

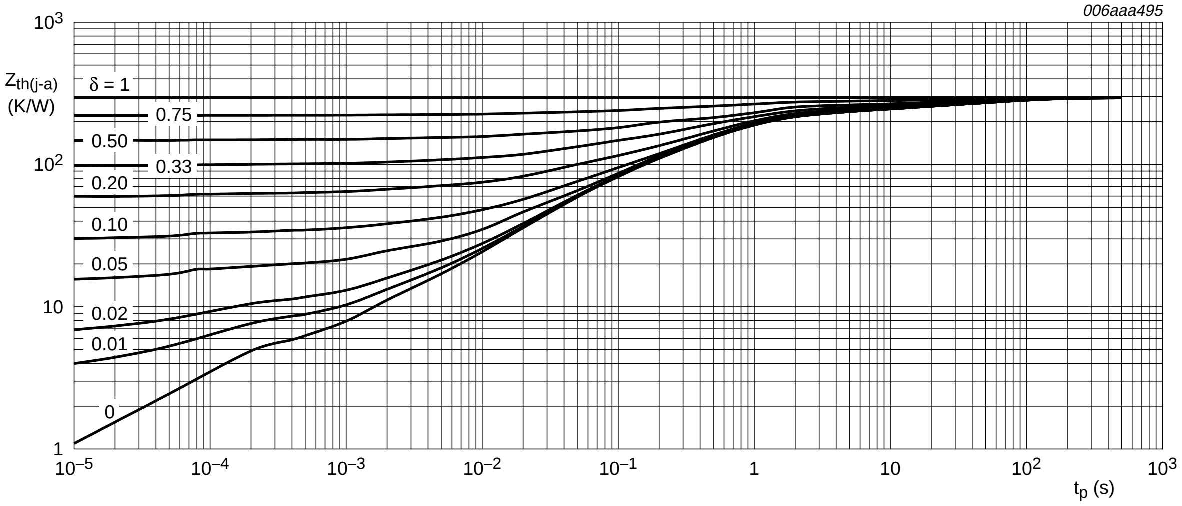
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 $cm^2$.

[3] Device mounted on a ceramic PCB, $Al_2O_3$, standard footprint.



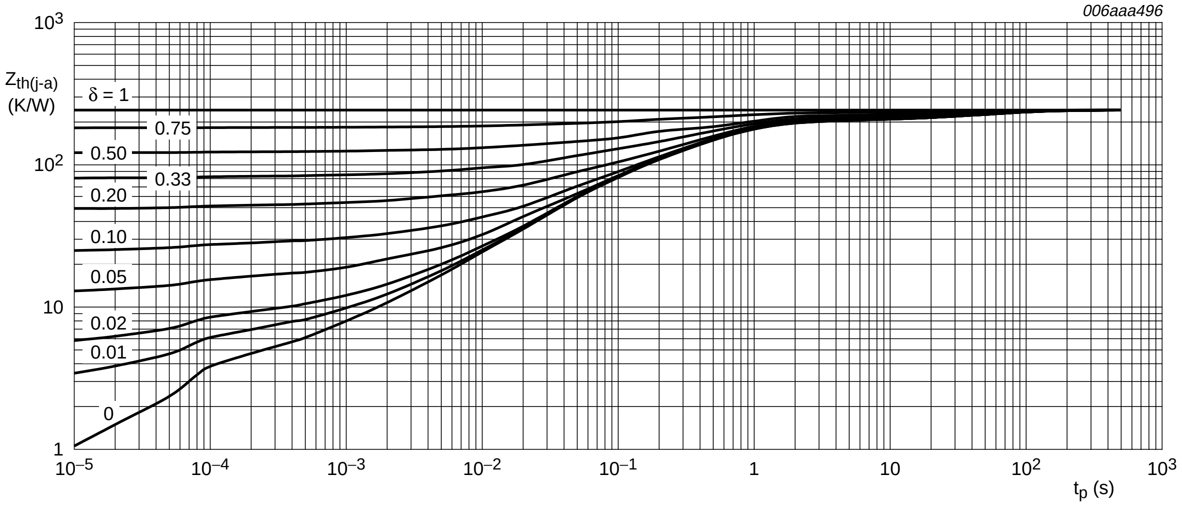

FR4 PCB, standard footprint

**Fig 2. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values**




FR4 PCB, mounting pad for collector 1 $cm^2$

**Fig 3. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values**




Ceramic PCB, $Al_2O_3$, standard footprint

**Fig 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values**

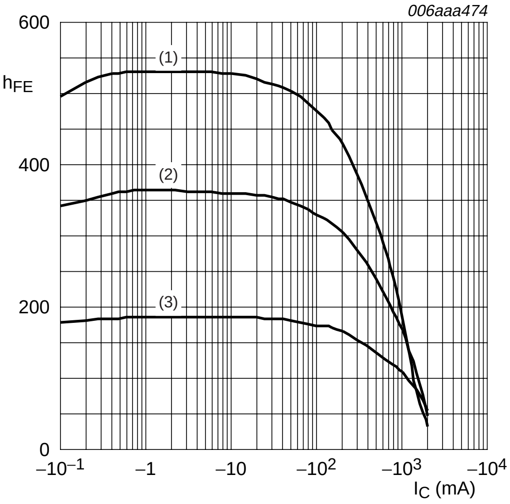
# 7. Characteristics

**Table 7. Characteristics**

*$T_{amb}$ = 25 °C unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Per transistor** | | | | | | | |
| $I_{CBO}$ | collector-base cut-off current | $V_{CB}$ = –60 V; $I_E$ = 0 A | | - | - | –100 | nA |
| | | $V_{CB}$ = –60 V; $I_E$ = 0 A; $T_j$ = 150 °C | | - | - | –50 | µA |
| $I_{CES}$ | collector-emitter cut-off current | $V_{CE}$ = –60 V; $V_{BE}$ = 0 V | | - | - | –100 | nA |
| $I_{EBO}$ | emitter-base cut-off current | $V_{EB}$ = –5 V; $I_C$ = 0 A | | - | - | –100 | nA |
| $h_{FE}$ | DC current gain | $V_{CE}$ = –5 V; $I_C$ = –1 mA | | 200 | 350 | - | |
| | | $V_{CE}$ = –5 V; $I_C$ = –500 mA | [1] | 150 | 250 | - | |
| | | $V_{CE}$ = –5 V; $I_C$ = –1 A | [1] | 100 | 160 | - | |
| $V_{CEsat}$ | collector-emitter saturation voltage | $I_C$ = –100 mA; $I_B$ = –1 mA | | - | –110 | –165 | mV |
| | | $I_C$ = –500 mA; $I_B$ = –50 mA | | - | –120 | –175 | mV |
| | | $I_C$ = –1 A; $I_B$ = –100 mA | [1] | - | –250 | –330 | mV |
| $V_{BEsat}$ | base-emitter saturation voltage | $I_C$ = –1 A; $I_B$ = –50 mA | [1] | - | –0.95 | –1.1 | V |
| $R_{CEsat}$ | collector-emitter saturation resistance | $I_C$ = –1 A; $I_B$ = –100 mA | [1] | - | 250 | 330 | mΩ |
| $V_{BEon}$ | base-emitter turn-on voltage | $I_C$ = –1 A; $V_{CE}$ = –5 V | [1] | - | –0.82 | –0.9 | V |
| $t_d$ | delay time | $I_C$ = –0.5 A; $I_{Bon}$ = –25 mA; $I_{Boff}$ = 25 mA | | - | 11 | - | ns |
| $t_r$ | rise time | | | - | 30 | - | ns |
| $t_{on}$ | turn-on time | | | - | 41 | - | ns |
| $t_s$ | storage time | | | - | 205 | - | ns |
| $t_f$ | fall time | | | - | 55 | - | ns |
| $t_{off}$ | turn-off time | | | - | 260 | - | ns |
| $f_T$ | transition frequency | $V_{CE}$ = –10 V; $I_C$ = –50 mA; f = 100 MHz | | 150 | 185 | - | MHz |
| $C_c$ | collector capacitance | $V_{CB}$ = –10 V; $I_E$ = $i_e$ = 0 A; f = 1 MHz | | - | 9 | 15 | pF |

[1] Pulse test: $t_p \leq 300$ µs; $\delta \leq 0.02$.



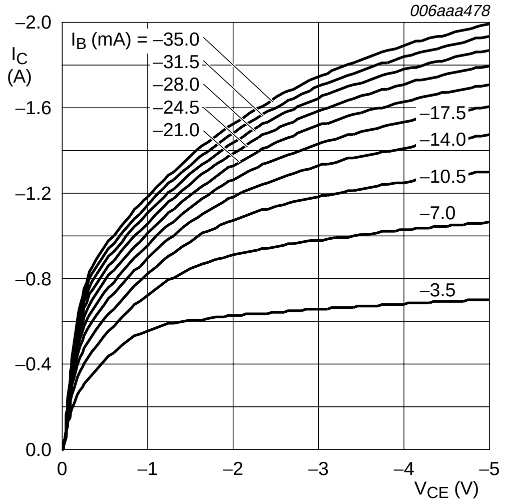

$V_{CE}$ = −5 V

(1) $T_{amb}$ = 100 °C

(2) $T_{amb}$ = 25 °C

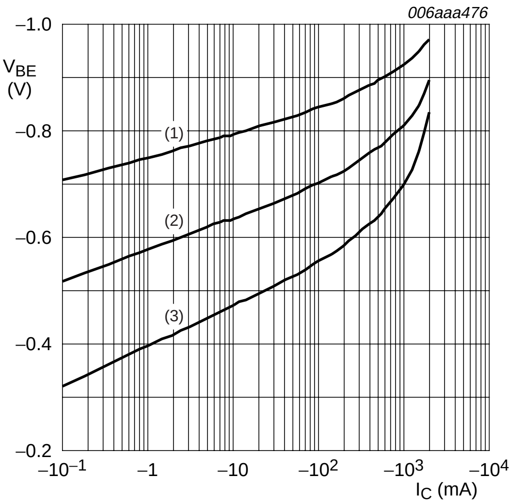
(3) $T_{amb}$ = −55 °C

**Fig 5. DC current gain as a function of collector current; typical values**




$T_{amb}$ = 25 °C

**Fig 6. Collector current as a function of collector-emitter voltage; typical values**



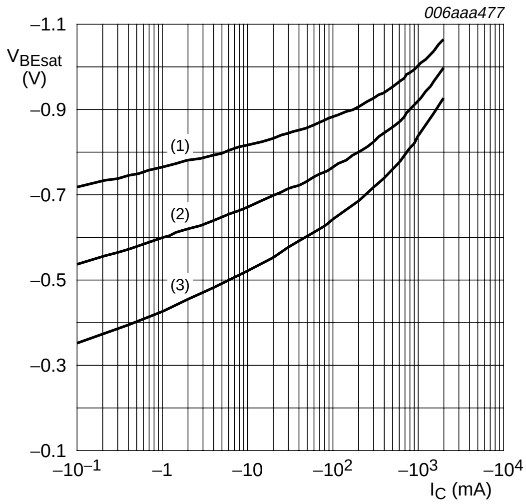

$V_{CE}$ = −5 V

(1) $T_{amb}$ = −55 °C

(2) $T_{amb}$ = 25 °C

(3) $T_{amb}$ = 100 °C

**Fig 7. Base-emitter voltage as a function of collector current; typical values**



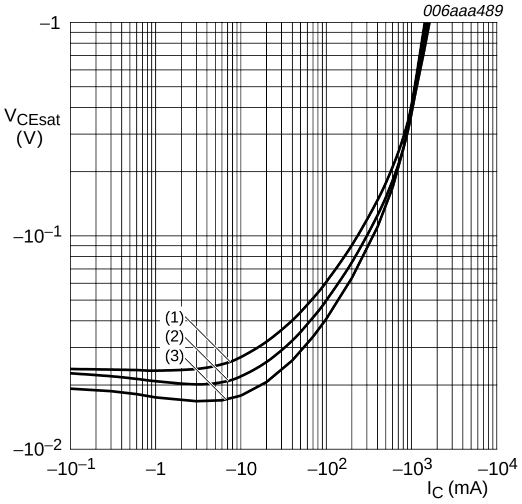

$I_C/I_B$ = 20

(1) $T_{amb}$ = −55 °C

(2) $T_{amb}$ = 25 °C

(3) $T_{amb}$ = 100 °C

**Fig 8. Base-emitter saturation voltage as a function of collector current; typical values**



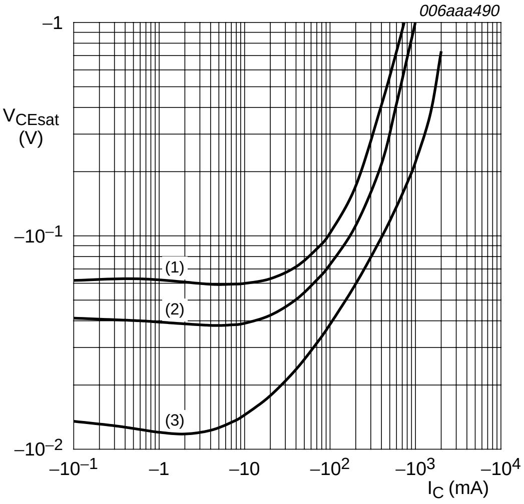

$I_C/I_B$ = 20

(1) $T_{amb}$ = 100 °C

(2) $T_{amb}$ = 25 °C

(3) $T_{amb}$ = −55 °C

**Fig 9. Collector-emitter saturation voltage as a function of collector current; typical values**



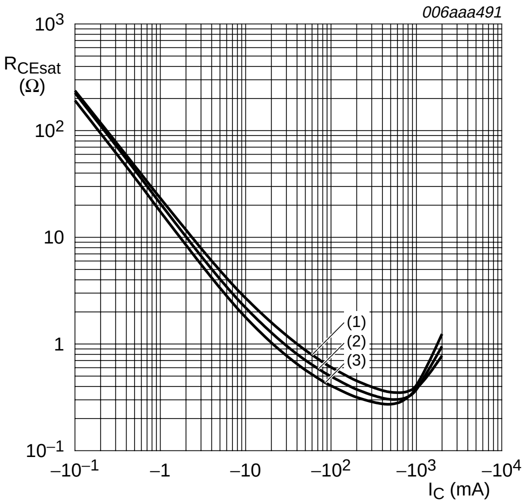

$T_{amb}$ = 25 °C

(1) $I_C/I_B$ = 100

(2) $I_C/I_B$ = 50

(3) $I_C/I_B$ = 10

**Fig 10. Collector-emitter saturation voltage as a function of collector current; typical values**



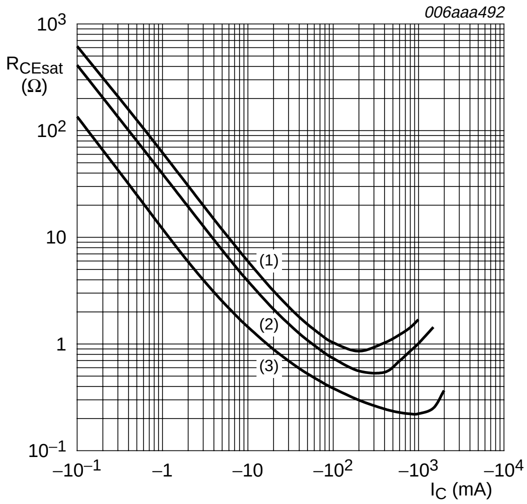

$I_C/I_B$ = 20

(1) $T_{amb}$ = 100 °C

(2) $T_{amb}$ = 25 °C

(3) $T_{amb}$ = −55 °C

**Fig 11. Collector-emitter saturation resistance as a function of collector current; typical values**




$T_{amb}$ = 25 °C

(1) $I_C/I_B$ = 100

(2) $I_C/I_B$ = 50

(3) $I_C/I_B$ = 10

**Fig 12. Collector-emitter saturation resistance as a function of collector current; typical values**

## 8. Test information

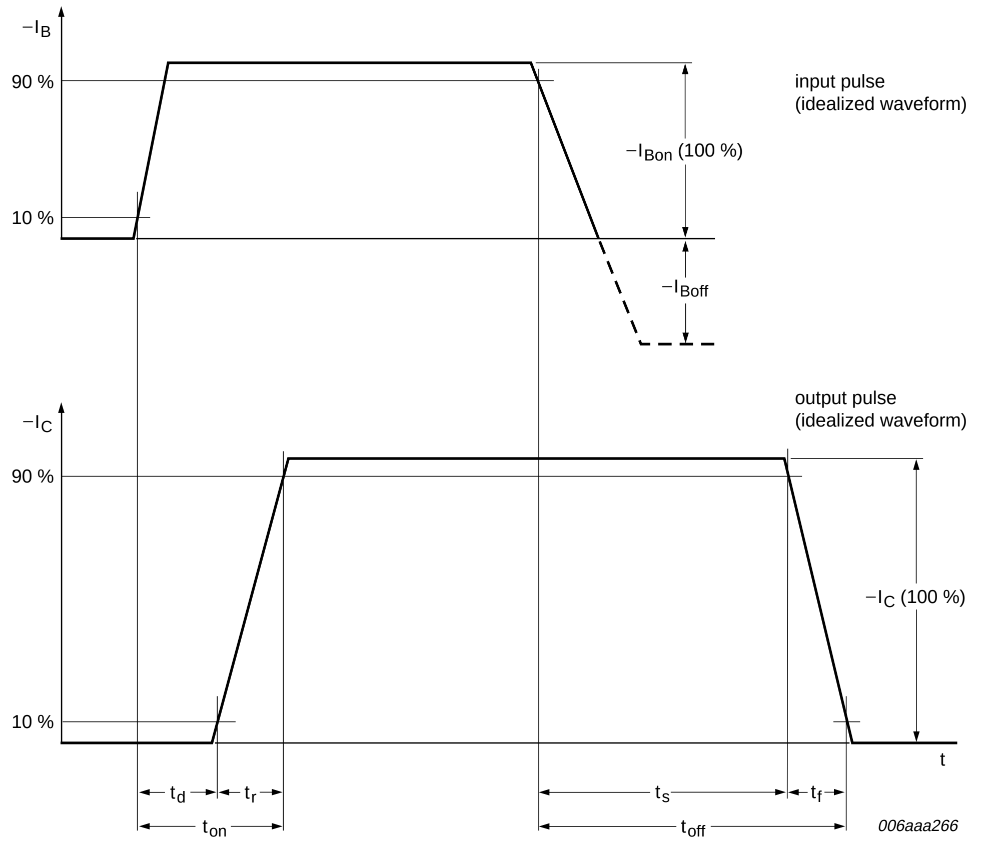
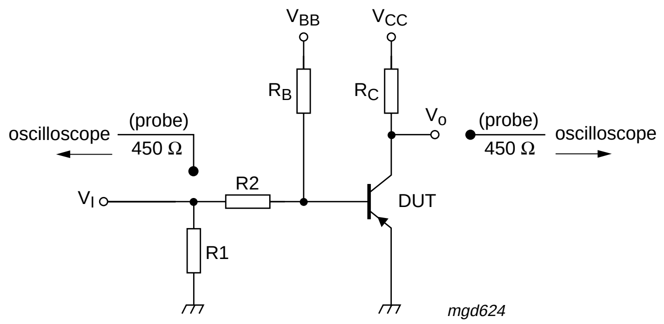



**Fig 13. BISS transistor switching time definition**




$I_C$ = –0.5 A; $I_{Bon}$ = –25 mA; $I_{Boff}$ = 25 mA; R1 = open; R2 = 100 Ω; $R_B$ = 300 Ω; $R_C$ = 20 Ω

**Fig 14. Test circuit for switching times**

# 9. Package outline

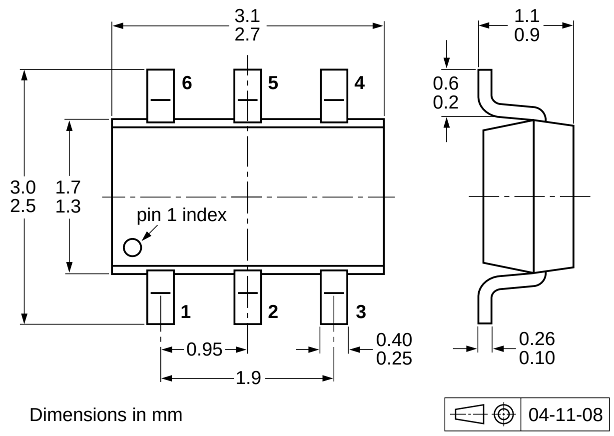



**Fig 15. Package outline SOT457 (SC-74)**

# 10. Packing information

**Table 8. Packing methods**

*The indicated -xxx are the last three digits of the 12NC ordering code.*[1]

| Type number | Package | Description | | Packing quantity | |
|---|---|---|---|---|---|
| | | | | 3000 | 10000 |
| PBSS5160DS | SOT457 | 4 mm pitch, 8 mm tape and reel; T1 | [2] | -115 | -135 |
| | | 4 mm pitch, 8 mm tape and reel; T2 | [3] | -125 | -165 |

[1] For further information and the availability of packing methods, see Section 14.

[2] T1: normal taping

[3] T2: reverse taping

# 11. Soldering

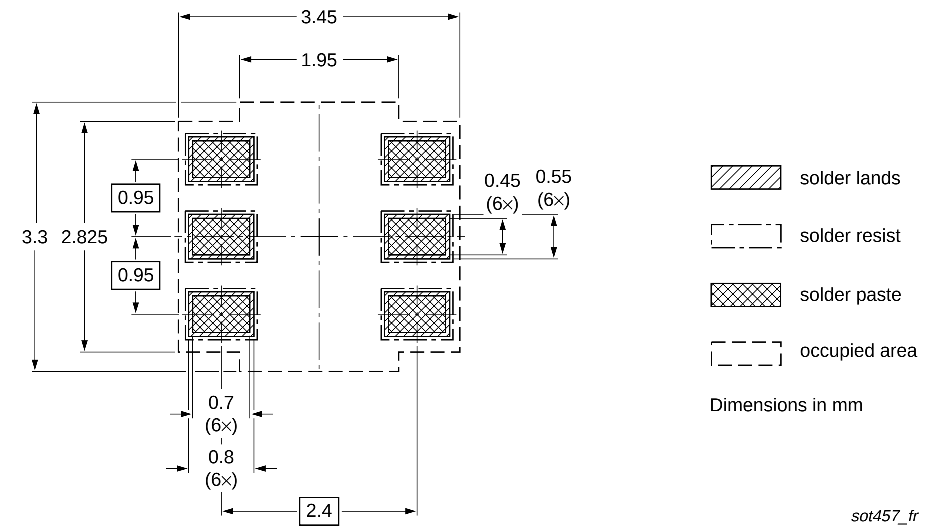



**Fig 16. Reflow soldering footprint SOT457 (SC-74)**

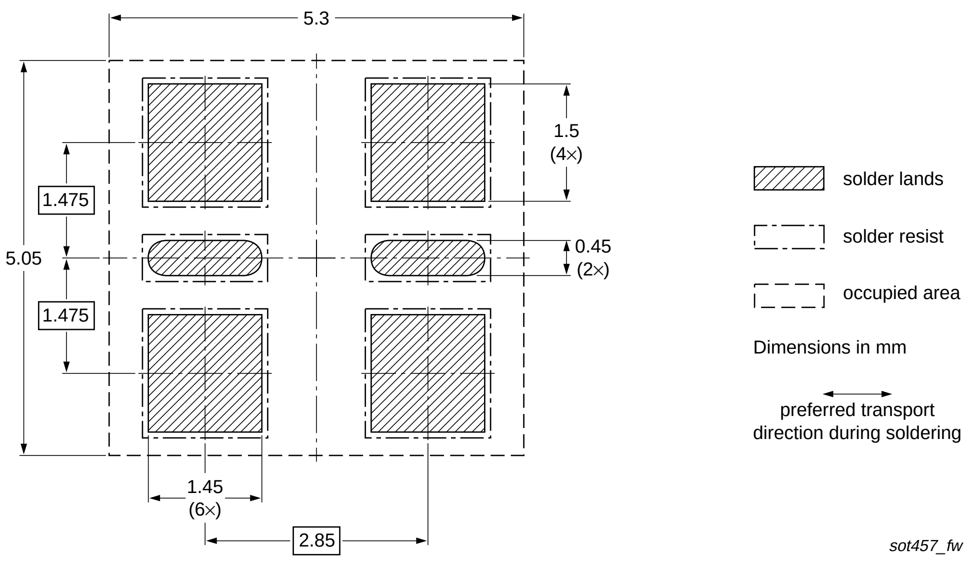



**Fig 17. Wave soldering footprint SOT457 (SC-74)**

## 12. Revision history

Table 9. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| PBSS5160DS_3 | 20081009 | Product data sheet | - | PBSS5160DS_2 |
| Modifications: | • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.<br>• Legal texts have been adapted to the new company name where appropriate.<br>• Figure 9: amended<br>• Section 13 “Legal information”: updated | | | |
| PBSS5160DS_2 | 20050628 | Product data sheet | - | PBSS5160DS_1 |
| PBSS5160DS_1 | 20040716 | Objective data sheet | - | - |

# 13. Legal information

## 13.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term ‘short data sheet’ is explained in section “Definitions”.

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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## 15. Contents





**Date of release: 9 October 2008**
**Document identifier: PBSS5160DS_3**