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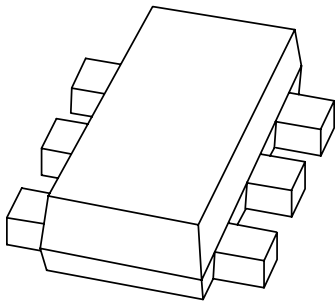
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Kind regards,

Team Nexperia

# DATA SHEET



**PBSS5240V**

40 V low  $V_{CEsat}$  PNP transistor

# 40 V low $V_{CEsat}$ PNP transistor

# PBSS5240V

### FEATURES

- Low collector-emitter saturation voltage  $V_{CEsat}$
- High collector current capability  $I_C$  and  $I_{CM}$
- High collector current gain ( $h_{FE}$ ) at high  $I_C$
- High efficiency leading to reduced heat generation
- Reduced printed-circuit board area requirements.

### APPLICATIONS

- Power management:
  - DC-DC converter
  - Supply line switching
  - Battery charger
  - LCD back lighting.
- Peripheral driver:
  - Driver in low supply voltage applications (e.g. lamps, LEDs)
  - Inductive load drivers (e.g. relay, buzzers and motors).

### DESCRIPTION

PNP transistor providing low  $V_{CEsat}$  and high current capability in a SOT666 plastic package.  
 NPN complement: PBSS4240V.

### MARKING

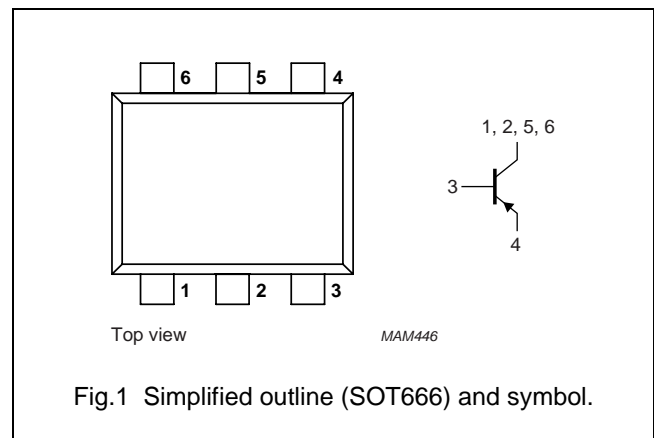
TYPE NUMBER	MARKING CODE
PBSS5240V	52

### QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
$V_{CEO}$	collector-emitter voltage	-40	V
$I_C$	collector current (DC)	-1.8	A
$I_{CRP}$	peak collector current	-2	A
$R_{CEsat}$	equivalent on-resistance	<250	m $\Omega$

### PINNING

PIN	DESCRIPTION
1	collector
2	collector
3	base
4	emitter
5	collector
6	collector



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**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CBO}$	collector-base voltage	open emitter	–	–40	V
$V_{CEO}$	collector-emitter voltage	open base	–	–40	V
$V_{EBO}$	emitter-base voltage	open collector	–	–5	V
$I_C$	collector current (DC)	note 1	–	–1.8	A
$I_{CRP}$	peak repetitive collector current	note 2	–	–2	A
$I_{CM}$	peak collector current		–	–3	A
$I_B$	base current (DC)		–	–300	mA
$I_{BM}$	peak base current		–	–1	A
$P_{tot}$	total power dissipation	$T_{amb} \leq 25\text{ °C}$ ; note 3	–	300	mW
		$T_{amb} \leq 25\text{ °C}$ ; note 4	–	500	mW
		$T_{amb} \leq 25\text{ °C}$ ; note 1	–	900	mW
		$T_{amb} \leq 25\text{ °C}$ ; notes 2 and 3	–	1.2	W
$T_{stg}$	storage temperature		–65	+150	°C
$T_j$	junction temperature		–	150	°C
$T_{amb}$	operating ambient temperature		–65	+150	°C

**Notes**

1. Device mounted on a ceramic circuit board,  $Al_2O_3$ , standard footprint.
2. Operated under pulsed conditions: duty cycle  $\delta \leq 20\%$ , pulse width  $t_p \leq 30\text{ ms}$ .
3. Device mounted on a printed-circuit board, single-sided copper, tinplated, standard footprint.
4. Device mounted on a printed-circuit board, single-sided copper, tinplated, mounting pad for collector  $1\text{ cm}^2$ .

**THERMAL CHARACTERISTICS**

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	note 1	410	K/W
		note 2	215	K/W
		note 3	140	K/W
		notes 1 and 4	110	K/W

**Notes**

1. Device mounted on a printed-circuit board, single-sided copper, tinplated, standard footprint.
2. Device mounted on a printed-circuit board, single-sided copper, tinplated, mounting pad for collector  $1\text{ cm}^2$ .
3. Device mounted on a ceramic circuit board,  $Al_2O_3$ , standard footprint.
4. Operated under pulsed conditions: duty cycle  $\delta \leq 20\%$ , pulse width  $t_p \leq 30\text{ ms}$ .

**Soldering**

The only recommended soldering method is reflow soldering.

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## PBSS5240V

**CHARACTERISTICS**

$T_{amb} = 25\text{ °C}$  unless otherwise specified.

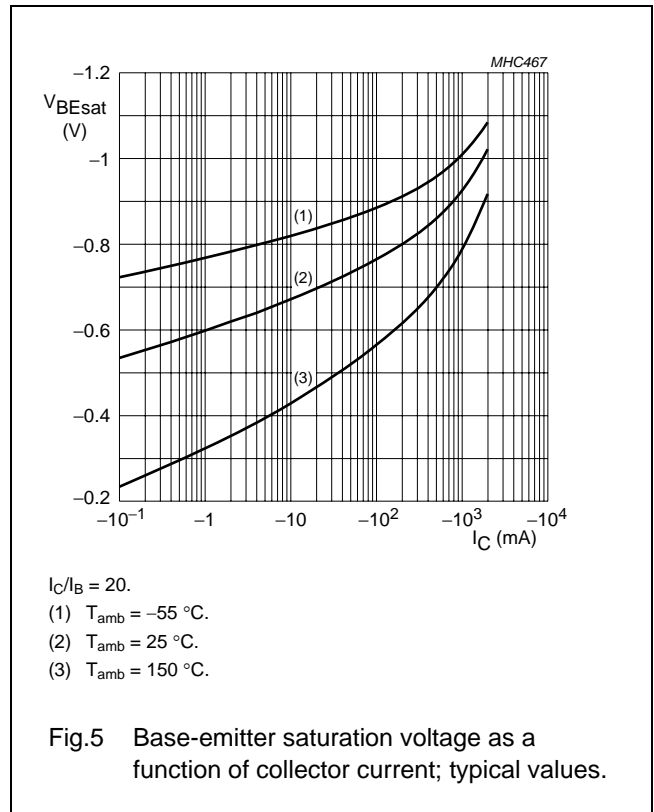
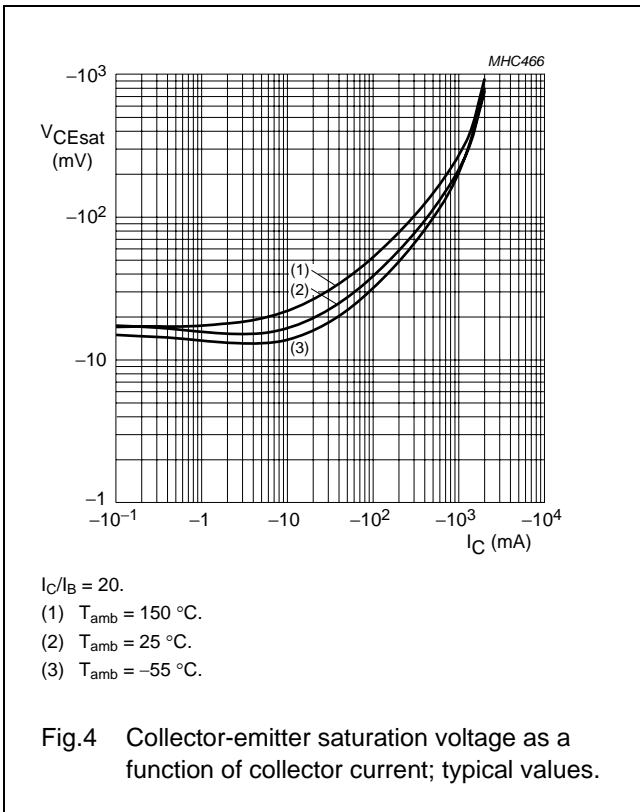
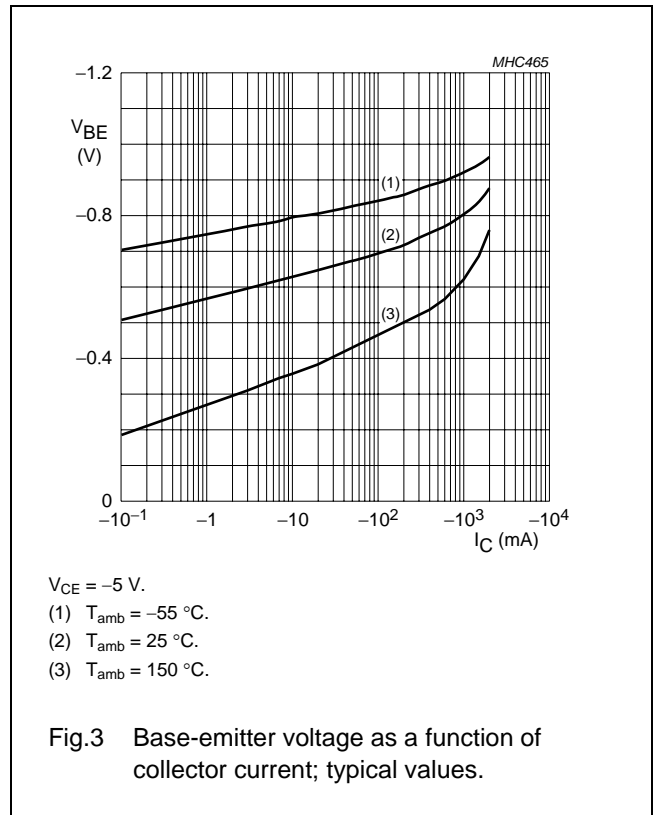
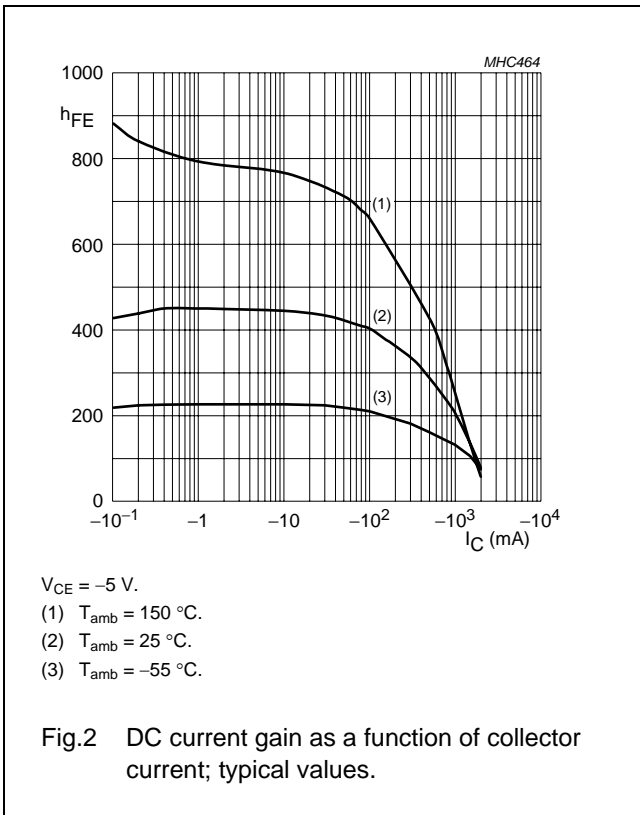
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{CBO}$	collector-base cut-off current	$V_{CB} = -40\text{ V}; I_E = 0$	–	–	–100	nA
		$V_{CB} = -40\text{ V}; I_E = 0; T_{amb} = 150\text{ °C}$	–	–	–50	$\mu\text{A}$
$I_{CEO}$	collector-emitter cut-off current	$V_{CE} = -30\text{ V}; I_B = 0$	–	–	–100	nA
$I_{EBO}$	emitter-base cut-off current	$V_{EB} = -5\text{ V}; I_C = 0$	–	–	–100	nA
$h_{FE}$	DC current gain	$V_{CE} = -5\text{ V}; I_C = -1\text{ mA}$	300	–	–	
		$V_{CE} = -5\text{ V}; I_C = -100\text{ mA}$	300	–	800	
		$V_{CE} = -5\text{ V}; I_C = -500\text{ mA}$	250	–	–	
		$V_{CE} = -5\text{ V}; I_C = -1\text{ A}$	160	–	–	
		$V_{CE} = -5\text{ V}; I_C = -2\text{ A}; \text{note 1}$	50	–	–	
$V_{CEsat}$	collector-emitter saturation voltage	$I_C = -100\text{ mA}; I_B = -1\text{ mA}$	–	–80	–120	mV
		$I_C = -500\text{ mA}; I_B = -50\text{ mA}$	–	–100	–145	mV
		$I_C = -1\text{ A}; I_B = -100\text{ mA}; \text{note 1}$	–	–180	–250	mV
		$I_C = -2\text{ A}; I_B = -200\text{ mA}$	–	–370	–530	mV
$R_{CEsat}$	equivalent on-resistance	$I_C = -1\text{ A}; I_B = -100\text{ mA}; \text{note 1}$	–	180	<250	$\text{m}\Omega$
$V_{BEsat}$	base-emitter saturation voltage	$I_C = -1\text{ A}; I_B = -100\text{ mA}$	–	–	–1.1	V
$V_{BEon}$	base-emitter turn-on voltage	$V_{CE} = -5\text{ V}; I_C = -1\text{ A}$	–	–	–1	V
$f_T$	transition frequency	$I_C = -50\text{ mA}; V_{CE} = -10\text{ V};$ $f = 100\text{ MHz}$	150	–	–	MHz
$C_c$	collector capacitance	$V_{CB} = -10\text{ V}; I_E = I_e = 0; f = 1\text{ MHz}$	–	–	12	pF

**Note**

1. Pulse test:  $t_p \leq 300\text{ }\mu\text{s}$ ;  $\delta \leq 0.02$ .

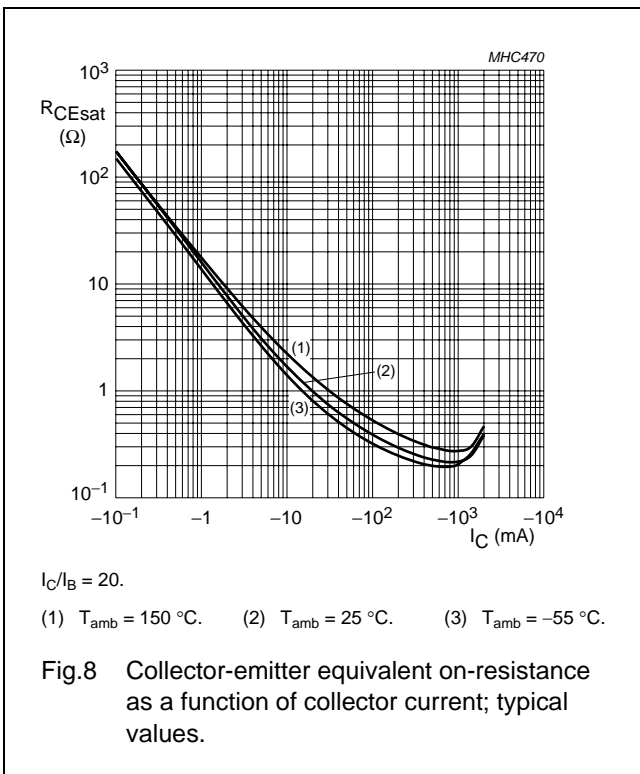
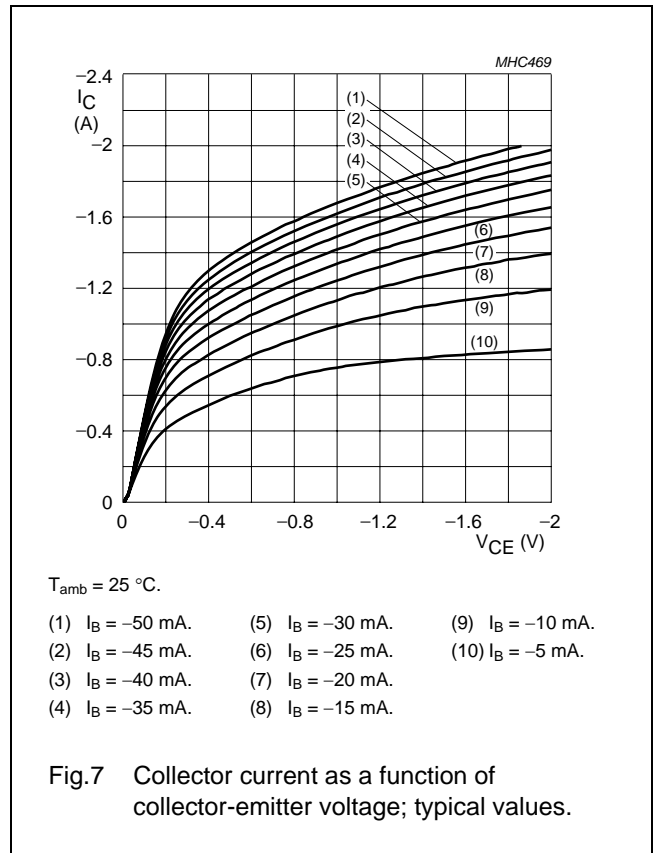
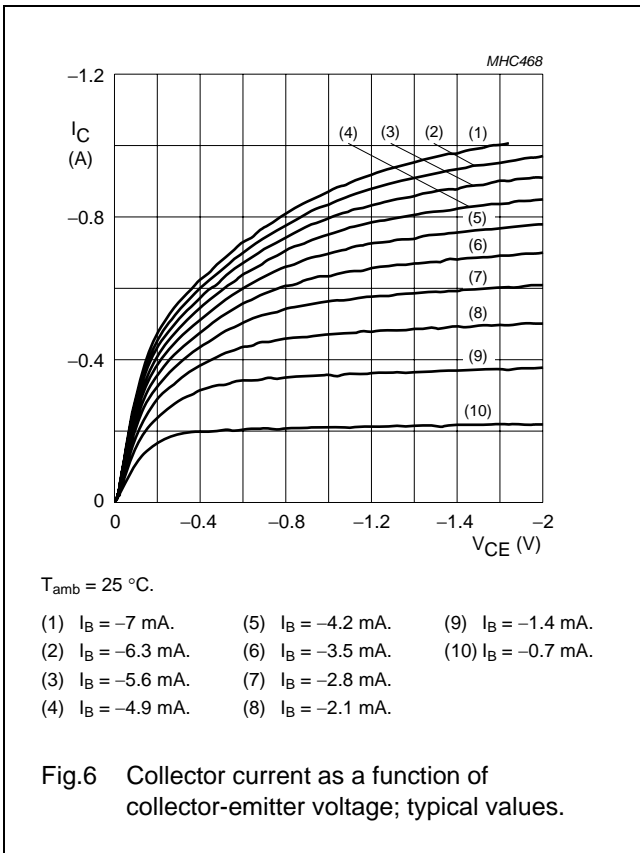
40 V low  $V_{CEsat}$  PNP transistor

PBSS5240V



40 V low  $V_{CEsat}$  PNP transistor

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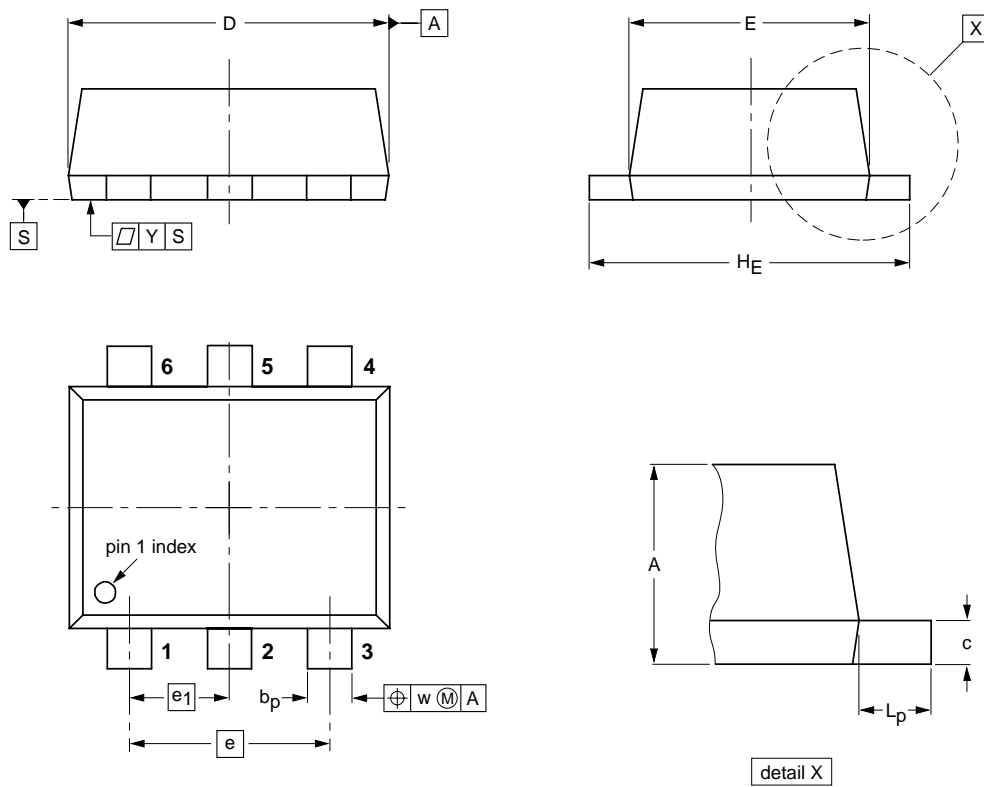
40 V low  $V_{CEsat}$  PNP transistor

PBSS5240V

PACKAGE OUTLINE

Plastic surface mounted package; 6 leads

SOT666



DIMENSIONS (mm are the original dimensions)

UNIT	A	$b_p$	c	D	E	e	$e_1$	$H_E$	$L_p$	w	y
mm	0.6 0.5	0.27 0.17	0.18 0.08	1.7 1.5	1.3 1.1	1.0	0.5	1.7 1.5	0.3 0.1	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT666						-01-01-04 01-08-27



40 V low  $V_{CEsat}$  PNP transistor

PBSS5240V

## DATA SHEET STATUS

DOCUMENT STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)</sup>	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

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# ***NXP Semiconductors***

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## **Contact information**

For additional information please visit: <http://www.nxp.com>

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