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Team Nexperia

PNP resistor-equipped transistors; R1 = 1 k Ω , R2 = 1 k Ω

Rev. 05 — 2 September 2009

Product data sheet

1. **Product profile**

1.1 General description

PNP Resistor-Equipped Transistors (RET).

Table 1. **Product overview**

Type number	Package	NPN		
	NXP	JEITA	JEDEC	complement
PDTA113EE	SOT416	SC-75	-	PDTC113EE
PDTA113EK	SOT346	SC-59A	TO-236	PDTC113EK
PDTA113EM	SOT883	SC-101	-	PDTC113EM
PDTA113ES ^[1]	SOT54 (TO-92)	SC-43A	TO-92	PDTC113ES
PDTA113ET	SOT23	-	TO-236AB	PDTC113ET
PDTA113EU	SOT323	SC-70	-	PDTC113EU

[1] Also available in SOT54A and SOT54 variant packages (see Section 2)

1.2 Features

- Built-in bias resistors
- Simplifies circuit design

1.3 Applications

- General purpose switching and amplification
- Inverter and interface circuits

1.4 Quick reference data

Table 2. **Quick reference data**

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{CEO}	collector-emitter voltage	open base	-	-	-50	V
I _O	output current (DC)		-	-	-100	mA
R1	bias resistor 1 (input)		0.7	1	1.3	kΩ
R2/R1	bias resistor ratio		0.8	1	1.2	



- Circuit drivers

Reduces component count

Reduces pick and place costs

PNP resistor-equipped transistors; R1 = 1 k Ω , R2 = 1 k Ω

2. Pinning information

Pin	Description	Simplified outline	Symbol
SOT54			
1	input (base)		
2	output (collector)		
3	GND (emitter)	1 1 2 3 001aab347	1 R2 006aaa148
SOT54A			
1	input (base)		
2	output (collector)		2
3	GND (emitter)	001aab348	R1 R2 006aaa148
SOT54 va	riant		
1	input (base)		
2	output (collector)		R1 2
3	GND (emitter)	Cm Cm D D D D D D D D D D D D D D D D D	1 R2 006aaa148
SOT23, S	OT323, SOT346, SOT416		
1	input (base)		
2	GND (emitter)	3	
3	output (collector)	1 2 006aaa144	1 R1 R2 sym003
SOT883			
1	input (base)		
2	GND (emitter)		
3	output (collector)	2 Transparent top view	

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PDTA113E_SER_5

PNP resistor-equipped transistors; R1 = 1 k Ω , R2 = 1 k Ω

3. Ordering information

Table 4. Orde	ering inforn	nation					
Type number	Package	Package					
	Name	Description	Version				
PDTA113EE	SC-75	plastic surface mounted package; 3 leads	SOT416				
PDTA113EK	SC-59A	plastic surface mounted package; 3 leads	SOT346				
PDTA113EM	SC-101	leadless ultra small plastic package; 3 solder lands; body $1.0 \times 0.6 \times 0.5$ mm	SOT883				
PDTA113ES ^[1]	SC-43A	plastic single-ended leaded (through hole) package; 3 leads	SOT54				
PDTA113ET	-	plastic surface mounted package; 3 leads	SOT23				
PDTA113EU	SC-70	plastic surface mounted package; 3 leads	SOT323				

[1] Also available in SOT54A and SOT54 variant packages (see <u>Section 2</u> and <u>Section 9</u>).

4. Marking

Type numberMarking code[1]PDTA113EE16PDTA113EK17PDTA113EMG4PDTA113ESTA113E	
PDTA113EK17PDTA113EMG4PDTA113ESTA113E	
PDTA113EM G4 PDTA113ES TA113E	
PDTA113ES TA113E	
PDTA113ET *15	
PDTA113EU *14	

[1] * = -: made in Hong Kong

* = p: made in Hong Kong

* = t: made in Malaysia

* = W: made in China

PNP resistor-equipped transistors; R1 = 1 k Ω , R2 = 1 k Ω

5. Limiting values

Symbol	Parameter	Conditions	Min	Мах	Unit
V _{CBO}	collector-base voltage	open emitter	-	-50	V
V _{CEO}	collector-emitter voltage	open base	-	-50	V
V _{EBO}	emitter-base voltage	open collector	-	-10	V
VI	input voltage				
	positive		-	+10	V
	negative		-	-10	V
lo	output current (DC)		-	-100	mA
I _{CM}	peak collector current		-	-100	mA
P _{tot}	total power dissipation	$T_{amb} \le 25 \ ^{\circ}C$			
	SOT416		<u>[1]</u> -	150	mW
	SOT346		<u>[1]</u> -	250	mW
	SOT883		[2][3]	250	mW
	SOT54		<u>[1]</u> -	500	mW
	SOT23		<u>[1]</u> -	250	mW
	SOT323		<u>[1]</u> -	200	mW
T _{stg}	storage temperature		-65	+150	°C
Tj	junction temperature		-	150	°C
T _{amb}	ambient temperature		-65	+150	°C

[1] Refer to standard mounting conditions

[2] Reflow soldering is the only recommended soldering method.

[3] Refer to SOT883 standard mounting conditions; FR4 printed-circuit board with 60 µm copper strip line.

6. Thermal characteristics

Table 7.	Thermal characteristics					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R _{th(j-a)}	thermal resistance from junction to ambient	in free air				
	SOT416		<u>[1]</u> -	-	833	K/W
	SOT346		<u>[1]</u> -	-	500	K/W
	SOT883		[2][3] _	-	500	K/W
	SOT54		<u>[1]</u> -	-	250	K/W
	SOT23		<u>[1]</u> -	-	500	K/W
	SOT323		<u>[1]</u> -	-	625	K/W

[1] Refer to standard mounting conditions.

[2] Reflow soldering is the only recommended soldering method.

[3] Refer to SOT883 standard mounting conditions; FR4 printed-circuit board with 60 µm copper strip line.

PNP resistor-equipped transistors; R1 = 1 k Ω , R2 = 1 k Ω

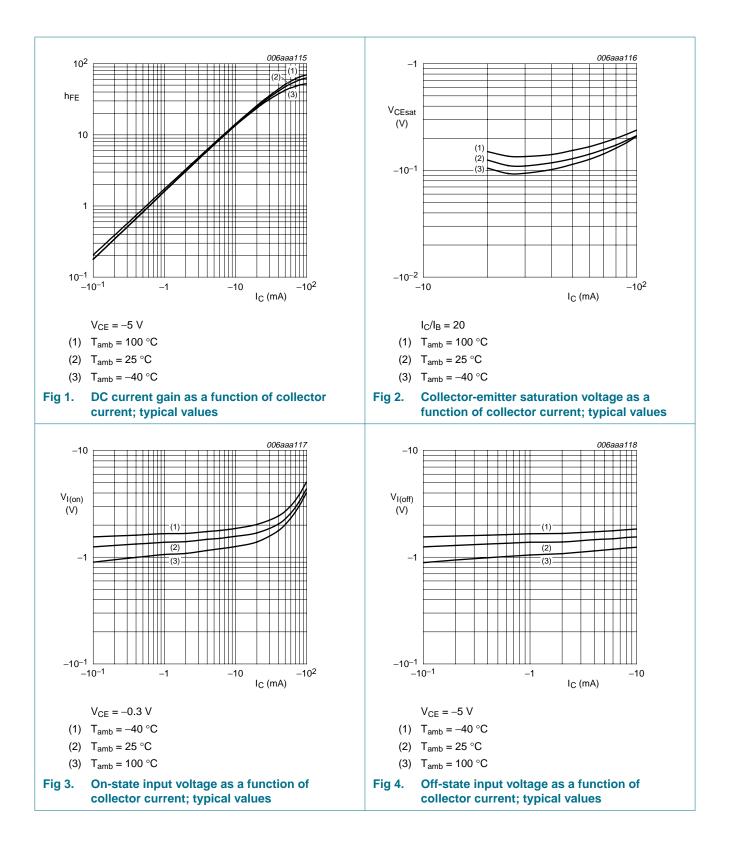
7. Characteristics

Table 8.Characteristics

 $T_{amb} = 25 \circ C$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
I _{CBO}	collector-base cut-off current	$V_{CB} = -50 \text{ V}; I_E = 0 \text{ A}$	-	-	-100	nA
I _{CEO}		$V_{CE} = -30 \text{ V}; I_B = 0 \text{ A}$	-	-	-1	μA
	cut-off current	$V_{CE} = -30 \text{ V}; I_B = 0 \text{ A};$ $T_j = 150 \text{ °C}$	-	-	-50	μΑ
I _{EBO}	emitter-base cut-off current	$V_{EB} = -5 \text{ V}; \text{ I}_{C} = 0 \text{ A}$	-	-	-4	mA
h _{FE}	DC current gain	$V_{CE} = -5 \text{ V}; I_C = -40 \text{ mA}$	30	-	-	
V _{CEsat}	collector-emitter saturation voltage	$I_{C} = -30$ mA; $I_{B} = -1.5$ mA	-	-	-150	mV
V _{I(off)}	off-state input voltage	V_{CE} = -5 V; I _C = -100 μ A	-	-1.3	-0.5	V
V _{I(on)}	on-state input voltage	V_{CE} = -300 mV; I _C = -20 mA	-2	-1.7	-	V
R1	bias resistor 1 (input)		0.7	1	1.3	kΩ
R2/R1	bias resistor ratio		0.8	1	1.2	
C _c	collector capacitance	$V_{CB} = -10 \text{ V}; \text{ I}_{E} = \text{i}_{e} = 0 \text{ A};$ f = 1 MHz	-	-	2	pF

PNP resistor-equipped transistors; R1 = 1 k Ω , R2 = 1 k Ω



NXP Semiconductors

PDTA113E series

PNP resistor-equipped transistors; R1 = 1 k Ω , R2 = 1 k Ω

8. Package outline

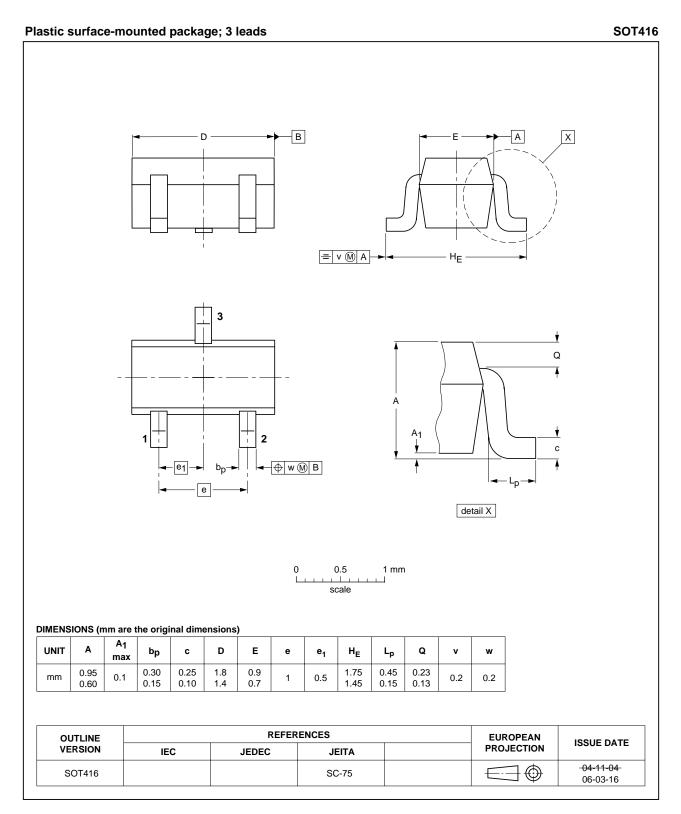


Fig 5. Package outline SOT416 (SC-75)

PNP resistor-equipped transistors; R1 = 1 k Ω , R2 = 1 k Ω

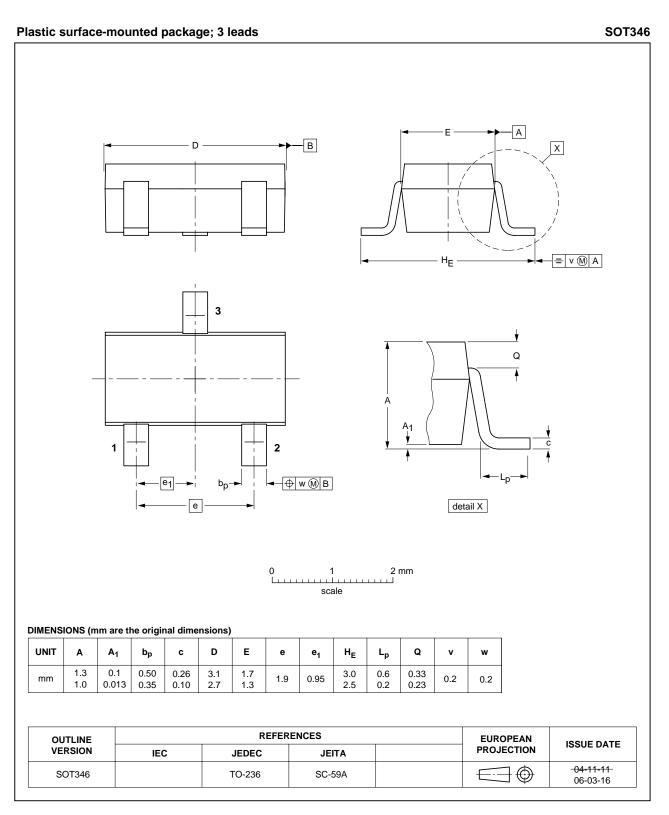


Fig 6. Package outline SOT346 (SC-59A/TO-236)

PNP resistor-equipped transistors; R1 = 1 k Ω , R2 = 1 k Ω

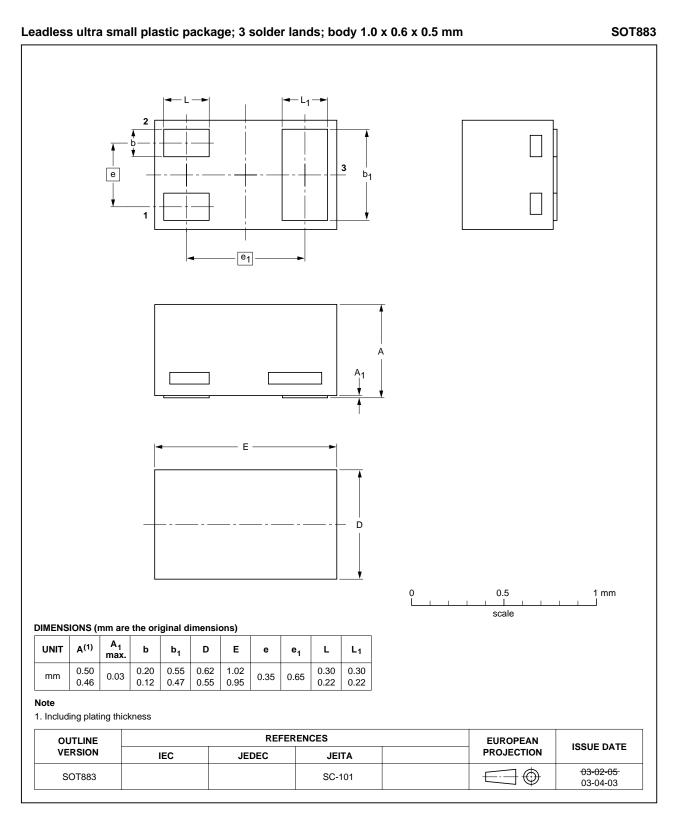


Fig 7. Package outline SOT883 (SC-101)

PNP resistor-equipped transistors; R1 = 1 k Ω , R2 = 1 k Ω

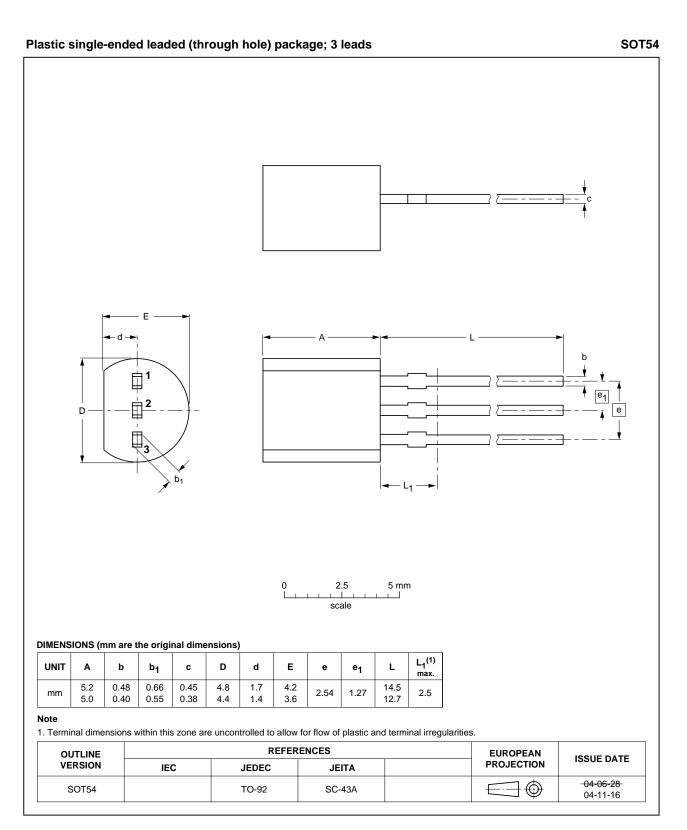


Fig 8. Package outline SOT54 (SC-43A/TO-92)

PNP resistor-equipped transistors; R1 = 1 k Ω , R2 = 1 k Ω

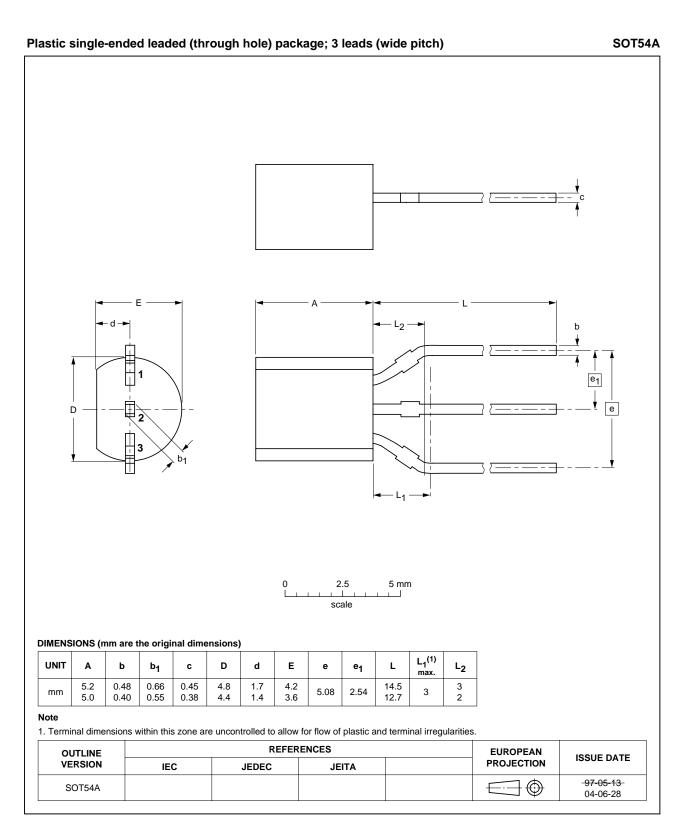


Fig 9. Package outline SOT54A

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Product data sheet

PNP resistor-equipped transistors; R1 = 1 k Ω , R2 = 1 k Ω

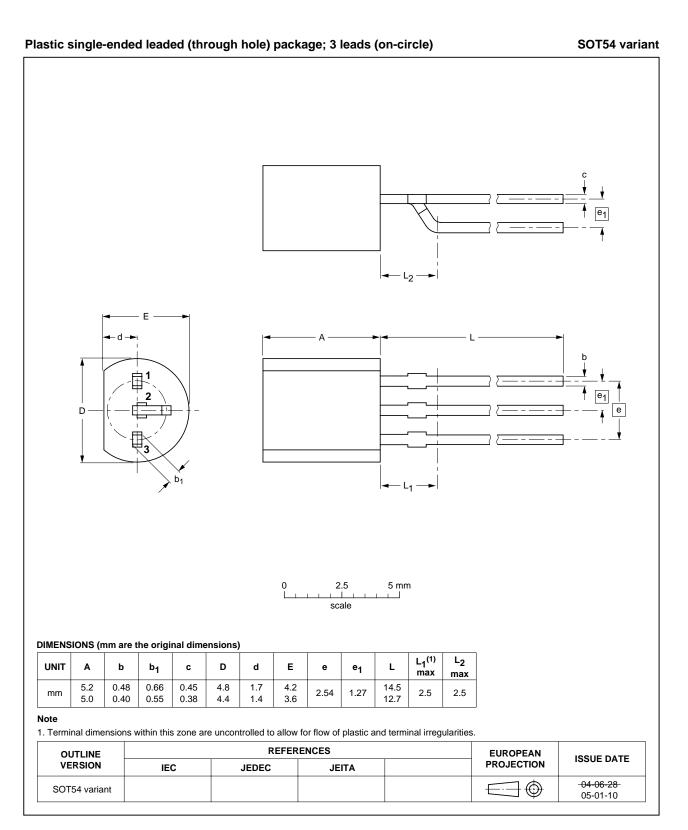


Fig 10. Package outline SOT54 variant

PNP resistor-equipped transistors; R1 = 1 k Ω , R2 = 1 k Ω

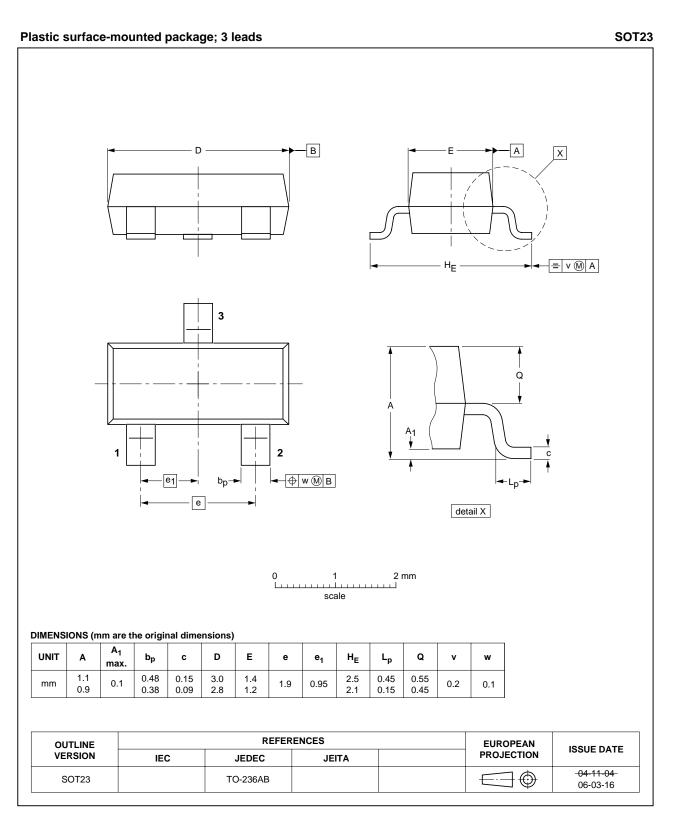


Fig 11. Package outline SOT23 (TO-236AB)

PNP resistor-equipped transistors; R1 = 1 k Ω , R2 = 1 k Ω

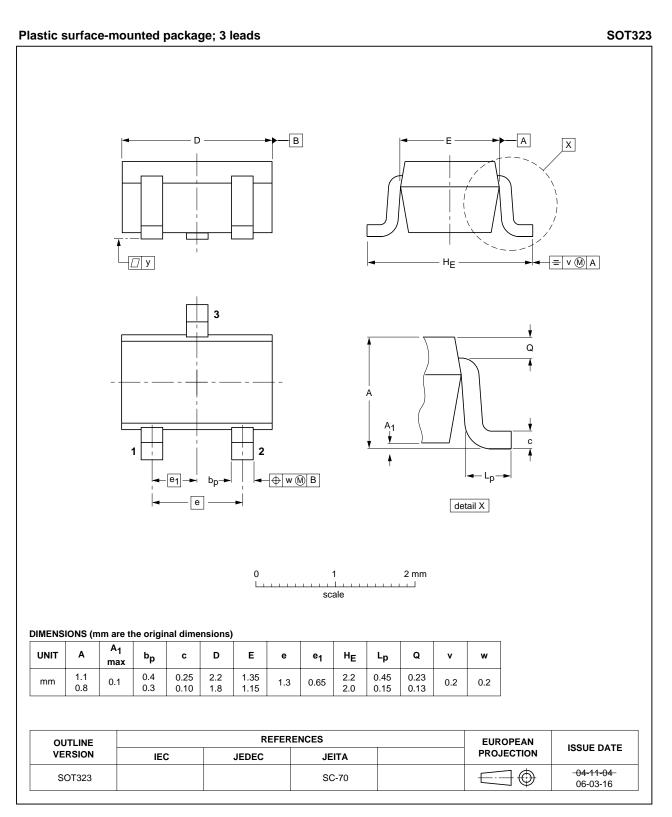


Fig 12. Package outline SOT323 (SC-70)

PNP resistor-equipped transistors; R1 = 1 k Ω , R2 = 1 k Ω

9. Packing information

Table 9. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code. [1]

Type number	Package	e Description		Packing quantity		
			3000	5000	10000	
PDTA113EE	SOT416	4 mm pitch, 8 mm tape and reel	-115	-	-135	
PDTA113EK	SOT346	4 mm pitch, 8 mm tape and reel	-115	-	-135	
PDTA113EM	SOT883	2 mm pitch, 8 mm tape and reel	-	-	-315	
PDTA113ES	SOT54	bulk, straight leads	-	-412	-	
	SOT54A	tape and reel, wide pitch	-	-	-116	
	SOT54A	tape ammopack, wide patch	-	-	-126	
	SOT54 variant	bulk, delta pinning	-	-112	-	
PDTA113ET	SOT23	4 mm pitch, 8 mm tape and reel	-215	-	-235	
PDTA113EU	SOT323	4 mm pitch, 8 mm tape and reel	-115	-	-135	

[1] For further information and the availability of packing methods, see Section 12.

PNP resistor-equipped transistors; R1 = 1 k Ω , R2 = 1 k Ω

10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PDTA113E_SER_5	20090902	Product data sheet	-	PDTA113E_SER_4
Modifications:		eet was changed to reflect w legal definitions and discl		
	Figure 5 "Page 5"	ckage outline SOT416 (SC-	75)" updated	
	Figure 6 "Pa	ckage outline SOT346 (SC-	59A/TO-236)" updated	k
	Figure 11 "P	ackage outline SOT23 (TO-	236AB)" updated	
	Figure 12 "P	ackage outline SOT323 (SC	C-70)" updated	
PDTA113E_SER_4	20050405	Product data sheet	-	PDTA113ET_3
PDTA113ET_3	20040720	Objective data sheet	-	PDTA113ET_2
PDTA113ET_2	20040415	Objective data sheet	-	PDTA113ET_1
PDTA113ET_1	20040316	Objective data sheet	-	-

11. Legal information

11.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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PDTA113E_SER_5
Product data sheet

NXP Semiconductors

PDTA113E series

PNP resistor-equipped transistors; R1 = 1 k Ω , R2 = 1 k Ω

13. Contents

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Date of release: 2 September 2009 Document identifier: PDTA113E_SER_5



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