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Kind regards,

Team Nexperia

PDTA114Y series

PNP resistor-equipped transistors;
R1 = 10 k Ω , R2 = 47 k Ω

Rev. 5 — 18 November 2011

Product data sheet

1. Product profile

1.1 General description

PNP Resistor-Equipped Transistor (RET) family in Surface-Mounted Device (SMD) plastic packages.

Table 1. Product overview

Type number	Package			NPN complement	Package configuration
	NXP	JEITA	JEDEC		
PDTA114YE	SOT416	SC-75	-	PDTC114YE	ultra small
PDTA114YM	SOT883	SC-101	-	PDTC114YM	leadless ultra small
PDTA114YT	SOT23	-	TO-236AB	PDTC114YT	small
PDTA114YU	SOT323	SC-70	-	PDTC114YU	very small

1.2 Features and benefits

- 100 mA output current capability
- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs
- AEC-Q101 qualified

1.3 Applications

- Digital applications in automotive and industrial segments
- Control of IC inputs
- Cost-saving alternative for BC847/857 series in digital applications
- Switching loads

1.4 Quick reference data

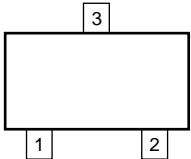
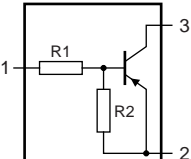
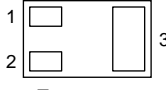
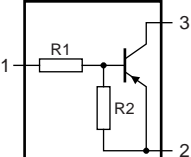
Table 2. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CEO}	collector-emitter voltage	open base	-	-	-50	V
I _O	output current		-	-	-100	mA
R1	bias resistor 1 (input)		7	10	13	k Ω
R2/R1	bias resistor ratio		3.7	4.7	5.7	



2. Pinning information

Table 3. Pinning

Pin	Description	Simplified outline	Graphic symbol
SOT23; SOT323; SOT416			
1	input (base)	 <p>006aaa144</p>	 <p>sym003</p>
2	GND (emitter)		
3	output (collector)		
SOT883			
1	input (base)	 <p>Transparent top view</p>	 <p>sym003</p>
2	GND (emitter)		
3	output (collector)		

3. Ordering information

Table 4. Ordering information

Type number	Package		
	Name	Description	Version
PDTA114YE	SC-75	plastic surface-mounted package; 3 leads	SOT416
PDTA114YM	SC-101	leadless ultra small plastic package; 3 solder lands; body 1.0 × 0.6 × 0.5 mm	SOT883
PDTA114YT	-	plastic surface-mounted package; 3 leads	SOT23
PDTA114YU	SC-70	plastic surface-mounted package; 3 leads	SOT323

4. Marking

Table 5. Marking codes

Type number	Marking code ^[1]
PDTA114YE	36
PDTA114YM	DF
PDTA114YT	*29
PDTA114YU	*55

[1] * = placeholder for manufacturing site code

5. Limiting values

Table 6. Limiting values

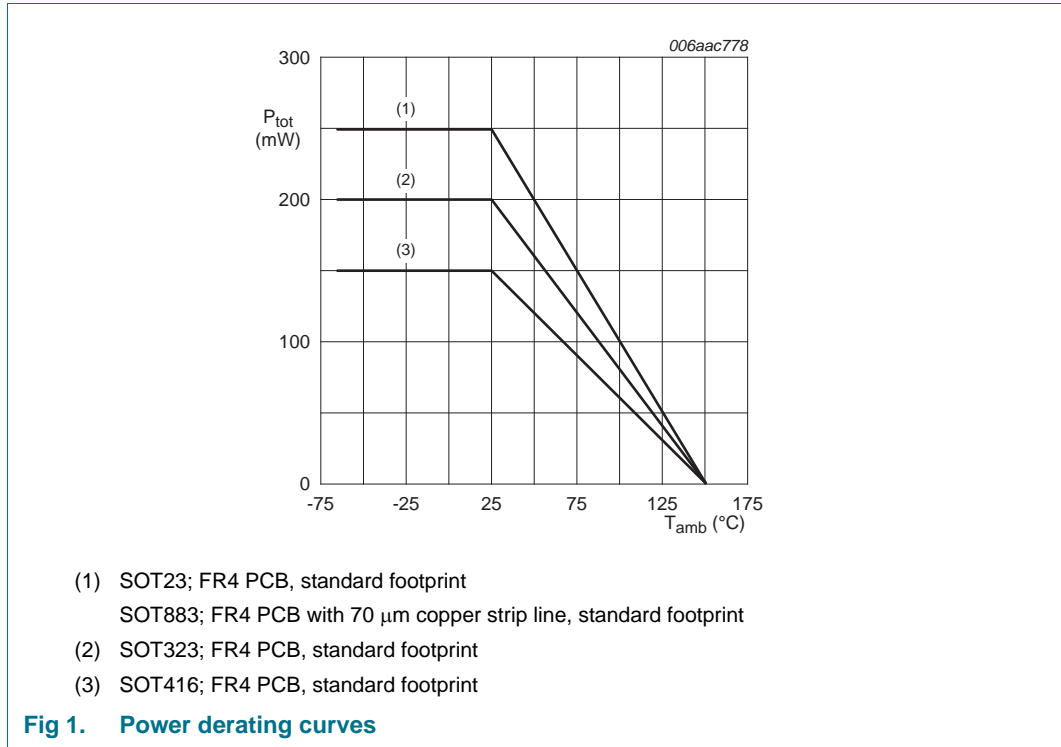
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
V _{CBO}	collector-base voltage	open emitter	-	-50	V	
V _{CEO}	collector-emitter voltage	open base	-	-50	V	
V _{EBO}	emitter-base voltage	open collector	-	-6	V	
V _I	input voltage					
	positive		-	+6	V	
	negative		-	-40	V	
I _O	output current		-	-100	mA	
I _{CM}	peak collector current	single pulse; t _p ≤ 1 ms	-	-100	mA	
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C				
	PDTA114YE (SOT416)		[1][2]	-	150	mW
	PDTA114YM (SOT883)		[2][3]	-	250	mW
	PDTA114YT (SOT23)		[1]	-	250	mW
	PDTA114YU (SOT323)		[1]	-	200	mW
T _j	junction temperature		-	150	°C	
T _{amb}	ambient temperature		-65	+150	°C	
T _{stg}	storage temperature		-65	+150	°C	

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

[2] Reflow soldering is the only recommended soldering method.

[3] Device mounted on an FR4 PCB with 70 μ m copper strip line, standard footprint.



6. Thermal characteristics

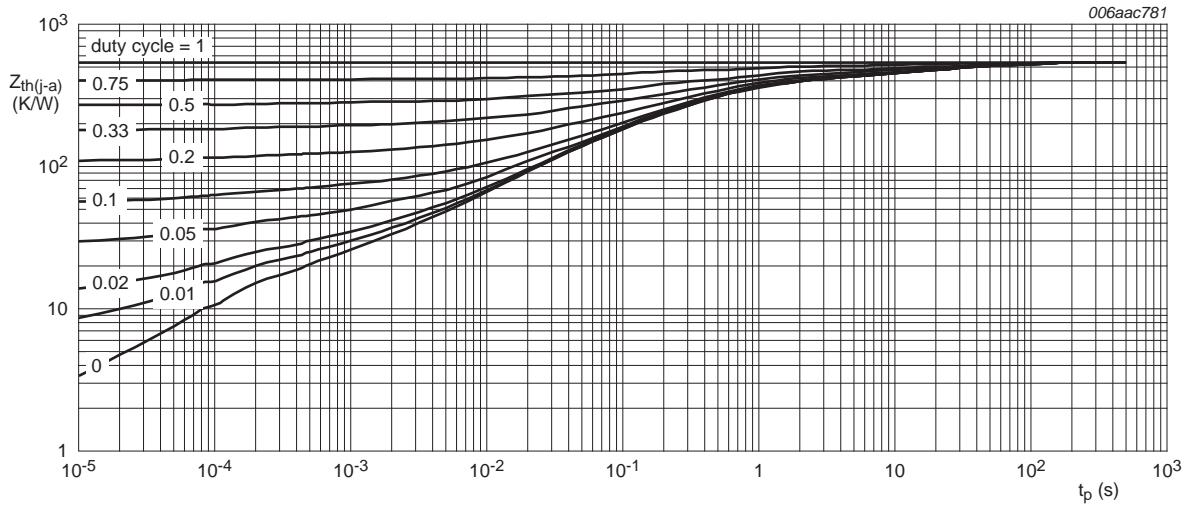
Table 7. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air				
	PDTA114YE (SOT416)	[1][2]	-	-	830	K/W
	PDTA114YM (SOT883)	[2][3]	-	-	500	K/W
	PDTA114YT (SOT23)	[1]	-	-	500	K/W
	PDTA114YU (SOT323)	[1]	-	-	625	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

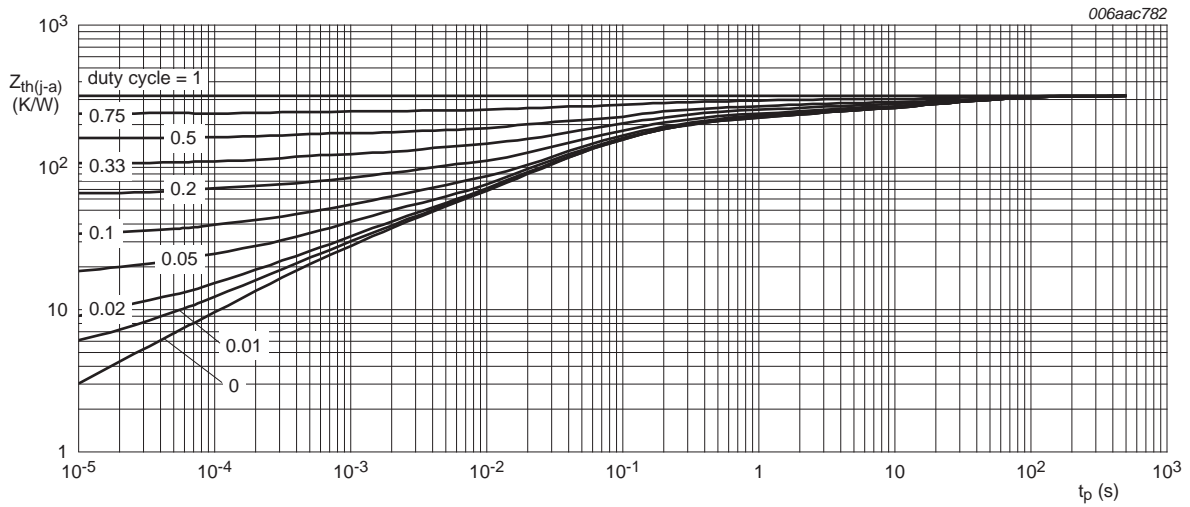
[2] Reflow soldering is the only recommended soldering method.

[3] Device mounted on an FR4 PCB with 70 μm copper strip line, standard footprint.



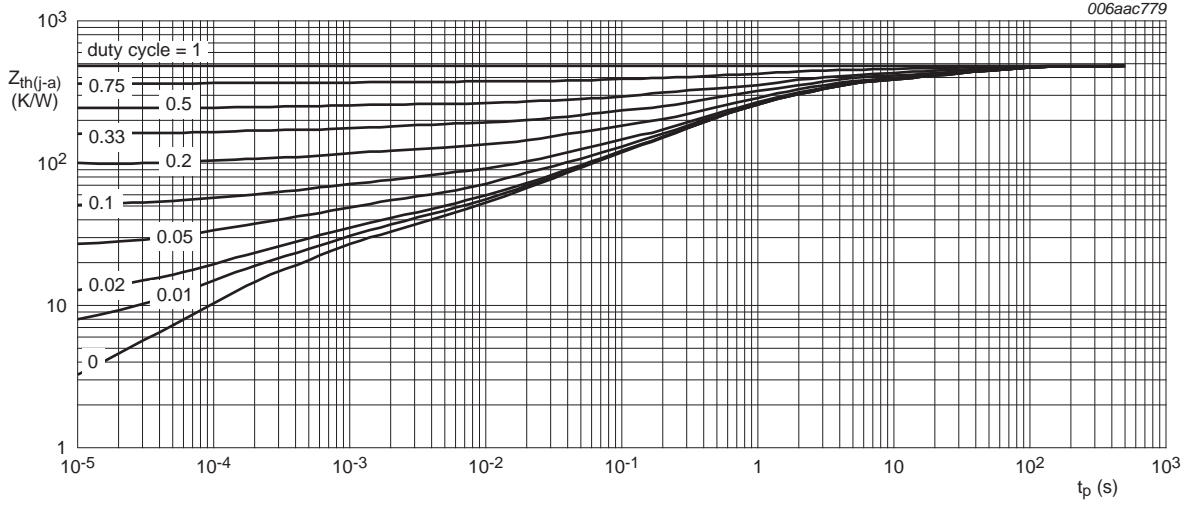
FR4 PCB, standard footprint

Fig 2. Transient thermal impedance from junction to ambient as a function of pulse duration for PDTA114YE (SOT416); typical values



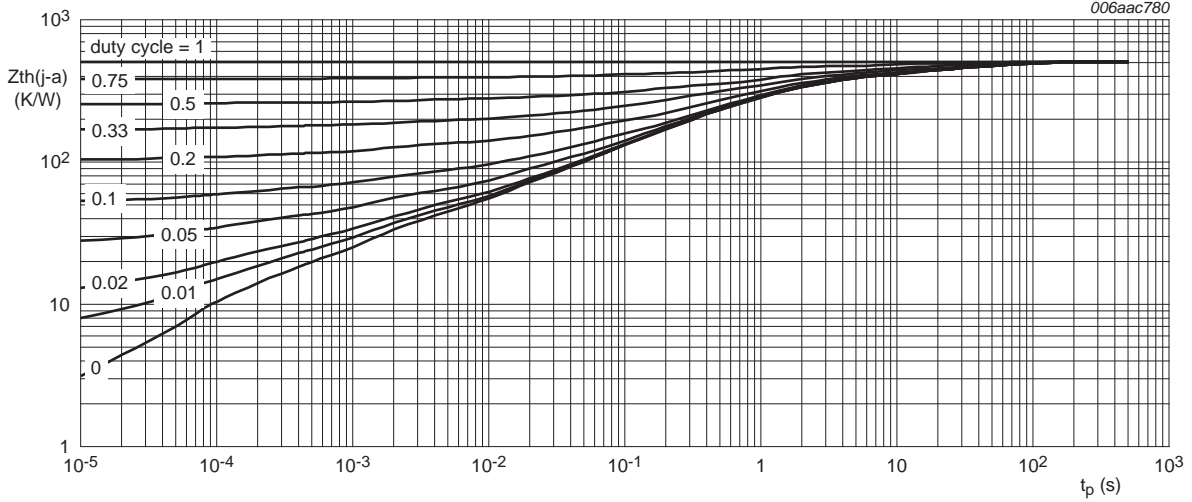
FR4 PCB, 70 μm copper strip line

Fig 3. Transient thermal impedance from junction to ambient as a function of pulse duration for PDTA114YM (SOT883); typical values



FR4 PCB, standard footprint

Fig 4. Transient thermal impedance from junction to ambient as a function of pulse duration for PDTA114YT (SOT23); typical values



FR4 PCB, standard footprint

Fig 5. Transient thermal impedance from junction to ambient as a function of pulse duration for PDTA114YU (SOT323); typical values

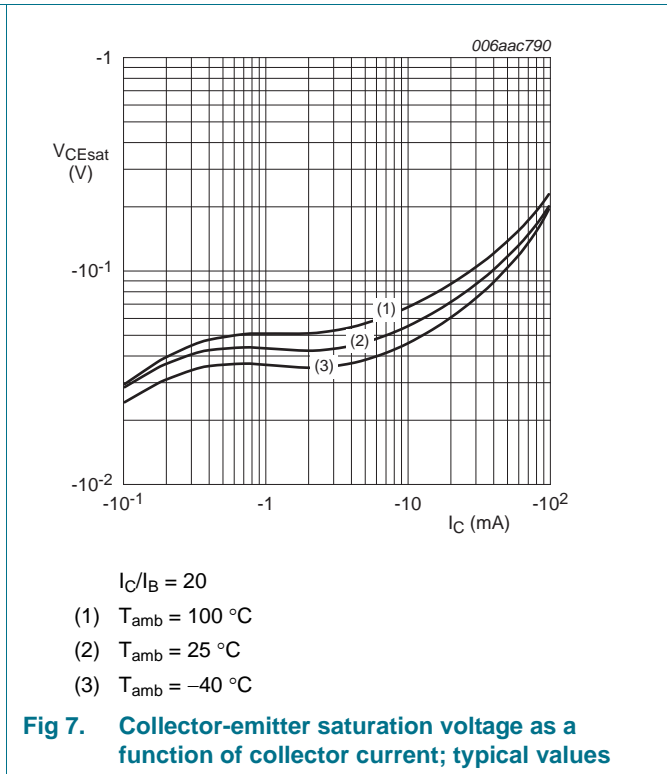
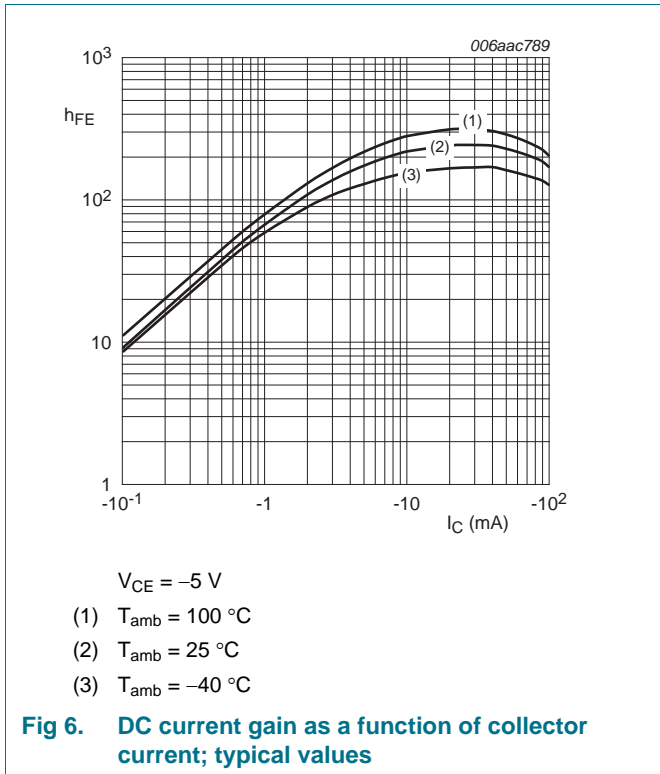
7. Characteristics

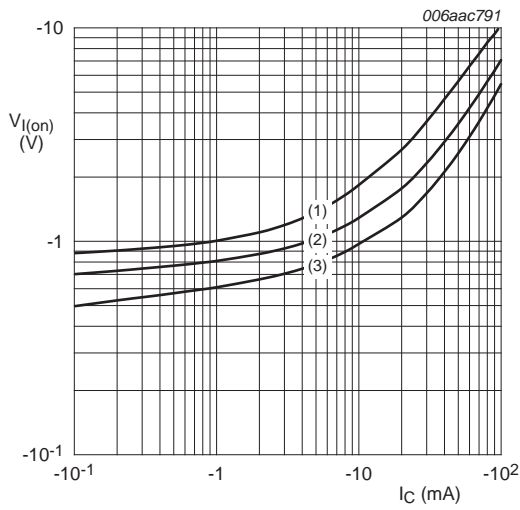
Table 8. Characteristics

T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I _{CBO}	collector-base cut-off current	V _{CB} = -50 V; I _E = 0 A	-	-	-100	nA
I _{CEO}	collector-emitter cut-off current	V _{CE} = -30 V; I _B = 0 A	-	-	-1	μA
		V _{CE} = -30 V; I _B = 0 A; T _j = 150 °C	-	-	-5	μA
I _{EBO}	emitter-base cut-off current	V _{EB} = -5 V; I _C = 0 A	-	-	-150	μA
h _{FE}	DC current gain	V _{CE} = -5 V; I _C = -5 mA	100	-	-	
V _{CEsat}	collector-emitter saturation voltage	I _C = -5 mA; I _B = -0.25 mA	-	-	-100	mV
V _{I(off)}	off-state input voltage	V _{CE} = -5 V; I _C = -100 μA	-	-0.7	-0.5	V
V _{I(on)}	on-state input voltage	V _{CE} = -0.3 V; I _C = -1 mA	-1.4	-0.8	-	V
R1	bias resistor 1 (input)		7	10	13	kΩ
R2/R1	bias resistor ratio		3.7	4.7	5.7	
C _c	collector capacitance	V _{CB} = -10 V; I _E = i _e = 0 A; f = 1 MHz	-	-	3	pF
f _T	transition frequency	V _{CE} = -5 V; I _C = -10 mA; [1]	-	180	-	MHz
		f = 100 MHz				

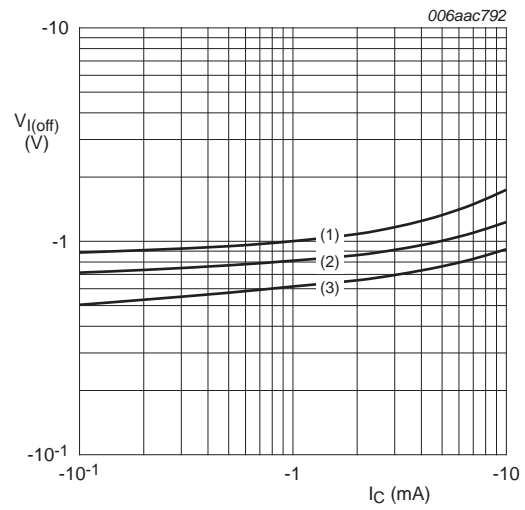
[1] Characteristics of built-in transistor





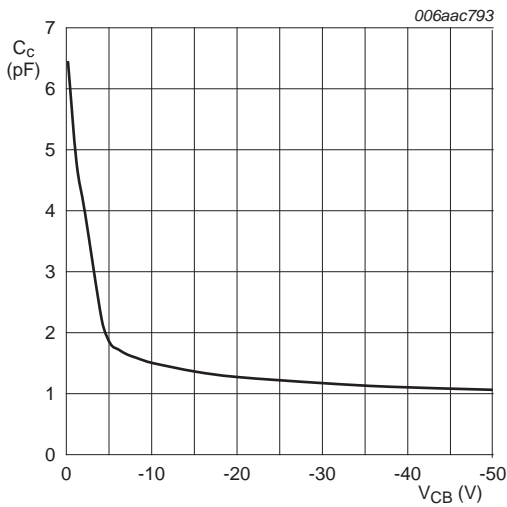
$V_{CE} = -0.3 \text{ V}$
 (1) $T_{amb} = -40 \text{ }^\circ\text{C}$
 (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 (3) $T_{amb} = 100 \text{ }^\circ\text{C}$

Fig 8. On-state input voltage as a function of collector current; typical values



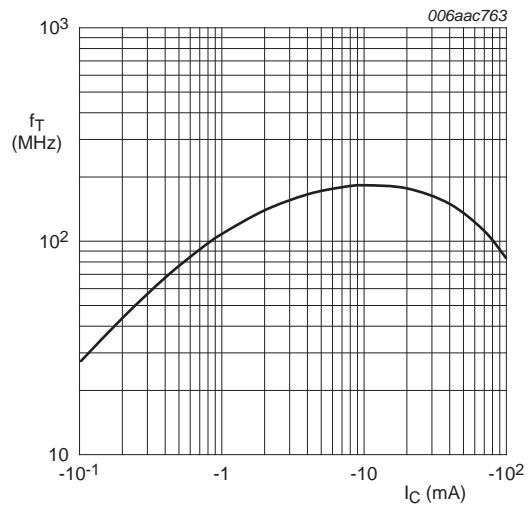
$V_{CE} = -5 \text{ V}$
 (1) $T_{amb} = -40 \text{ }^\circ\text{C}$
 (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 (3) $T_{amb} = 100 \text{ }^\circ\text{C}$

Fig 9. Off-state input voltage as a function of collector current; typical values



$f = 1 \text{ MHz}; T_{amb} = 25 \text{ }^\circ\text{C}$

Fig 10. Collector capacitance as a function of collector-base voltage; typical values



$V_{CE} = -5 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}$

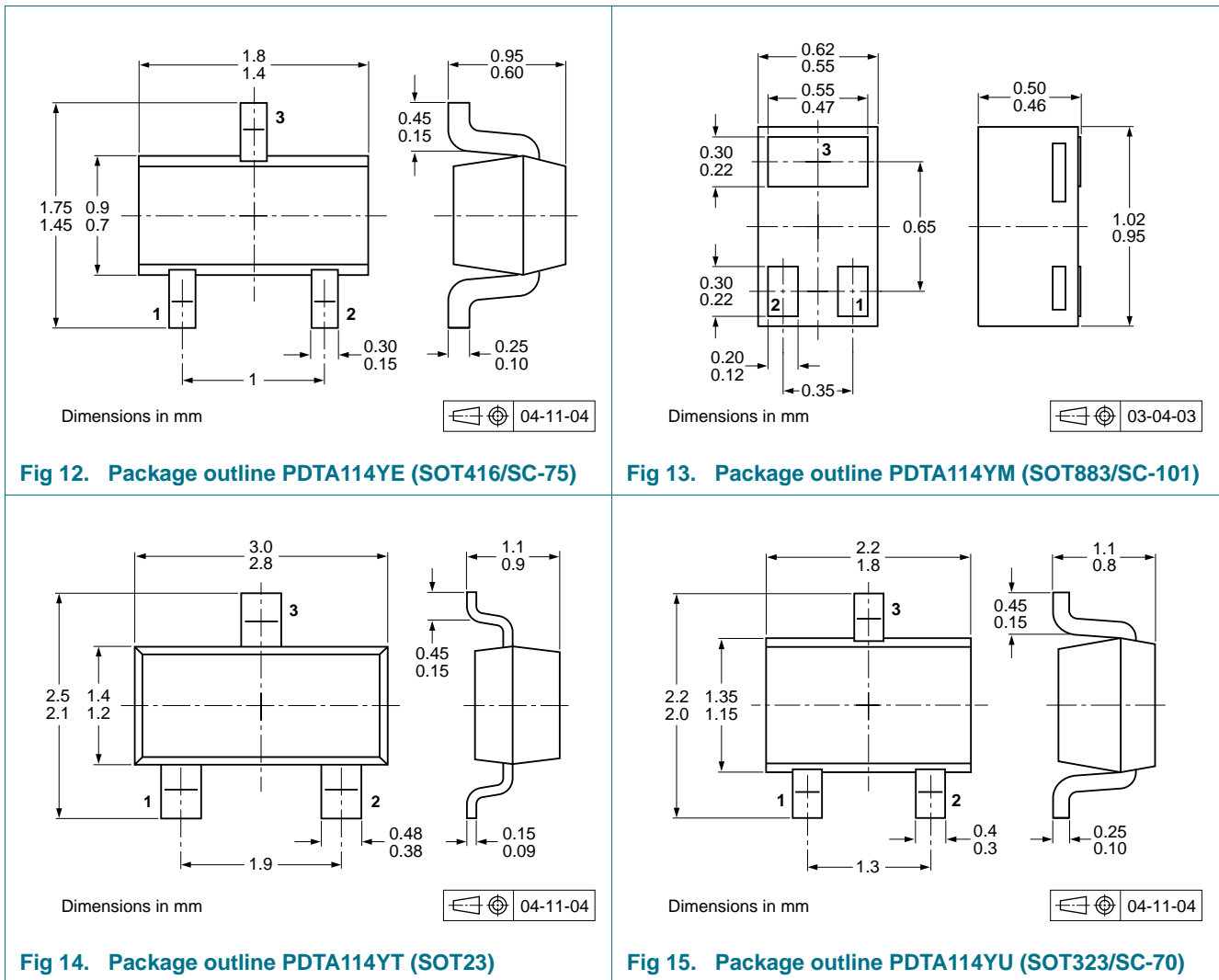
Fig 11. Transition frequency as a function of collector current; typical values of built-in transistor

8. Test information

8.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

9. Package outline



10. Packing information

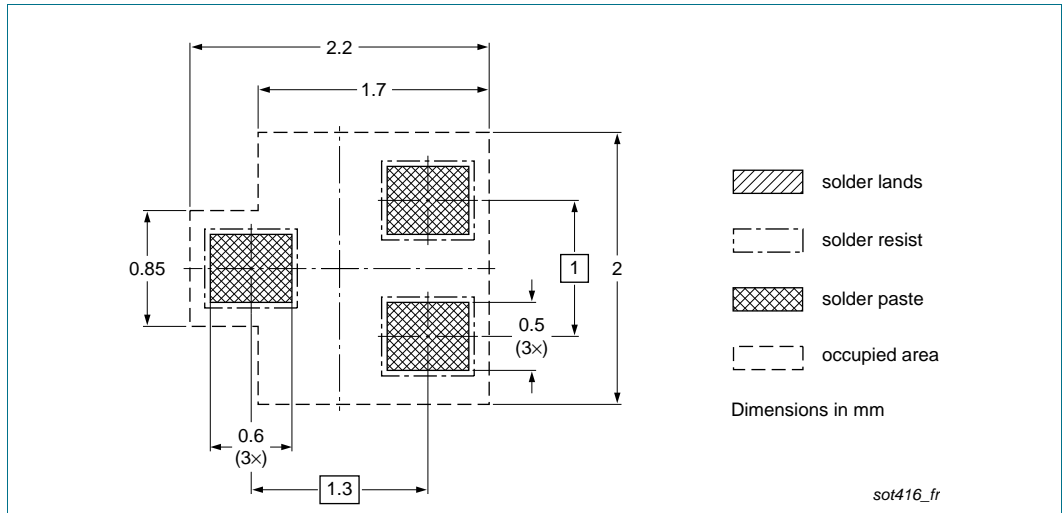
Table 9. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code.^[1]

Type number	Package	Description	Packing quantity		
			3000	5000	10000
PDTA114YE	SOT416	4 mm pitch, 8 mm tape and reel	-115	-	-135
PDTA114YM	SOT883	2 mm pitch, 8 mm tape and reel	-	-	-315
PDTA114YT	SOT23	4 mm pitch, 8 mm tape and reel	-215	-	-235
PDTA114YU	SOT323	4 mm pitch, 8 mm tape and reel	-115	-	-135

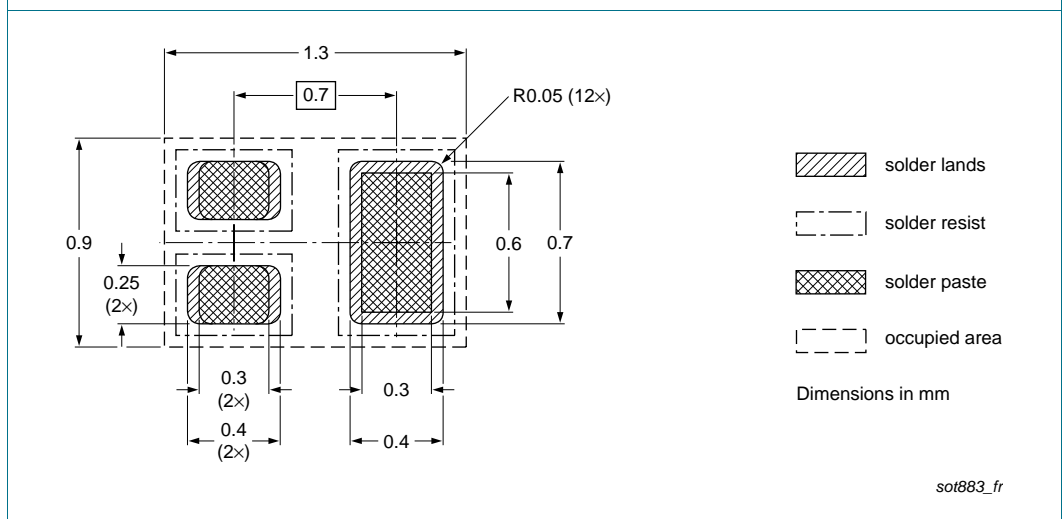
[1] For further information and the availability of packing methods, see [Section 14](#).

11. Soldering



Reflow soldering is the only recommended soldering method.

Fig 16. Reflow soldering footprint PDTA114YE (SOT416/SC-75)



Reflow soldering is the only recommended soldering method.

Fig 17. Reflow soldering footprint PDTA114YM (SOT883/SC-101)

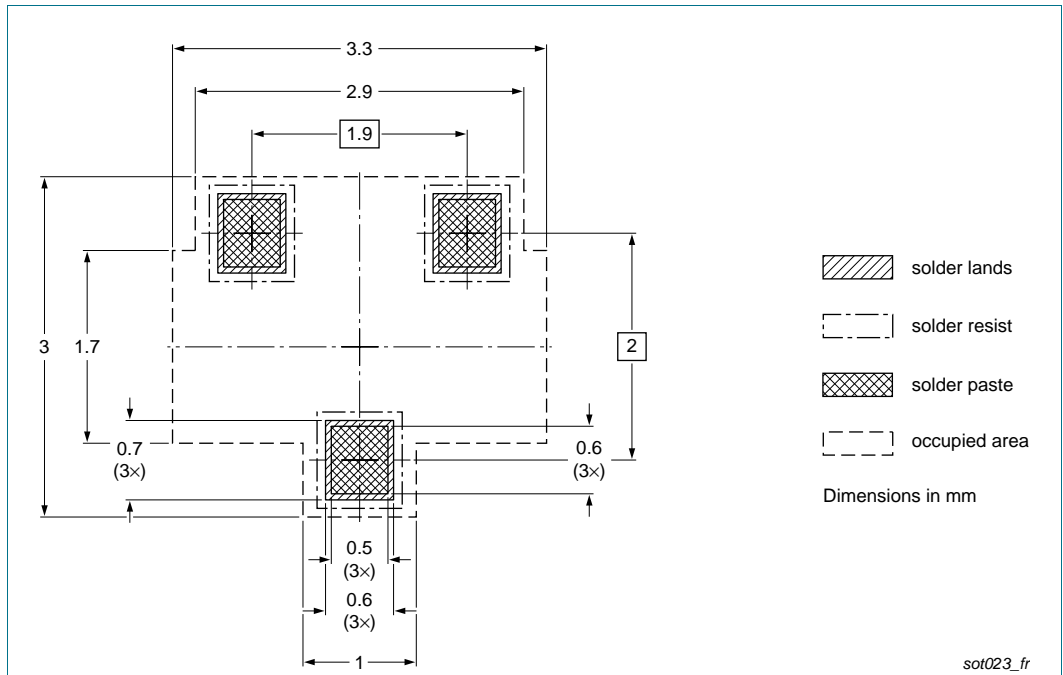


Fig 18. Reflow soldering footprint PDTA114YT (SOT23)

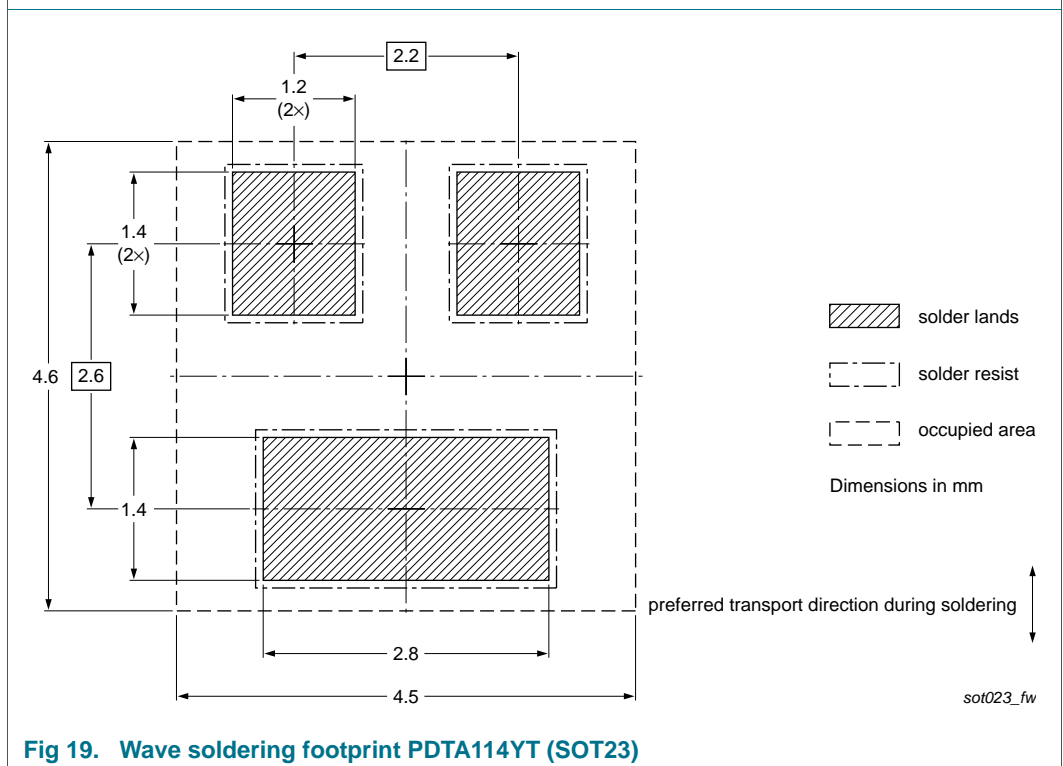


Fig 19. Wave soldering footprint PDTA114YT (SOT23)

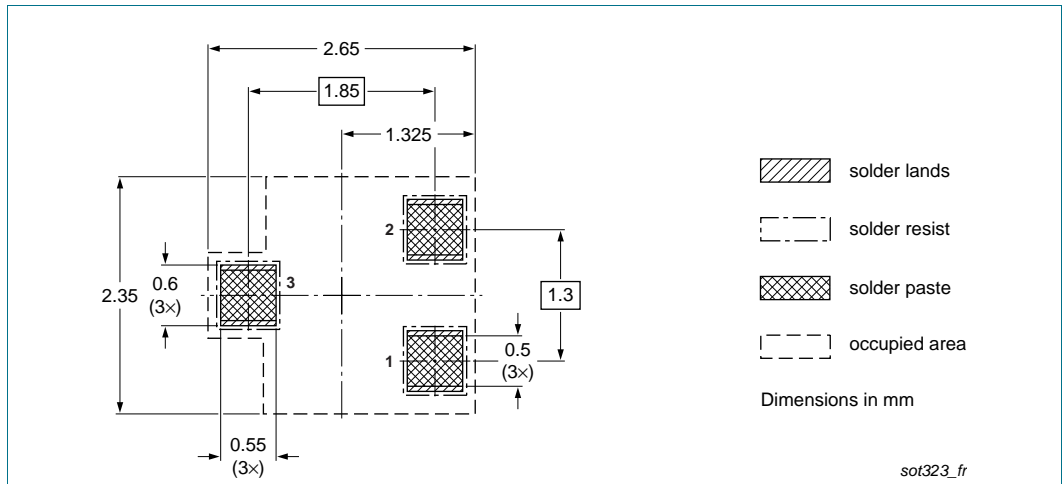


Fig 20. Reflow soldering footprint PDTA114YU (SOT323/SC-70)

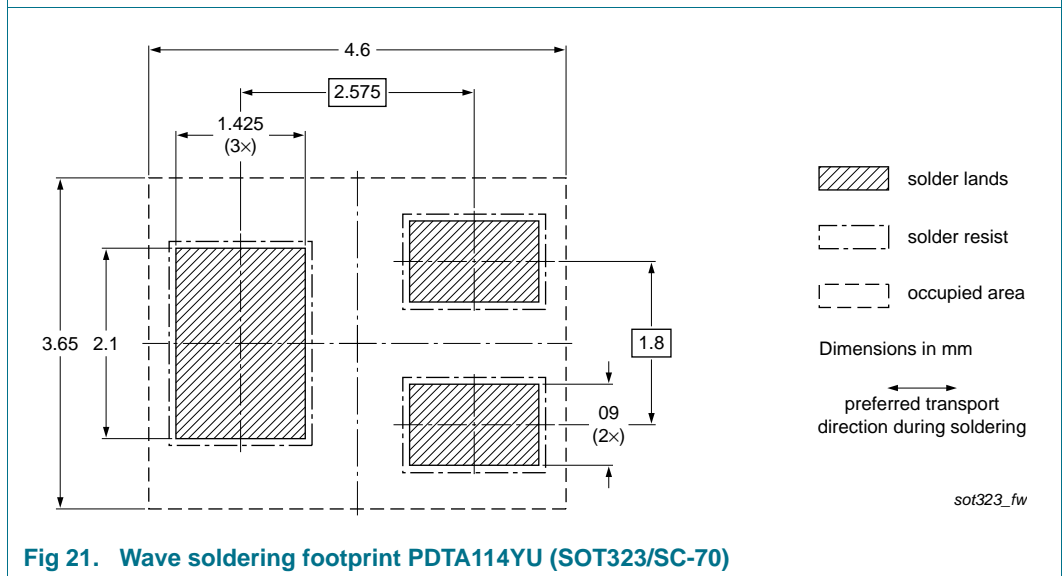


Fig 21. Wave soldering footprint PDTA114YU (SOT323/SC-70)

12. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PDTA114Y_SER v.5	20111118	Product data sheet	-	PDTA114Y_SERIES v.4
Modifications:	<ul style="list-style-type: none"> • The format of this document has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Type numbers PDTA114YEF, PDTA114YK and PDTA114YS removed. • Section 1 "Product profile": updated • Section 3 "Ordering information": added • Section 4 "Marking": updated • Figure 1 to 11: added • Section 5 "Limiting values": updated • Section 6 "Thermal characteristics": updated • Table 8 "Characteristics": $V_{i(on)}$ redefined to $V_{I(on)}$ on-state input voltage, $V_{i(off)}$ redefined to $V_{I(off)}$ off-state input voltage, I_{CEO} updated, f_T added • Section 8 "Test information": added • Section 9 "Package outline": superseded by minimized package outline drawings • Section 10 "Packing information": added • Section 11 "Soldering": added • Section 13 "Legal information": updated 			
PDTA114Y_SERIES v.4	20040802	Product data sheet	-	PDTA114Y_SERIES v.3
PDTA114Y_SERIES v.3	20030909	Product specification	-	PDTA114Y_SERIES v.2
PDTA114Y_SERIES v.2	20030411	Product specification	-	PDTA114YEF v.1
PDTA114YEF v.1	20020515	Product specification	-	-

13. Legal information

13.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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