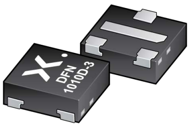


PDTA143X/123J/143Z/114YQA series

50 V, 100 mA PNP resistor-equipped transistors

Rev. 1 — 30 October 2015 | Product data sheet

1. Product profile

1.1 General description

100 mA PNP Resistor-Equipped Transistor (RET) family in a leadless ultra small DFN1010D-3 (SOT1215) Surface-Mounted Device (SMD) plastic package with visible and solderable side pads.

Table 1. Product overview

Type number	R1	R2	Package Nexperia	NPN complement
PDTA143XQA	4.7 kΩ	10 kΩ	DFN1010D-3 (SOT1215)	PDTC143XQA
PDTA123JQA	2.2 kΩ	47 kΩ		PDTC123JQA
PDTA143ZQA	4.7 kΩ	47 kΩ		PDTC143ZQA
PDTA114YQA	10 kΩ	47 kΩ		PDTC114YQA

1.2 Features and benefits

- 100 mA output current capability
- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduced pick and place costs
- Low package height of 0.37 mm
- AEC-Q101 qualified
- Suitable for Automatic Optical Inspection (AOI) of solder joint

1.3 Applications

- Digital applications
- Cost saving alternative for BC847/BC857 series in digital applications
- Controlling IC inputs
- Switching loads

1.4 Quick reference data

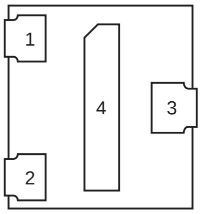
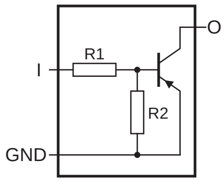
Table 2. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CEO}	collector-emitter voltage	open base	-	-	–50	V
I_O	output current		-	-	–100	mA

nexperia

2. Pinning information

Table 3. Pinning

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	I	input (base)	 Transparent top view	 aaa-019606
2	GND	GND (emitter)		
3	O	output (collector)		
4	O	output (collector)		

3. Ordering information

Table 4. Ordering information

Type number	Package		
	Name	Description	Version
PDTA143XQA	DFN1010D-3	plastic thermal enhanced ultra thin small outline package; no leads; 3 terminals; body: 1.1 × 1.0 × 0.37 mm	SOT1215
PDTA123JQA			
PDTA143ZQA			
PDTA114YQA			

4. Marking

Table 5. Marking codes

Type number	Marking code
PDTA143XQA	11 11 10
PDTA123JQA	11 00 01
PDTA143ZQA	11 01 01
PDTA114YQA	11 10 11

4.1 Binary marking code description

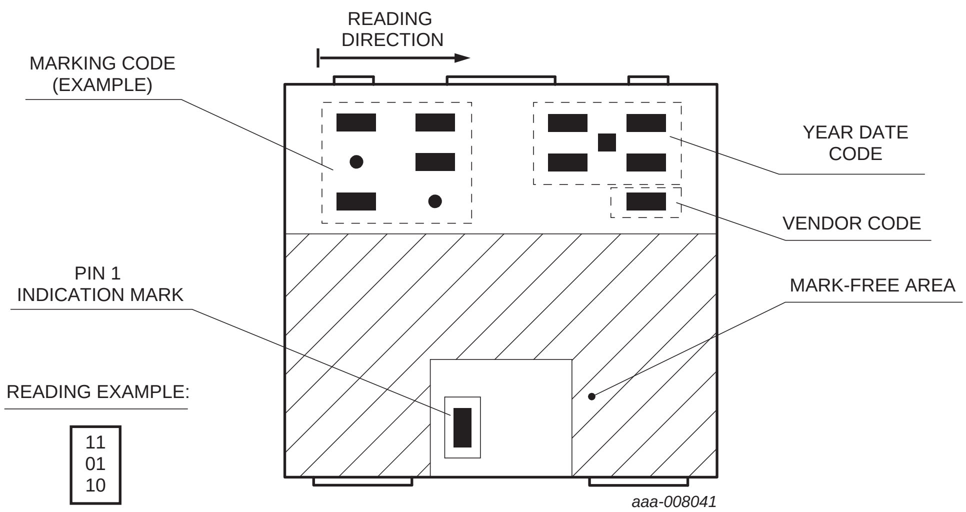


Fig 1. SOT1215 binary marking code description

5. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CBO}	collector-base voltage	open emitter	-	–50	V
V_{CEO}	collector-emitter voltage	open base	-	–50	V
V_{EBO}	emitter-base voltage				
	PDTA143XQA		-	–7	V
	PDTA123JQA		-	–5	V
	PDTA143ZQA		-	–5	V
	PDTA114YQA		-	–6	V

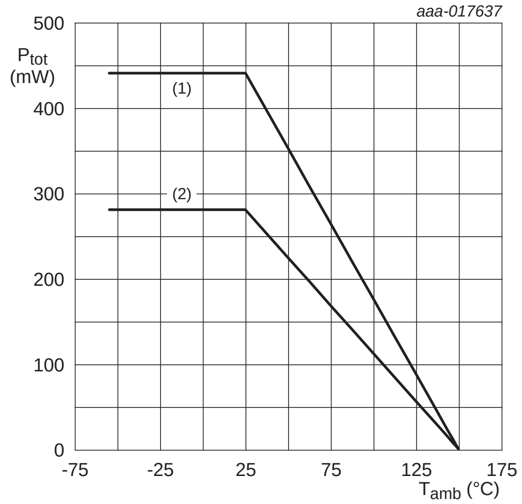
Table 6. Limiting values *...continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_I	input voltage					
	PDTA143XQA			–30	+7	V
	PDTA123JQA			–12	+5	V
	PDTA143ZQA			–30	+5	V
	PDTA114YQA			–40	+6	V
I_O	output current			-	–100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[1]	-	280	mW
			[2]	-	440	mW
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			–55	+150	°C
T_{stg}	storage temperature			–65	+150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, 4-layer copper, tin-plated and standard footprint.



(1) FR4 PCB, 4-layer copper, standard footprint

(2) FR4 PCB, standard footprint

Fig 2. Power derating curves

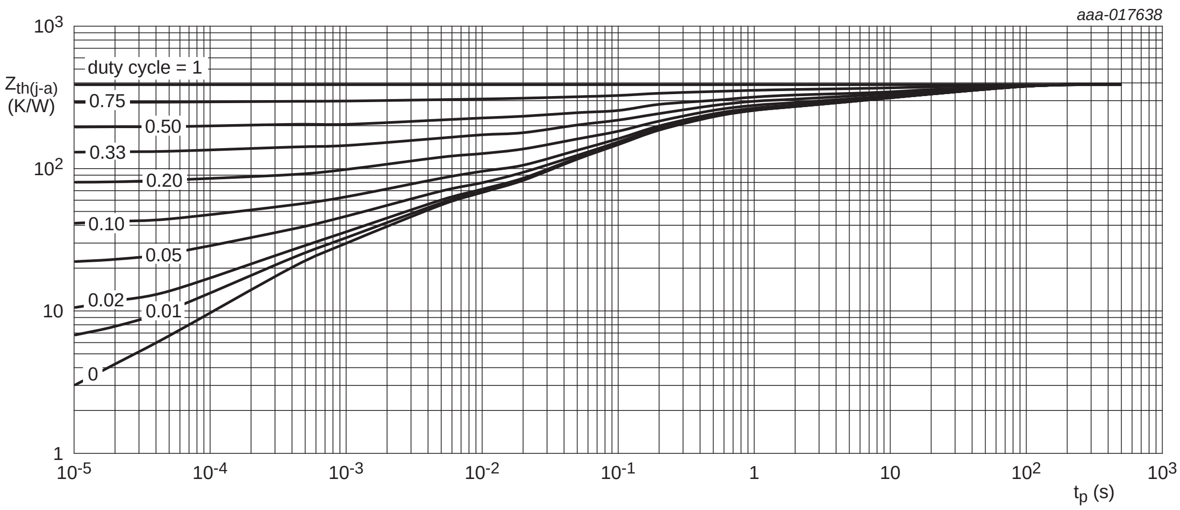
6. Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	446	K/W
			[2]	-	-	284	K/W

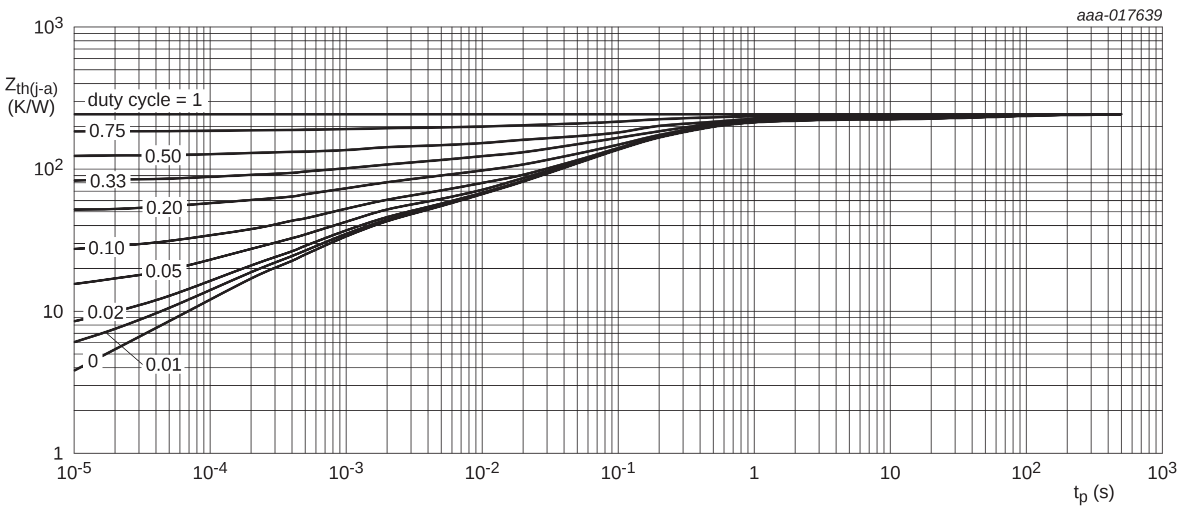
[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, 4-layer copper, tin-plated and standard footprint.



FR4 PCB, single-sided copper, tin-plated and standard footprint.

Fig 3. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, 4-layer copper, tin-plated and standard footprint.

Fig 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

7. Characteristics

Table 8. Characteristics

T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CBO}	collector-base cut-off current	V_{CB} = –50 V; I_E = 0 A	-	-	–100	nA
I_{CEO}	collector-emitter cut-off current	V_{CE} = –30 V; I_B = 0 A	-	-	–1	µA
		V_{CE} = –30 V; I_B = 0 A; T_j = 150 °C	-	-	–5	µA
I_{EBO}	emitter-base cut-off current					
	PDTA143XQA	V_{EB} = –5 V; I_C = 0 A	-	-	–600	µA
	PDTA123JQA		-	-	–180	µA
	PDTA143ZQA		-	-	–170	µA
	PDTA114YQA		-	-	–150	µA
h_{FE}	DC current gain					
	PDTA143XQA	V_{CE} = –5 V; I_C = –10 mA	50	-	-	
	PDTA123JQA	V_{CE} = –5 V; I_C = –10 mA	100	-	-	
	PDTA143ZQA	V_{CE} = –5 V; I_C = –10 mA	100	-	-	
	PDTA114YQA	V_{CE} = –5 V; I_C = –5 mA	100	-	-	
V_{CEsat}	collector-emitter saturation voltage					
	PDTA143XQA	I_C = –10 mA; I_B = –0.5 mA	-	-	–100	mV
	PDTA123JQA	I_C = –5 mA; I_B = –0.25 mA	-	-	–100	mV
	PDTA143ZQA	I_C = –5 mA; I_B = –0.25 mA	-	-	–100	mV
	PDTA114YQA	I_C = –5 mA; I_B = –0.25 mA	-	-	–100	mV
$V_{I(off)}$	off-state input voltage					
	PDTA143XQA	V_{CE} = –5 V; I_C = –100 µA	-	–0.9	–0.3	V
	PDTA123JQA		-	–0.6	–0.5	V
	PDTA143ZQA		-	–0.6	–0.5	V
	PDTA114YQA		-	–0.7	–0.5	V
$V_{I(on)}$	on-state input voltage					
	PDTA143XQA	V_{CE} = –0.3 V; I_C = –20 mA	–2.5	–1.5	-	V
	PDTA123JQA	V_{CE} = –0.3 V; I_C = –5 mA	–1.1	–0.75	-	V
	PDTA143ZQA	V_{CE} = –0.3 V; I_C = –5 mA	–1.3	–0.9	-	V
	PDTA114YQA	V_{CE} = –0.3 V; I_C = –1 mA	–1.4	–0.8	-	V
R1	bias resistor 1 (input)	[1]				
	PDTA143XQA		3.3	4.7	6.1	kΩ
	PDTA123JQA		1.54	2.2	2.86	kΩ
	PDTA143ZQA		3.3	4.7	6.1	kΩ
	PDTA114YQA		7	10	13	kΩ

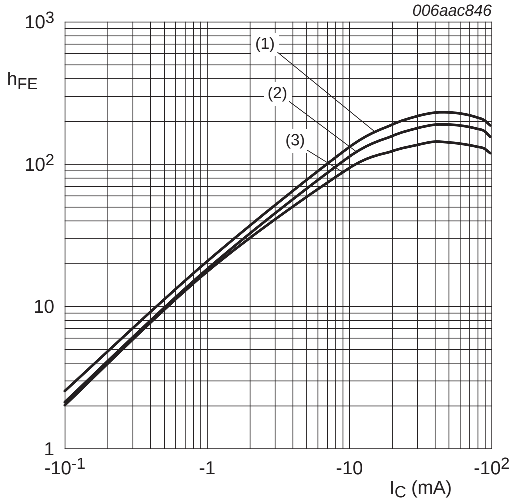
Table 8. Characteristics *...continued*

T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R2/R1	bias resistor ratio	[1]				
	PDTA143XQA		1.7	2.1	2.6	
	PDTA123JQA		17	21	26	
	PDTA143ZQA		8	10	12	
	PDTA114YQA		3.7	4.7	5.7	
C_c	collector capacitance	V_{CB} = −10 V; I_E = i_e = 0 A; f = 1 MHz	-	-	3	pF
f_T	transition frequency	V_{CE} = −5 V; I_C = −10 mA; f = 100 MHz [2]	-	180	-	MHz

[1] See Section 8 "Test information" for resistor calculation and test conditions.

[2] Characteristics of built-in transistor.



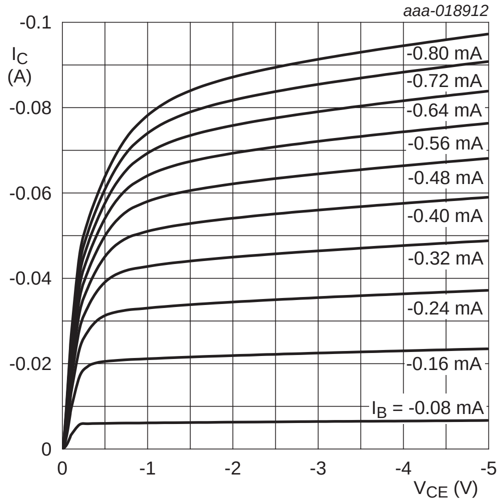
V_{CE} = –5 V

(1) T_{amb} = 100 °C

(2) T_{amb} = 25 °C

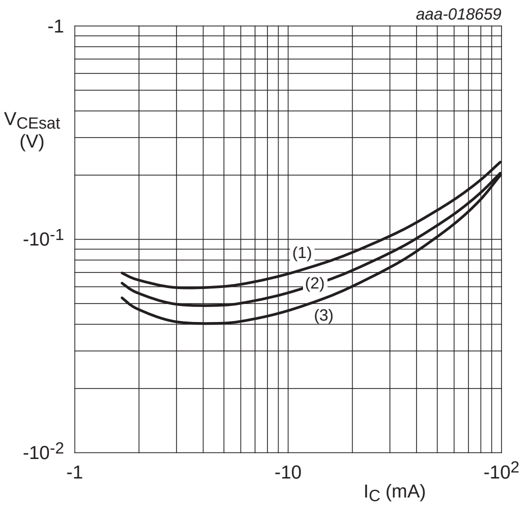
(3) T_{amb} = –40 °C

Fig 5. PDTA143XQA: DC current gain as a function of collector current; typical values



T_{amb} = 25 °C

Fig 6. PDTA143XQA: Collector current as a function of collector-emitter voltage; typical values



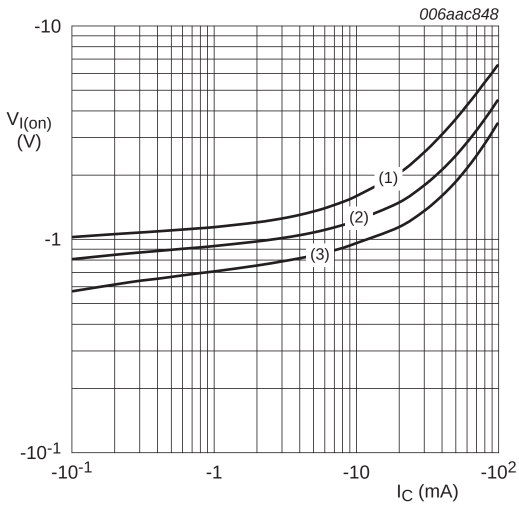
I_C/I_B = 20

(1) T_{amb} = 100 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = –40 °C

Fig 7. PDTA143XQA: Collector-emitter saturation voltage as a function of collector current; typical values



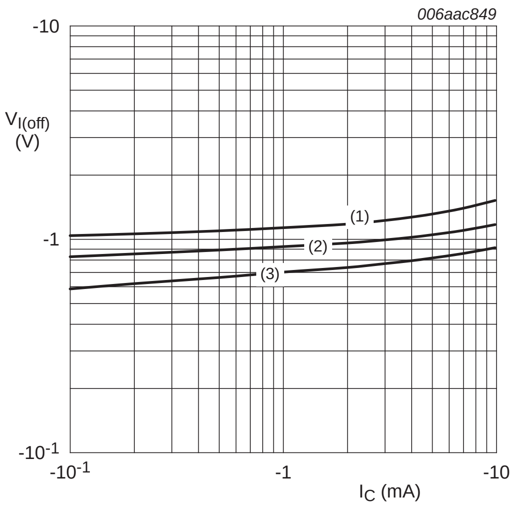
V_{CE} = –0.3 V

(1) T_{amb} = –40 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = 100 °C

Fig 8. PDTA143XQA: On-state input voltage as a function of collector current; typical values



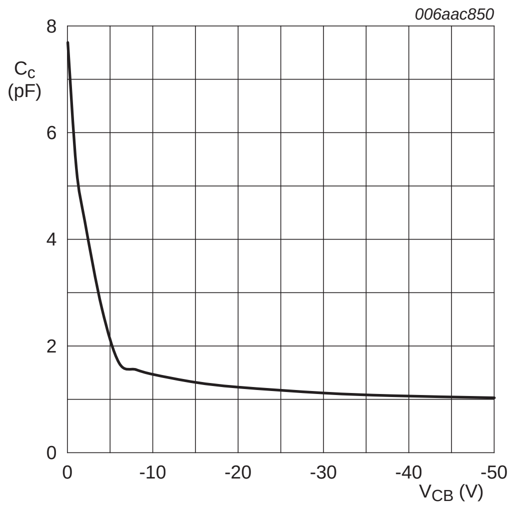
V_{CE} = –5 V

(1) T_{amb} = –40 °C

(2) T_{amb} = 25 °C

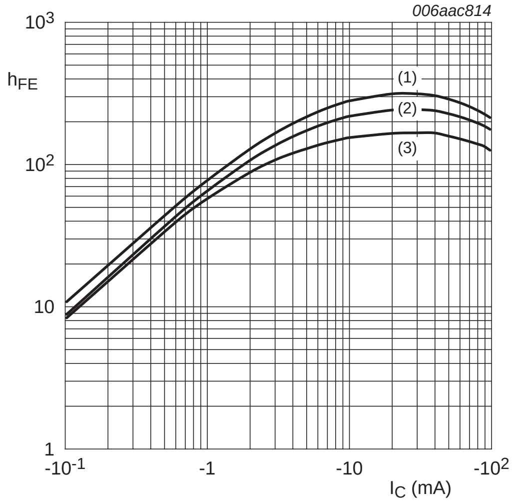
(3) T_{amb} = 100 °C

Fig 9. PDTA143XQA: Off-state input voltage as a function of collector current; typical values



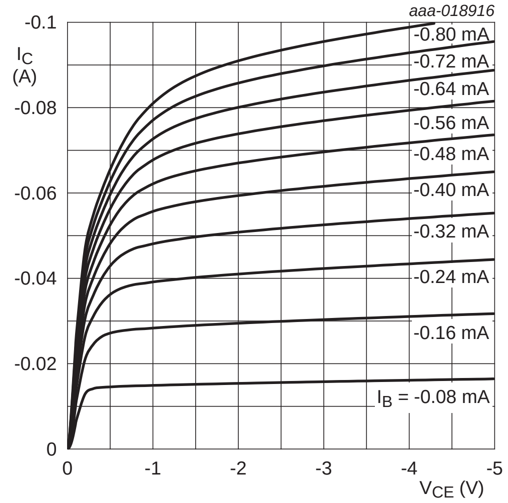
f = 1 MHz; T_{amb} = 25 °C

Fig 10. PDTA143XQA: Collector capacitance as a function of collector-base voltage; typical values



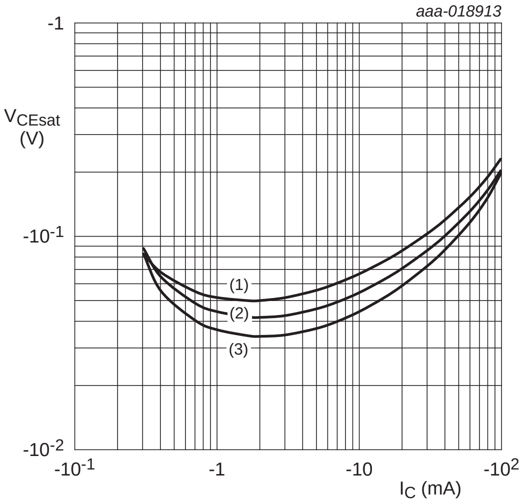
V_{CE} = –5 V
(1) T_{amb} = 100 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = –40 °C

Fig 11. PDTA123JQA: DC current gain as a function of collector current; typical values



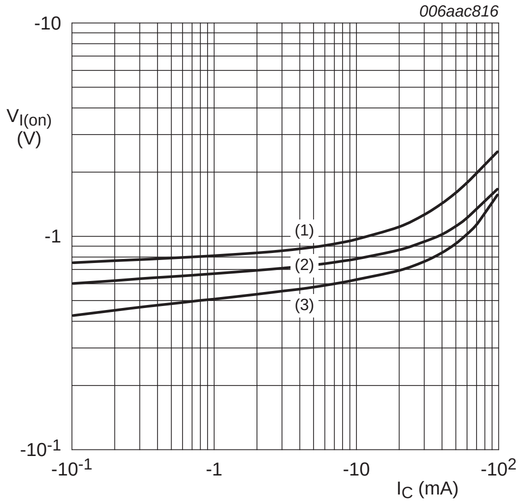
T_{amb} = 25 °C

Fig 12. PDTA123JQA: Collector current as a function of collector-emitter voltage; typical values



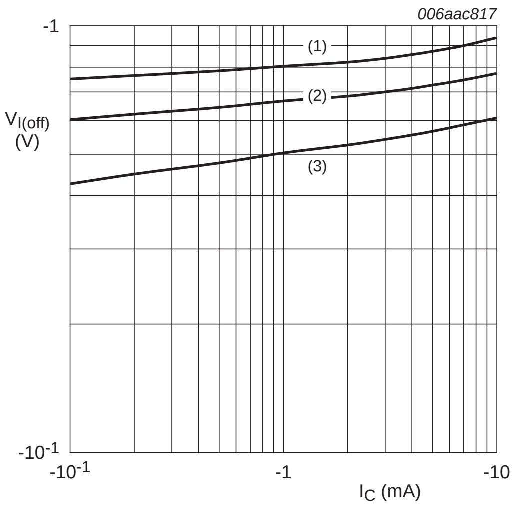
I_C/I_B = 20
(1) T_{amb} = 100 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = –40 °C

Fig 13. PDTA123JQA: Collector-emitter saturation voltage as a function of collector current; typical values



V_{CE} = –0.3V
(1) T_{amb} = –40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 100 °C

Fig 14. PDTA123JQA: On-state input voltage as a function of collector current; typical values



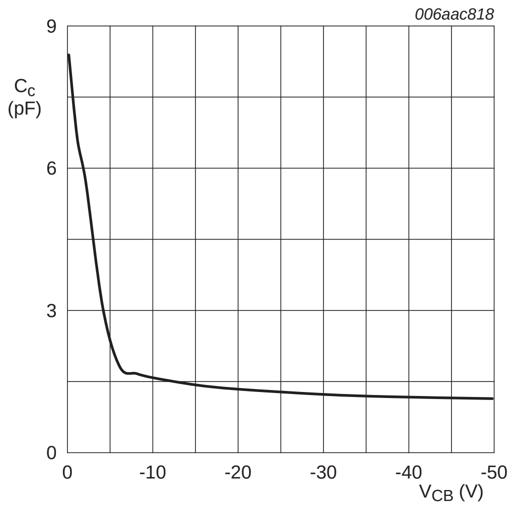
V_{CE} = –5 V

(1) T_{amb} = –40 °C

(2) T_{amb} = 25 °C

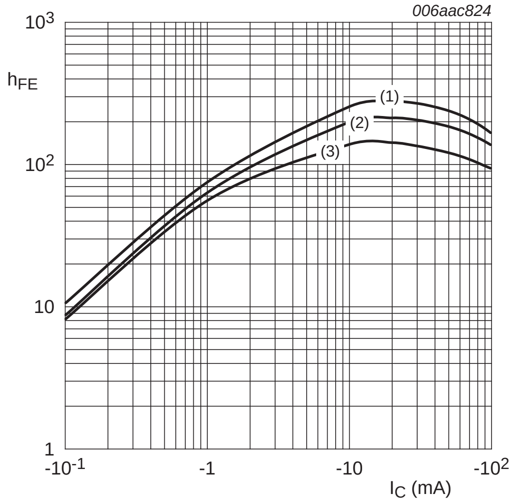
(3) T_{amb} = 100 °C

Fig 15. PDTA123JQA: Off-state input voltage as a function of collector current; typical values



f = 1 MHz; T_{amb} = 25 °C

Fig 16. PDTA123JQA: Collector capacitance as a function of collector-base voltage; typical values



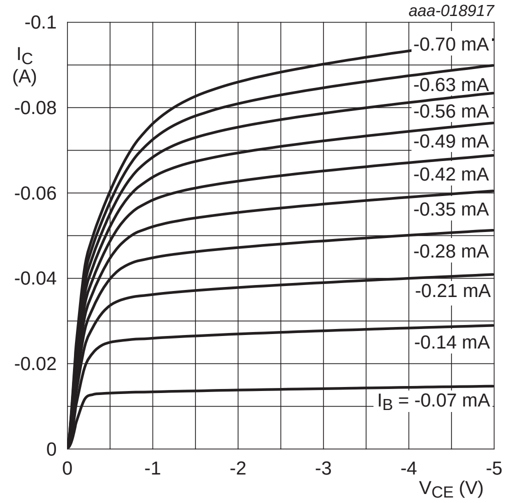
V_{CE} = –5 V

(1) T_{amb} = 100 °C

(2) T_{amb} = 25 °C

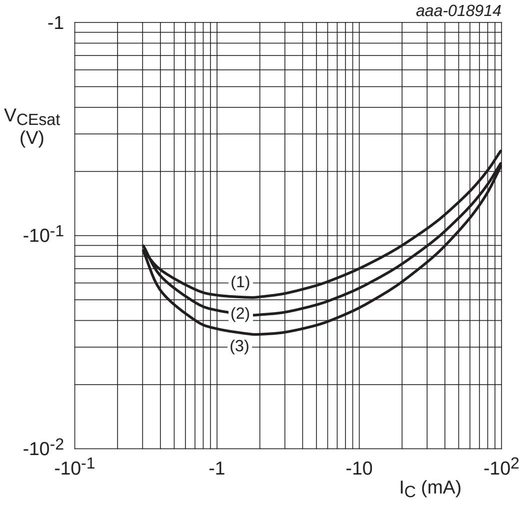
(3) T_{amb} = –40 °C

Fig 17. PDTA143ZQA: DC current gain as a function of collector current; typical values



T_{amb} = 25 °C

Fig 18. PDTA143ZQA: Collector current as a function of collector-emitter voltage; typical values



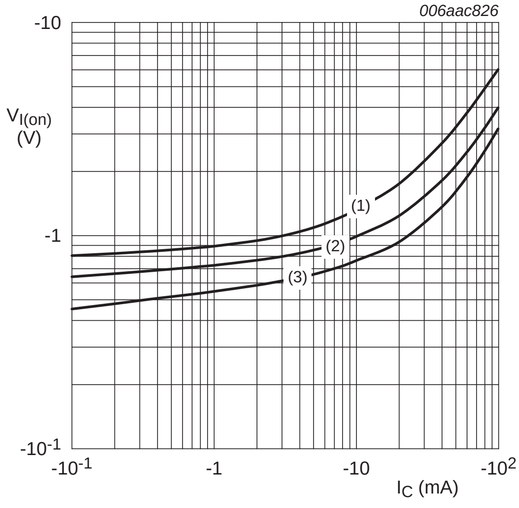
I_C/I_B = 20

(1) T_{amb} = 100 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = –40 °C

Fig 19. PDTA143ZQA: Collector-emitter saturation voltage as a function of collector current; typical values



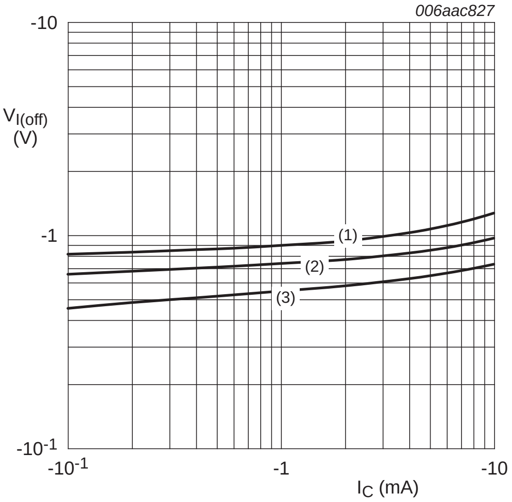
V_{CE} = –0.3 V

(1) T_{amb} = –40 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = 100 °C

Fig 20. PDTA143ZQA: On-state input voltage as a function of collector current; typical values



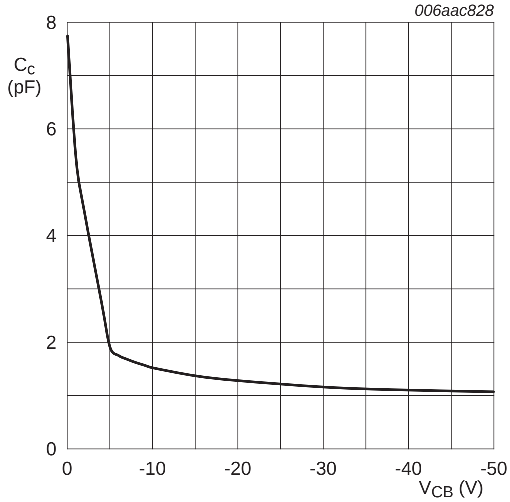
$V_{CE} = -5$ V

(1) $T_{amb} = -40$ °C

(2) $T_{amb} = 25$ °C

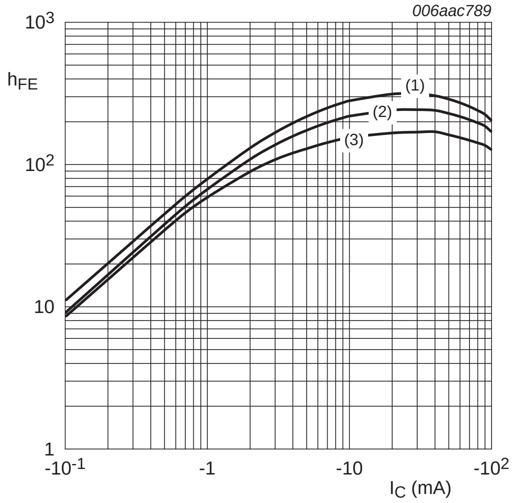
(3) $T_{amb} = 100$ °C

Fig 21. PDTA143ZQA: Off-state input voltage as a function of collector current; typical values



f = 1 MHz; $T_{amb} = 25$ °C

Fig 22. PDTA143ZQA: Collector capacitance as a function of collector-base voltage; typical values



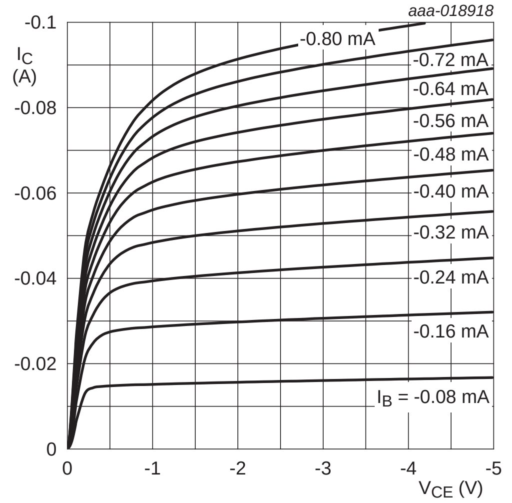
V_{CE} = –5 V

(1) T_{amb} = 100 °C

(2) T_{amb} = 25 °C

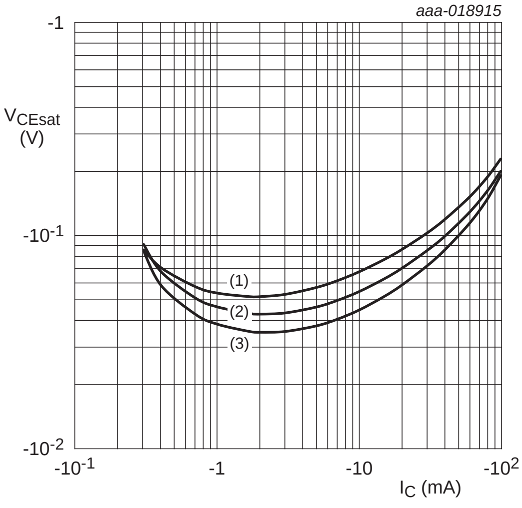
(3) T_{amb} = –40 °C

Fig 23. PDTA114YQA: DC current gain as a function of collector current; typical values



T_{amb} = 25 °C

Fig 24. PDTA114YQA: Collector current as a function of collector-emitter voltage; typical values



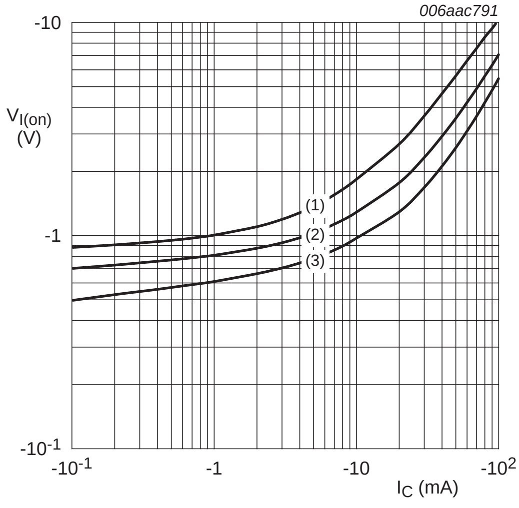
I_C/I_B = 20

(1) T_{amb} = 100 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = –40 °C

Fig 25. PDTA114YQA: Collector-emitter saturation voltage as a function of collector current; typical values



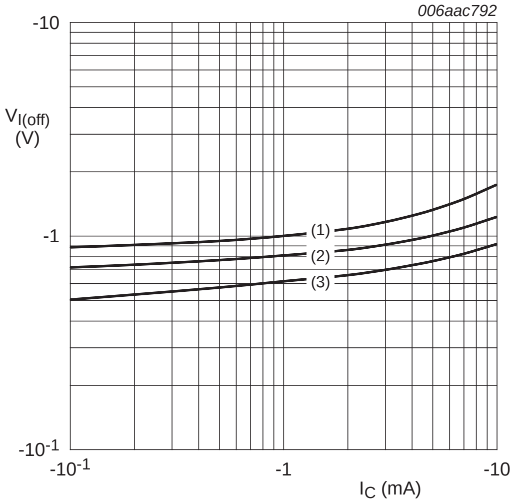
V_{CE} = –0.3 V

(1) T_{amb} = –40 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = 100 °C

Fig 26. PDTA114YQA: On-state input voltage as a function of collector current; typical values



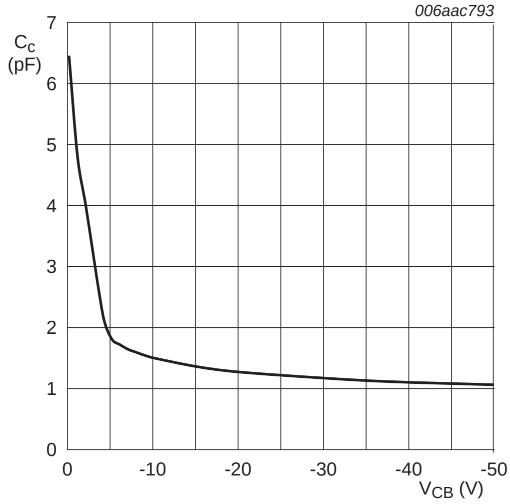
V_{CE} = –5 V

(1) T_{amb} = –40 °C

(2) T_{amb} = 25 °C

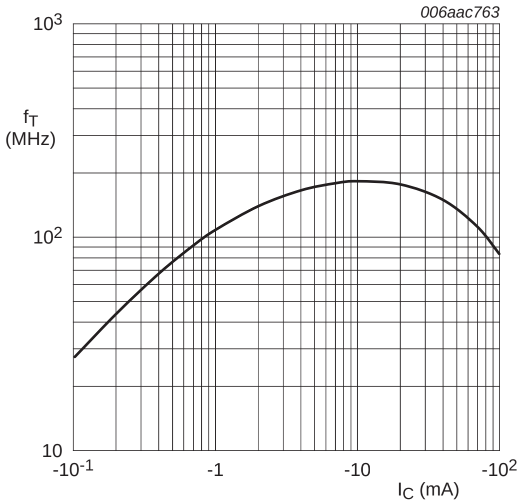
(3) T_{amb} = 100 °C

Fig 27. PDTA114YQA: Off-state input voltage as a function of collector current; typical values



f = 1 MHz; T_{amb} = 25 °C

Fig 28. PDTA114YQA: Collector capacitance as a function of collector-base voltage; typical values



V_{CE} = –5 V; T_{amb} = 25 °C

Fig 29. Transition frequency as a function of collector current; typical values of built-in transistor

8. Test information

8.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

8.2 Resistor calculation

- Calculation of bias resistor 1 (R1):

$$R1 = \frac{V(I_{I2}) - V(I_{I1})}{I_{I2} - I_{I1}}$$

- Calculation of bias resistor ratio (R2/R1):

$$\frac{R2}{R1} = \frac{V(I_{I4}) - V(I_{I3})}{R1 \cdot (I_{I4} - I_{I3})} - 1$$

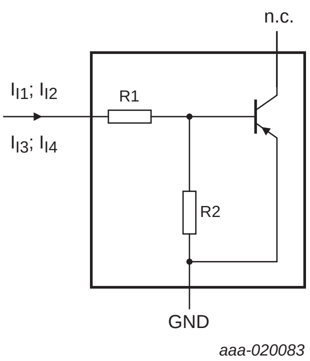


Fig 30. Resistor test circuit

8.3 Resistor test conditions

Table 9. Resistor test conditions

Type number	R1 (kΩ)	R2 (kΩ)	Test conditions			
			I_{I1}	I_{I2}	I_{I3}	I_{I4}
PDTA143XQA	4.7	10	–350 µA	–450 µA	350 µA	450 µA
PDTA123JQA	2.2	47	–90 µA	–140 µA	55 µA	105 µA
PDTA143ZQA	4.7	47	–90 µA	–140 µA	55 µA	105 µA
PDTA114YQA	10	47	–90 µA	–140 µA	55 µA	105 µA

9. Package outline

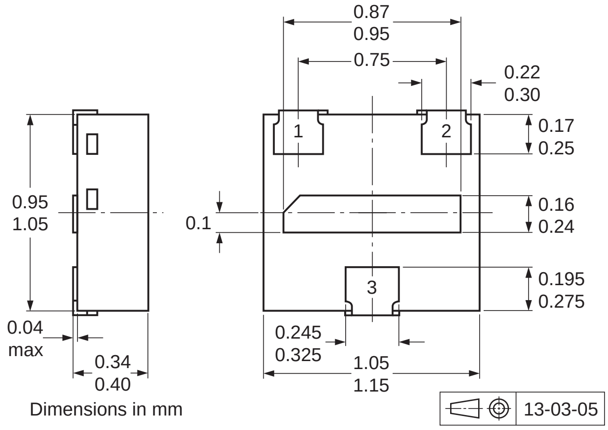


Fig 31. Package outline DFN1010D-3 (SOT1215)

10. Soldering

Footprint information for reflow soldering of DFN1010D-3 package **SOT1215**

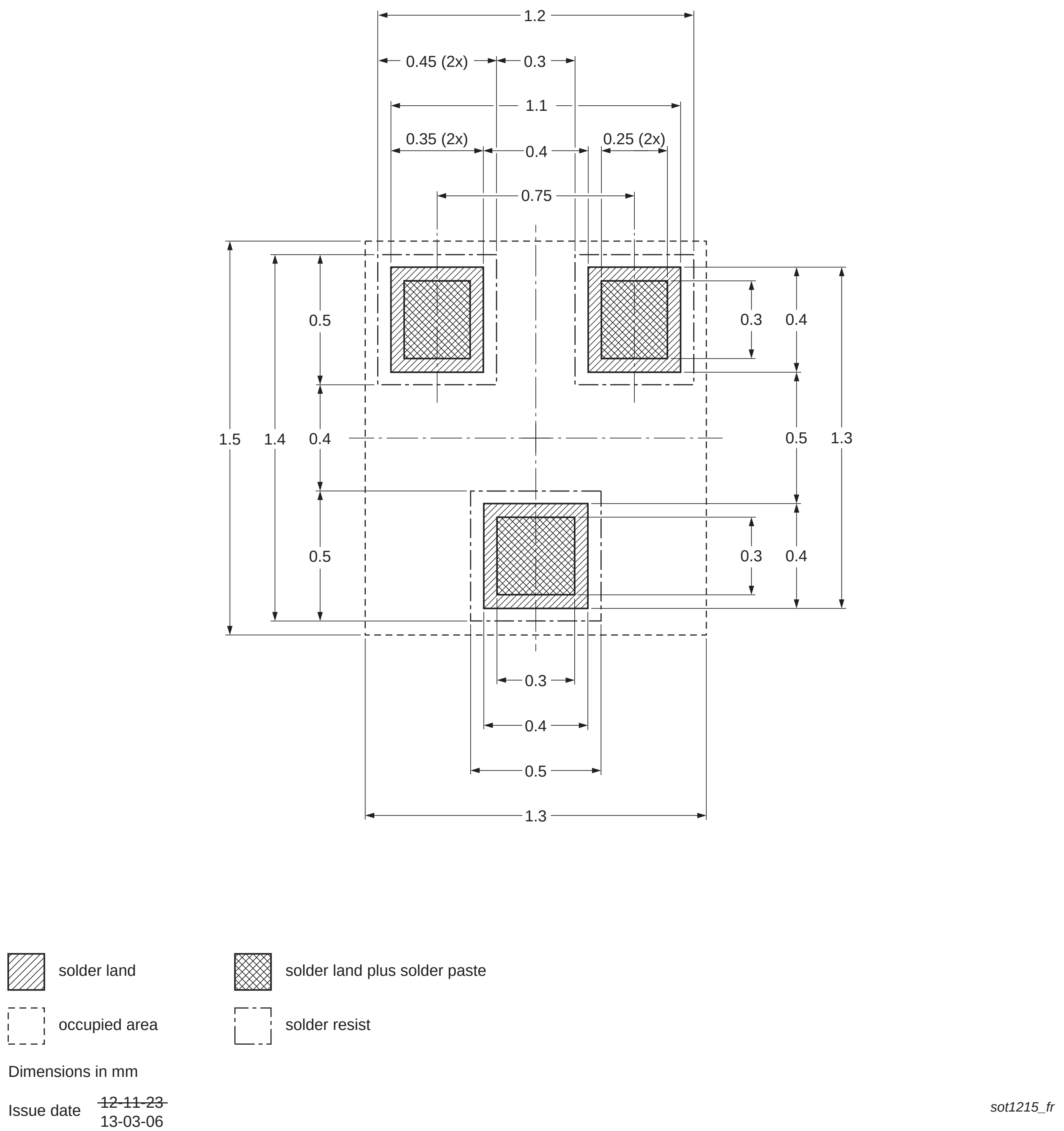


Fig 32. Reflow soldering footprint DFN1010D-3 (SOT1215)

11. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PDTA143X_123J_143Z_ 114YQA_SER v.1	20151030	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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14. Contents

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