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Team Nexperia



NPN resistor-equipped transistor; $R1 = 2.2 \text{ k}\Omega$, $R2 = 2.2 \text{ k}\Omega$ Rev. 1 — 3 April 2012 Product data sh

Product data sheet

Product profile 1.

1.1 General description

NPN Resistor-Equipped Transistor (RET) in a leadless ultra small DFN1006B-3 (SOT883B) Surface-Mounted Device (SMD) plastic package.

PNP complement: PDTA123EMB.

1.2 Features and benefits

- 100 mA output current capability
- Reduces component count
- Built-in bias resistors
- Reduces pick and place costs

1.3 Applications

Quick reference date

Table 4

- Low-current peripheral driver
- Control of IC inputs

- Simplifies circuit design
- AEC-Q101 qualified
- Leadless ultra small SMD plastic package
- Low package height of 0.37 mm
- Replaces general-purpose transistors in digital applications
- Mobile applications

1.4 Quick reference data

Table 1.	Quick reference data					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{CEO}	collector-emitter voltage	open base	-	-	50	V
lo	output current		-	-	100	mA
R1	bias resistor 1 (input)	T _{amb} = 25 °C	1.54	2.2	2.86	kΩ
R2/R1	bias resistor ratio		0.8	1	1.2	



NPN resistor-equipped transistor; R1 = 2.2 k Ω , R2 = 2.2 k Ω

2. Pinning information

Table 2.	Pinning	j information		
Pin	Symbol	Description	Simplified outline	Graphic symbol
1	I	input (base)		
2	G	GND (emitter)		3
3	0	output (collector)	2 Transparent top view SOT883B (DFN1006B-3)	1 R1 R2 2 sym007

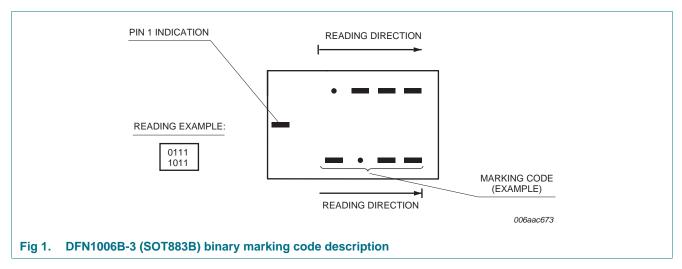
3. Ordering information

Table 3. Ordering information							
Type number	Package						
	Name	Description	Version				
PDTC123EMB	DFN1006B-3	Leadless ultra small plastic package; 3 solder lands; body 1.0 x 0.6 x 0.37 mm	SOT883B				

4. Marking

Table 4.	Marking codes	
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Type number	Marking code
PDTC123EMB	0011 0011



NPN resistor-equipped transistor; R1 = 2.2 k Ω , R2 = 2.2 k Ω

5. Limiting values

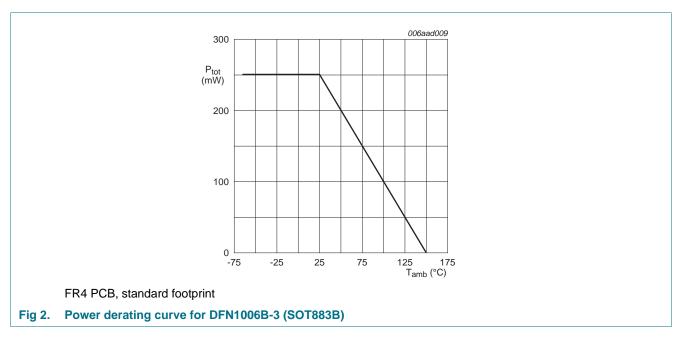
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Мах	Unit
V _{CBO}	collector-base voltage	open emitter		-	50	V
V _{CEO}	collector-emitter voltage	open base		-	50	V
V _{EBO}	emitter-base voltage	open collector		-	10	V
VI	input voltage	positive		-	12	V
		negative		-	-10	V
lo	output current			-	100	mA
I _{CM}	peak collector current	pulsed; t _p ≤ 1 ms		-	100	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	<u>[1][2]</u>	-	250	mW
Tj	junction temperature			-	150	°C
T _{amb}	ambient temperature			-65	150	°C
T _{stg}	storage temperature			-65	150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

[2] Reflow soldering is the only recommended soldering method.



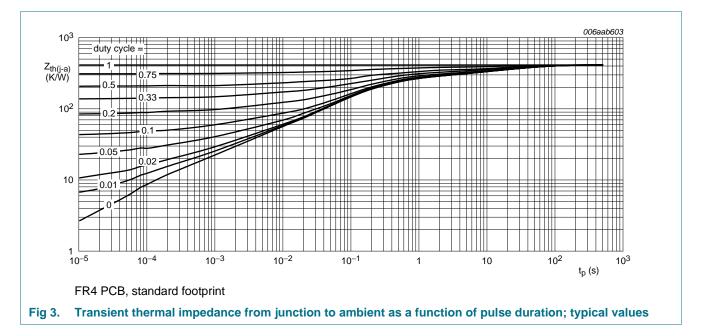
NPN resistor-equipped transistor; R1 = 2.2 k Ω , R2 = 2.2 k Ω

6. Thermal characteristics

Table 6.	Thermal characteristics						
Symbol	Parameter	Conditions		Min	Тур	Max	Unit
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1][2]	-	-	500	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Reflow soldering is the only recommended soldering method.

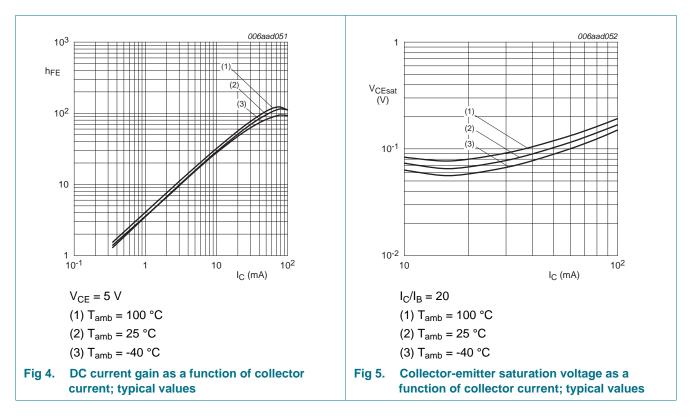


NPN resistor-equipped transistor; R1 = 2.2 k Ω , R2 = 2.2 k Ω

7. Characteristics

Table 7.	Characteristics						
Symbol	Parameter	Conditions		Min	Тур	Max	Unit
I _{CBO}	collector-base cut-off current	V_{CB} = 50 V; I _E = 0 A; T _{amb} = 25 °C		-	-	100	nA
I _{CEO}	collector-emitter cut-off	$V_{CE}=30~V;~I_B=0~A;~T_{amb}=25~^\circ C$		-	-	1	μA
	current	$V_{CE} = 30 \text{ V}; \text{ I}_{B} = 0 \text{ A}; \text{ T}_{j} = 150 ^{\circ}\text{C}$		-	-	5	μA
I _{EBO}	emitter-base cut-off current	$V_{EB} = 5 \text{ V; } I_C = 0 \text{ A; } T_{amb} = 25 \text{ °C}$		-	-	2	mA
h _{FE}	DC current gain	V_{CE} = 5 V; I _C = 20 mA; T _{amb} = 25 °C		30	-	-	
V _{CEsat}	collector-emitter saturation voltage	I_C = 10 mA; I_B = 0.5 mA; T_{amb} = 25 °C		-	-	150	mV
V _{I(off)}	off-state input voltage	V_{CE} = 5 V; I _C = 1 mA; T _{amb} = 25 °C		-	1.2	0.5	V
V _{I(on)}	on-state input voltage	V_{CE} = 0.3 V; I _C = 20 mA; T _{amb} = 25 °C		2	1.6	-	V
R1	bias resistor 1 (input)	T _{amb} = 25 °C		1.54	2.2	2.86	kΩ
R2/R1	bias resistor ratio			0.8	1	1.2	
C _C	collector capacitance	$V_{CB} = 10 \text{ V}; I_E = 0 \text{ A}; i_e = 0 \text{ A};$ f = 1 MHz; T _{amb} = 25 °C		-	-	2.5	pF
f _T	transition frequency	V_{CE} = 5 V; I _C = 10 mA; f = 100 MHz; T _{amb} = 25 °C	<u>[1]</u>	-	230	-	MHz

[1] Characteristics of built-in transistor.

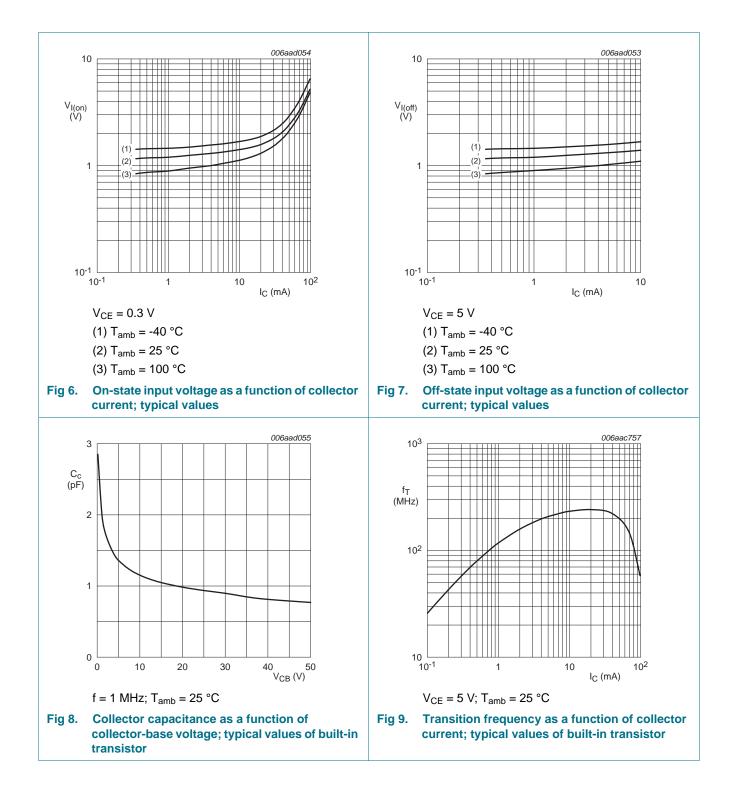


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NXP Semiconductors

PDTC123EMB

NPN resistor-equipped transistor; R1 = 2.2 k Ω , R2 = 2.2 k Ω



PDTC123EMB

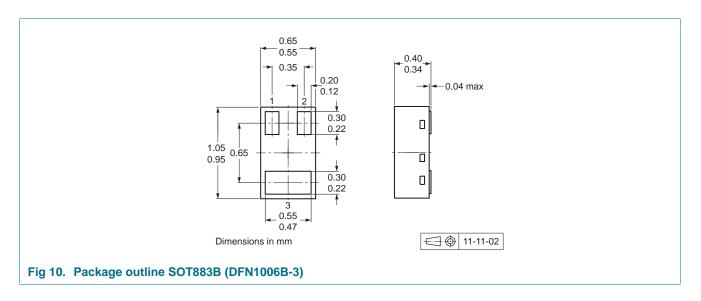
NPN resistor-equipped transistor; R1 = 2.2 k Ω , R2 = 2.2 k Ω

8. Test information

8.1 Quality information

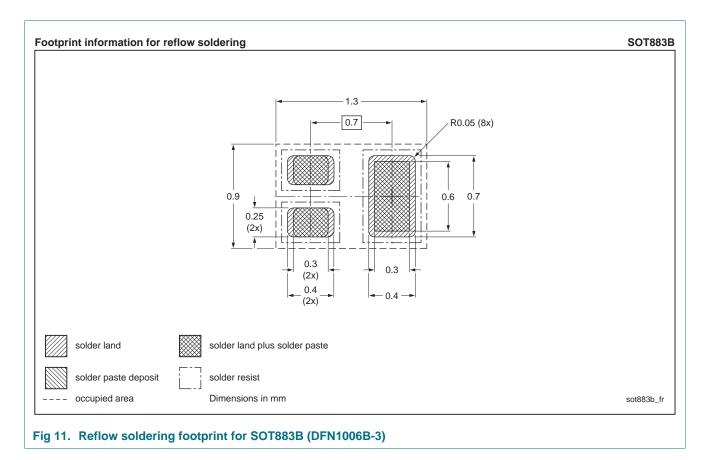
This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

9. Package outline



NPN resistor-equipped transistor; R1 = 2.2 k Ω , R2 = 2.2 k Ω

10. Soldering



NPN resistor-equipped transistor; R1 = 2.2 k Ω , R2 = 2.2 k Ω

11. Revision history

Table 8. Revision h	istory			
Document ID	Release date	Data sheet status	Change notice	Supersedes
PDTC123EMB v.1	20120403	Product data sheet	-	-

NPN resistor-equipped transistor; R1 = 2.2 k Ω , R2 = 2.2 k Ω

12. Legal information

12.1 Data sheet status

Document status ^[1] [2]	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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Product data sheet

PDTC123EMB

NPN resistor-equipped transistor; $R1 = 2.2 \text{ k}\Omega$, $R2 = 2.2 \text{ k}\Omega$

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PDTC123EMB

NPN resistor-equipped transistor; $R1 = 2.2 \text{ k}\Omega$, $R2 = 2.2 \text{ k}\Omega$

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