

PESDxUSB3S series

ESD protection for differential data lines

Rev. 4 — 30 January 2019

Product data sheet

1. Product profile

1.1. General description

The devices are ElectroStatic Discharge (ESD) protection for one, two and three differential channels.

The devices are footprint compatible to PCMFxUSB3S common mode filters with ESD protection.

Diodes provide protection to downstream components from ESD voltages up to ± 15 kV on each signal line.

Table 1. Product overview

| Type number | Number of channels | Package Name |
|-------------|--------------------|--------------|
| PESD1USB3S | 1 | WLCSP5 |
| PESD2USB3S | 2 | WLCSP10 |
| PESD3USB3S | 3 | WLCSP15 |

1.2. Features and benefits

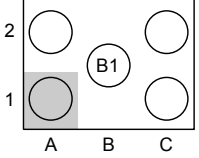
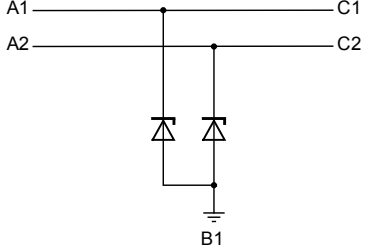
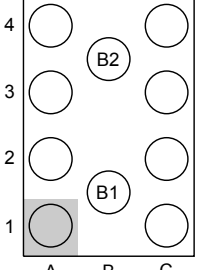
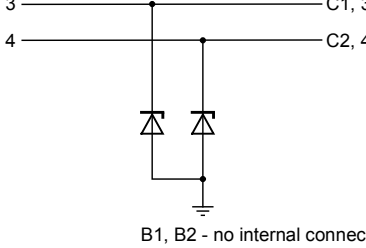
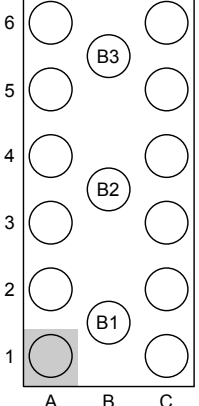
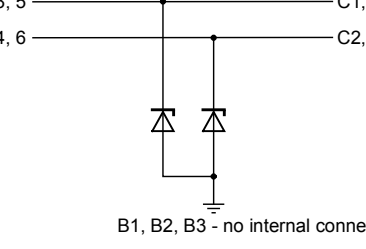
- Allows switching between PCMFxUSB3S common mode filters with ESD protection and PESDxUSB3S ESD protection in the same footprint
- TrEOS protection process for very high system-level ESD robustness: superior protection of sensitive Systems on Chips (SoCs)
- ESD protection for one, two and three differential channels up to ± 15 kV contact discharge according to IEC 61000-4-2
- Industry-standard WLCSP5, 10 and 15 packages for smallest footprint

1.3. Applications

- Smartphone, cellular and cordless phone
- USB3.1, USB2.0, HDMI2.0, HDMI1.4
- General-purpose downstream ESD protection for differential data lines
- Tablet PC and Mobile Internet Device (MID)
- MIPI D-PHY as used in Camera Serial Interface (CSI) and Display Serial Interface (DSI)

2. Pinning information

Table 2. Pinning

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----------------------------------|----------|----------------------|--|---|
| PESD1USB3S (WLCSP5_2-1-2) | | | | |
| A1 | CH1_IN+ | channel 1+, external |  <p>Transparent top view WLCSP5_2-1-2</p> |  <p>aaa-021381</p> |
| A2 | CH1_IN- | channel 1-, external | | |
| B1 | GND_CH1 | ground channel 1 | | |
| C1 | CH1_OUT+ | channel 1+, internal | | |
| C2 | CH1_OUT- | channel 1-, internal | | |
| PESD2USB3S (WLCSP10_4-2-4) | | | | |
| A1 | CH1_IN+ | channel 1+, external |  <p>Transparent top view WLCSP10_4-2-4</p> |  <p>B1, B2 - no internal connection aaa-021384</p> |
| A2 | CH1_IN- | channel 1-, external | | |
| A3 | CH2_IN+ | channel 2+, external | | |
| A4 | CH2_IN- | channel 2-, external | | |
| B1 | GND_CH1 | ground channel 1 | | |
| B2 | GND_CH2 | ground channel 2 | | |
| C1 | CH1_OUT+ | channel 1+, internal | | |
| C2 | CH1_OUT- | channel 1-, internal | | |
| C3 | CH2_OUT+ | channel 2+, internal | | |
| C4 | CH2_OUT- | channel 2-, internal | | |
| PESD3USB3S (WLCSP15_6-3-6) | | | | |
| A1 | CH1_IN+ | channel 1+, external |  <p>Transparent top view WLCSP15_6-3-6</p> |  <p>B1, B2, B3 - no internal connection aaa-021385</p> |
| A2 | CH1_IN- | channel 1-, external | | |
| A3 | CH2_IN+ | channel 2+, external | | |
| A4 | CH2_IN- | channel 2-, external | | |
| A5 | CH3_IN+ | channel 3+, external | | |
| A6 | CH3_IN- | channel 3-, external | | |
| B1 | GND_CH1 | ground channel 1 | | |
| B2 | GND_CH2 | ground channel 2 | | |
| B3 | GND_CH3 | ground channel 3 | | |
| C1 | CH1_OUT+ | channel 1+, internal | | |
| C2 | CH1_OUT- | channel 1-, internal | | |
| C3 | CH2_OUT+ | channel 2+, internal | | |
| C4 | CH2_OUT- | channel 2-, internal | | |
| C5 | CH3_OUT+ | channel 3+, internal | | |
| C6 | CH3_OUT- | channel 3-, internal | | |

3. Ordering information

Table 3. Ordering information

| Type number | Package | |
|-------------|---------|---|
| | Name | Description |
| PESD1USB3S | WLCSP5 | wafer level chip-size package; 5 bumps (2-1-2) |
| PESD2USB3S | WLCSP10 | wafer level chip-size package; 10 bumps (4-2-4) |
| PESD3USB3S | WLCSP15 | wafer level chip-size package; 15 bumps (6-3-6) |

4. Marking

Table 4. Marking codes

| Type number | Marking code |
|-------------|--------------|
| PESD1USB3S | PD1S |
| PESD2USB3S | PD2S |
| PESD3USB3S | PD3S |

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|---------------------------------|---|------|------|------|
| V_I | input voltage | | -0.5 | 5 | V |
| V_{ESD} | electrostatic discharge voltage | IEC 61000-4-2, level 4; all input pins to ground | | | |
| | | • contact discharge | -15 | 15 | kV |
| | | • air discharge | -15 | 15 | kV |
| | | IEC 61000-4-2, level 4; all output pins to ground | | | |
| | | • contact discharge | -2 | 2 | kV |
| | | • air discharge | -2 | 2 | kV |
| I_{PPM} | rated peak-pulse current | $t_p = 8/20 \mu s$ | -8 | 8 | A |
| T_{stg} | storage temperature | | -40 | +125 | °C |
| T_{amb} | ambient temperature | | -40 | +125 | °C |

6. Characteristics

6.1. Channel characteristics

Table 6. Channel characteristics

$T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------|-------------------------|--|-------|------|----------|----------|
| C_d | diode capacitance | $f = 1\text{ MHz}; V_1 = 2.5\text{ V}$ | [1] - | 0.45 | - | pF |
| I_{RM} | reverse leakage current | per line; $V_1 = 5\text{ V}$ | - | 1 | 100 | nA |
| V_{BR} | breakdown voltage | $I_R = 1\text{ mA}$ | 6 | 9 | - | V |
| V_F | forward voltage | $I_F = 10\text{ mA}$ | - | 0.8 | - | V |
| R_{dyn} | dynamic resistance | TLP | [2] | | | |
| | | • positive transient | - | 0.16 | - | Ω |
| | | • negative transient | - | 0.16 | - | Ω |
| | | surge | [3] | | | |
| | | • positive transient | - | 0.25 | - | Ω |
| | • negative transient | - | 0.25 | - | Ω | |

[1] This parameter is guaranteed by design.

[2] 100 ns Transmission Line Pulse (TLP); 50 Ω ; pulser at 70 to 90 ns.

[3] According to IEC 61000-4-5 (8/20 μs).

6.2. Frequency characteristics

Table 7. Frequency characteristics

$T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|-------------------|------------|-------|-----|-----|------|
| Differential mode: S_{dd21} | | | | | | |
| f_{-3dB} | cut-off frequency | | [1] - | 17 | - | GHz |

[1] Normalized to attenuation at 1 MHz.

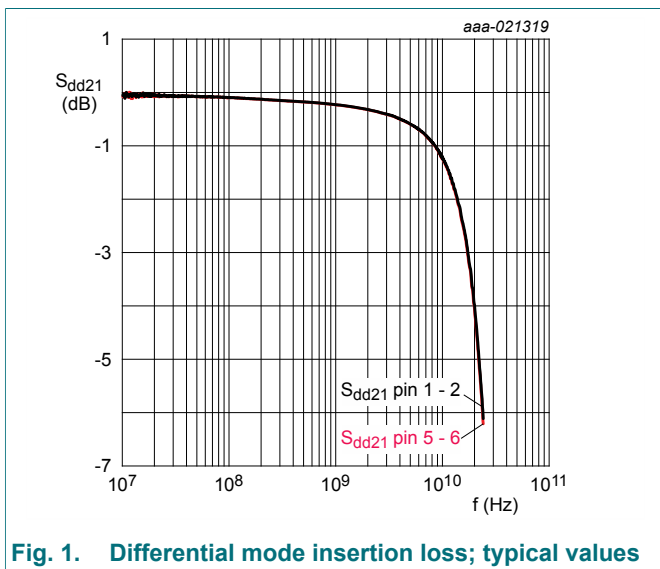


Fig. 1. Differential mode insertion loss; typical values

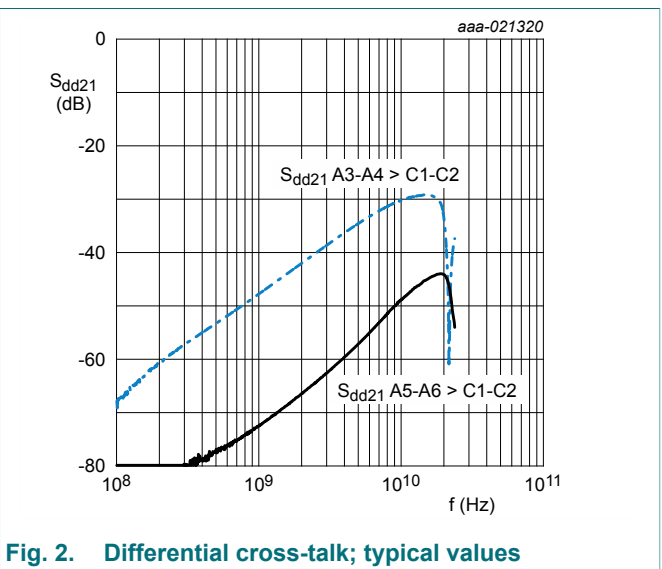


Fig. 2. Differential cross-talk; typical values

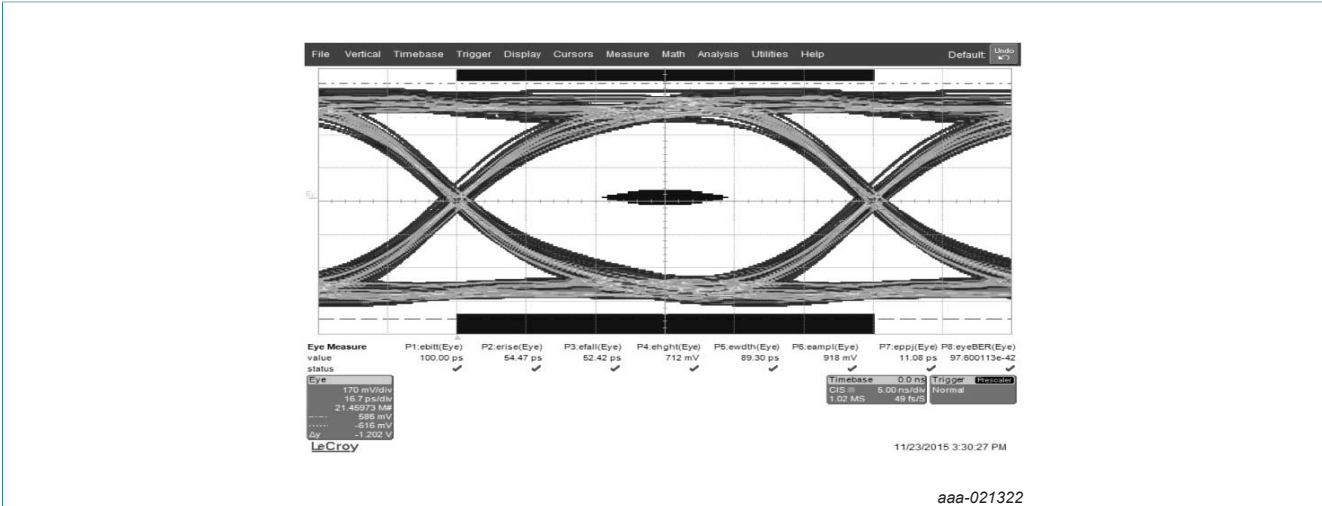
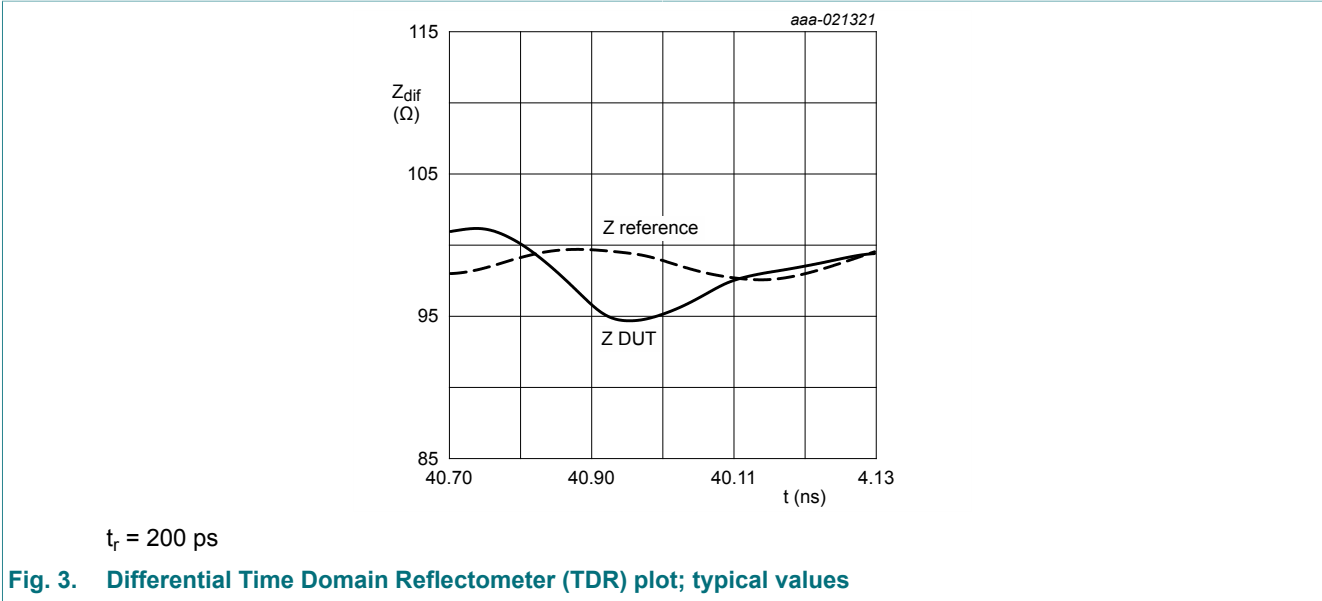


Fig. 4. USB3.1 eye diagram 10 Gbps, test board with PESD3USB3S; typical values

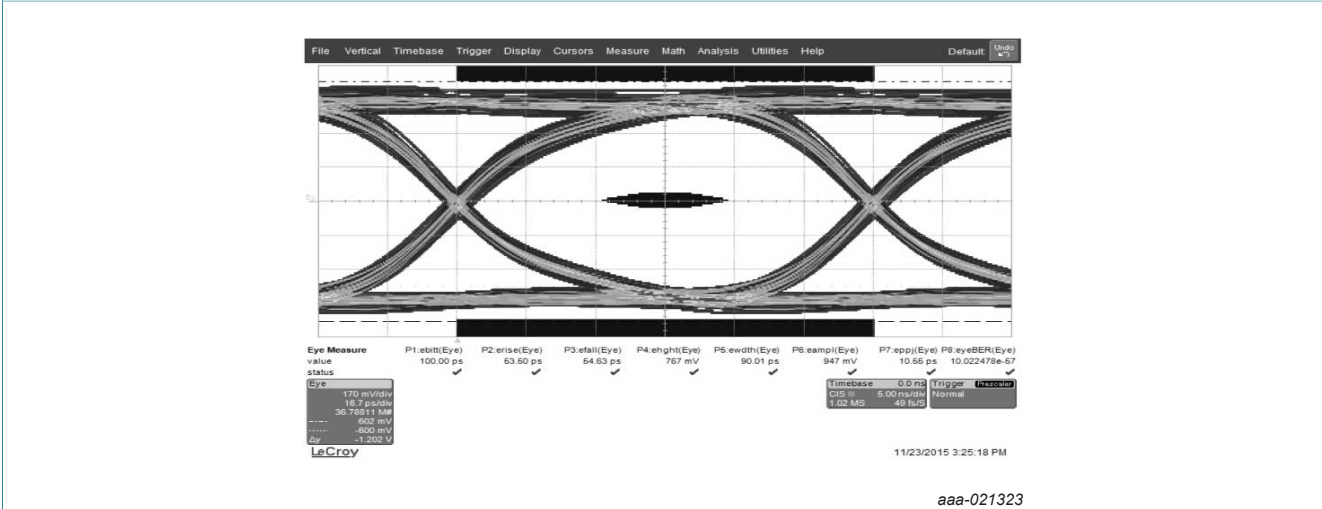


Fig. 5. USB3.1 eye diagram 10 Gbps, test board without device; typical values

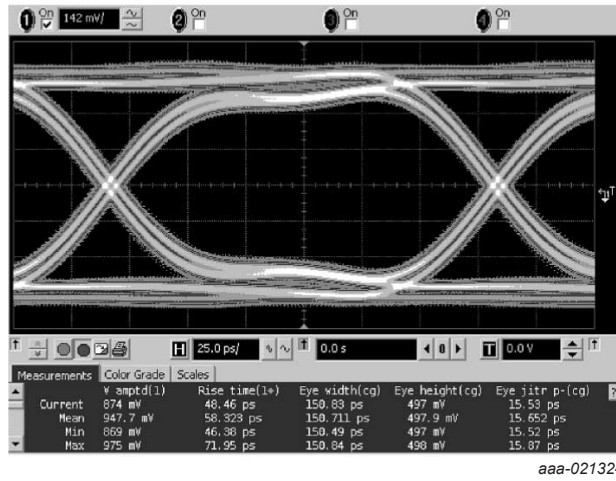


Fig. 6. HDMI 2.0 eye diagram TP1, test board with PESD3USB3S; typical values

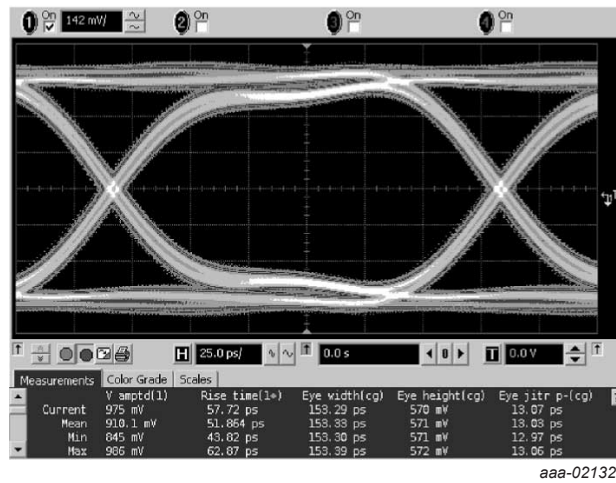
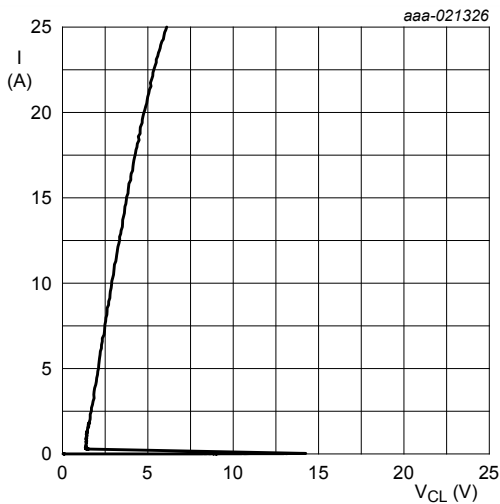
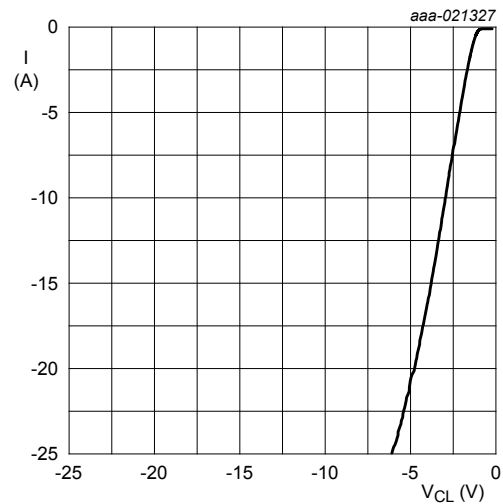


Fig. 7. HDMI 2.0 eye diagram TP1, test board without device; typical values



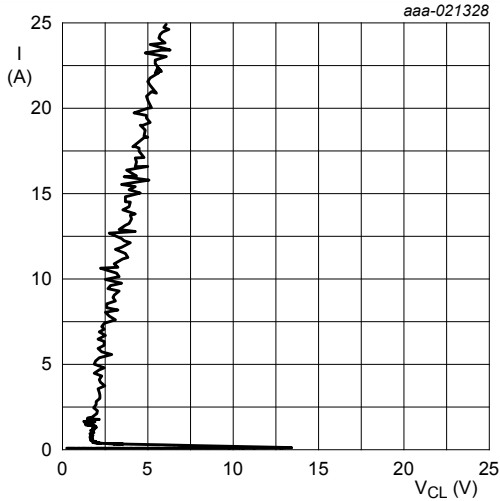
Transmission Line Pulse (TLP) = 100 ns

Fig. 8. Dynamic resistance with positive clamping; typical values



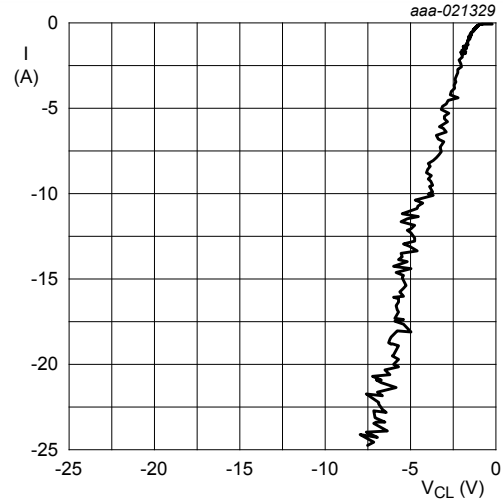
Transmission Line Pulse (TLP) = 100 ns

Fig. 9. Dynamic resistance with negative; typical values



Transmission Line Pulse (TLP) = 5 ns

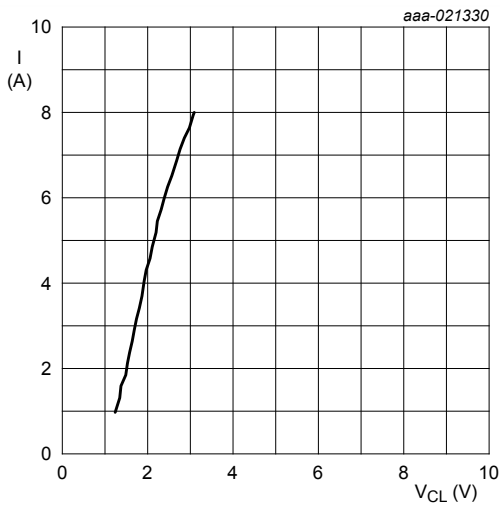
Fig. 10. Dynamic resistance with positive clamping; typical values



Transmission Line Pulse (TLP) = 5 ns

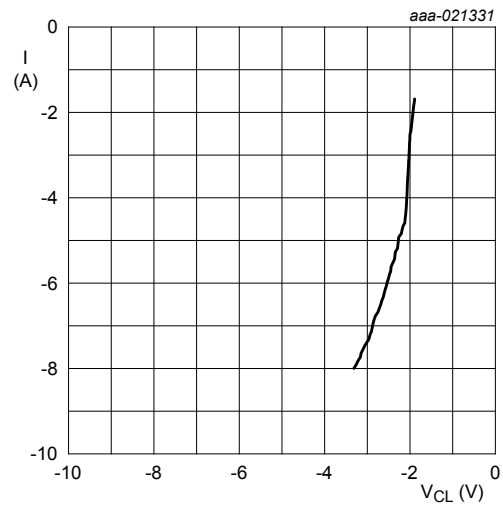
Fig. 11. Dynamic resistance with negative clamping; typical values

The device uses an advanced clamping structure showing a negative dynamic resistance. This snap-back behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid keeping the ESD protection device in snap-back state after exceeding breakdown voltage (due to an ESD pulse for instance).



IEC61000-4-5; $t_p = 8/20 \mu s$; positive pulse

Fig. 12. Dynamic resistance with positive clamping; typical values



IEC61000-4-5; $t_p = 8/20 \mu s$; negative pulse

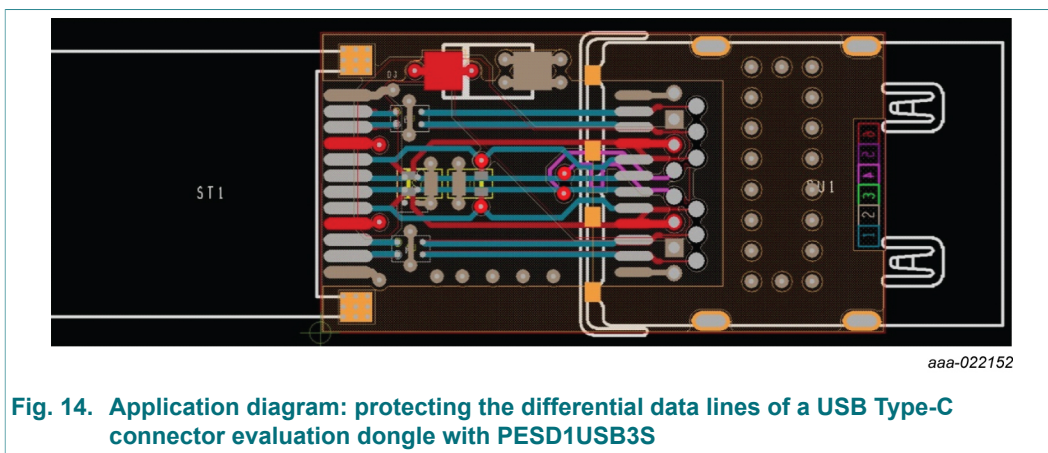
Fig. 13. Dynamic resistance with negative clamping; typical values

7. Application information

The device is designed to provide high-level ESD protection for differential high-speed data line pairs such as:

- USB 3.2
- HDMI 2.0
- Transition-Minimized Differential Signaling (TMDS)
- DisplayPort
- external Serial Advanced Technology Attachment (eSATA)
- Low Voltage Differential Signaling (LVDS)

When designing the Printed-Circuit Board (PCB), give careful consideration to impedance matching and signal coupling. Do not connect the protected signal lines to unlimited current sources like, for example, a battery.



Since the SuperSpeed TX/RX lines are separated by GND or VBUS from the Hi-Speed lines, PESD1USB3S makes it easy to achieve same signal lengths, straight routing, and optimal positioning for ESD protection directly at the connector.

8. Package outline

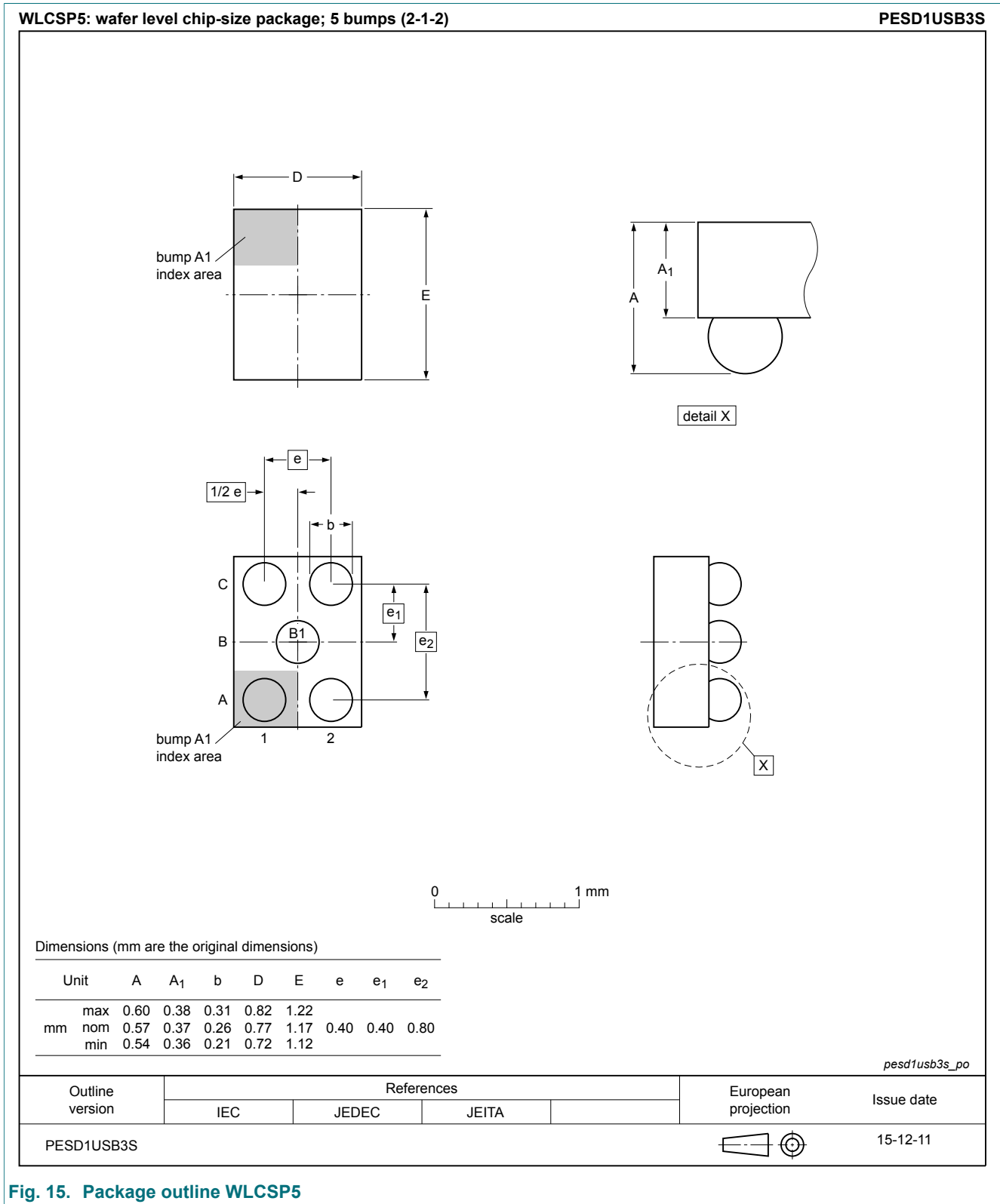
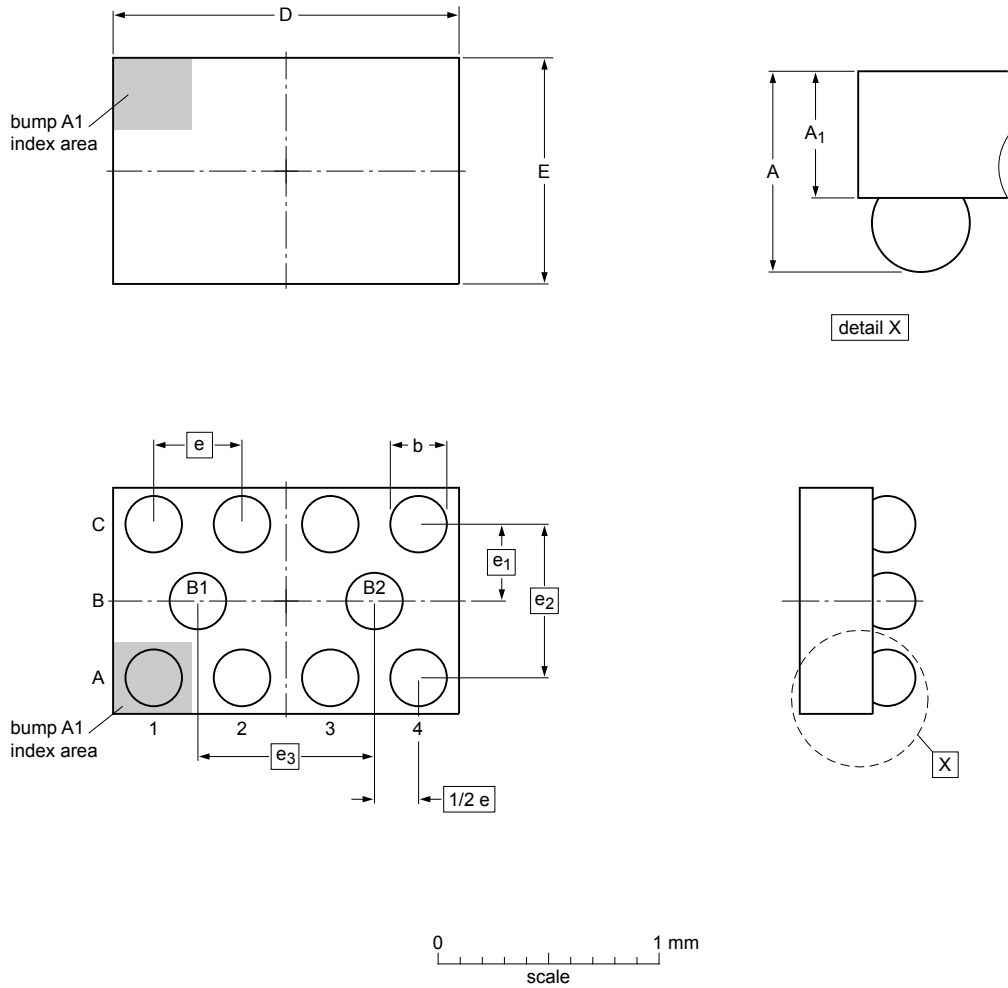


Fig. 15. Package outline WLCSP5

WLCSP10: wafer level chip-size package; 10 bumps (4-2-4)

PESD2USB3S



Dimensions (mm are the original dimensions)

| Unit | A | A ₁ | b | D | E | e | e ₁ | e ₂ | e ₃ |
|------|----------|----------------|------|------|------|------|----------------|----------------|----------------|
| mm | max 0.60 | 0.38 | 0.31 | 1.62 | 1.22 | | | | |
| | nom 0.57 | 0.37 | 0.26 | 1.57 | 1.17 | 0.40 | 0.40 | 0.80 | 0.80 |
| | min 0.54 | 0.36 | 0.21 | 1.52 | 1.12 | | | | |

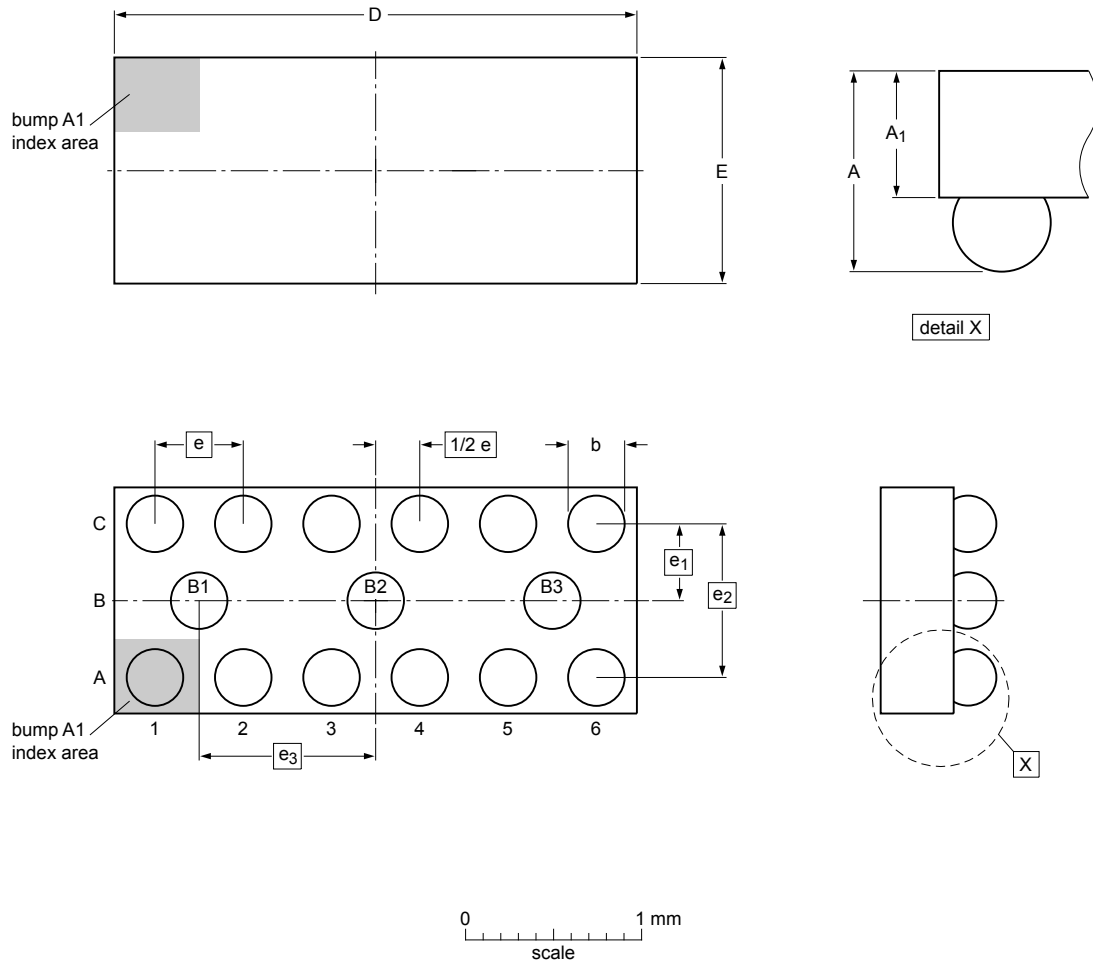
pesd2usb3s_po

| Outline version | References | | | | European projection | Issue date |
|-----------------|------------|-------|-------|--|---------------------|------------|
| | IEC | JEDEC | JEITA | | | |
| PESD2USB3S | | | | | | 15-12-11 |

Fig. 16. Package outline WLCSP10

WLCSP15: wafer level chip-size package; 15 bumps (6-3-6)

PESD3USB3S



Dimensions (mm are the original dimensions)

| Unit | A | A ₁ | b | D | E | e | e ₁ | e ₂ | e ₃ |
|--------|------|----------------|------|------|------|------|----------------|----------------|----------------|
| max | 0.60 | 0.38 | 0.31 | 2.42 | 1.22 | | | | |
| mm nom | 0.57 | 0.37 | 0.26 | 2.37 | 1.17 | 0.40 | 0.40 | 0.80 | 0.80 |
| min | 0.54 | 0.36 | 0.21 | 2.32 | 1.12 | | | | |

pesd3usb3s_po

| Outline version | References | | | | European projection | Issue date |
|-----------------|------------|-------|-------|--|---------------------|------------|
| | IEC | JEDEC | JEITA | | | |
| PESD3USB3S | | | | | | 15-12-11 |

Fig. 17. Package outline WLCSP15

9. Soldering

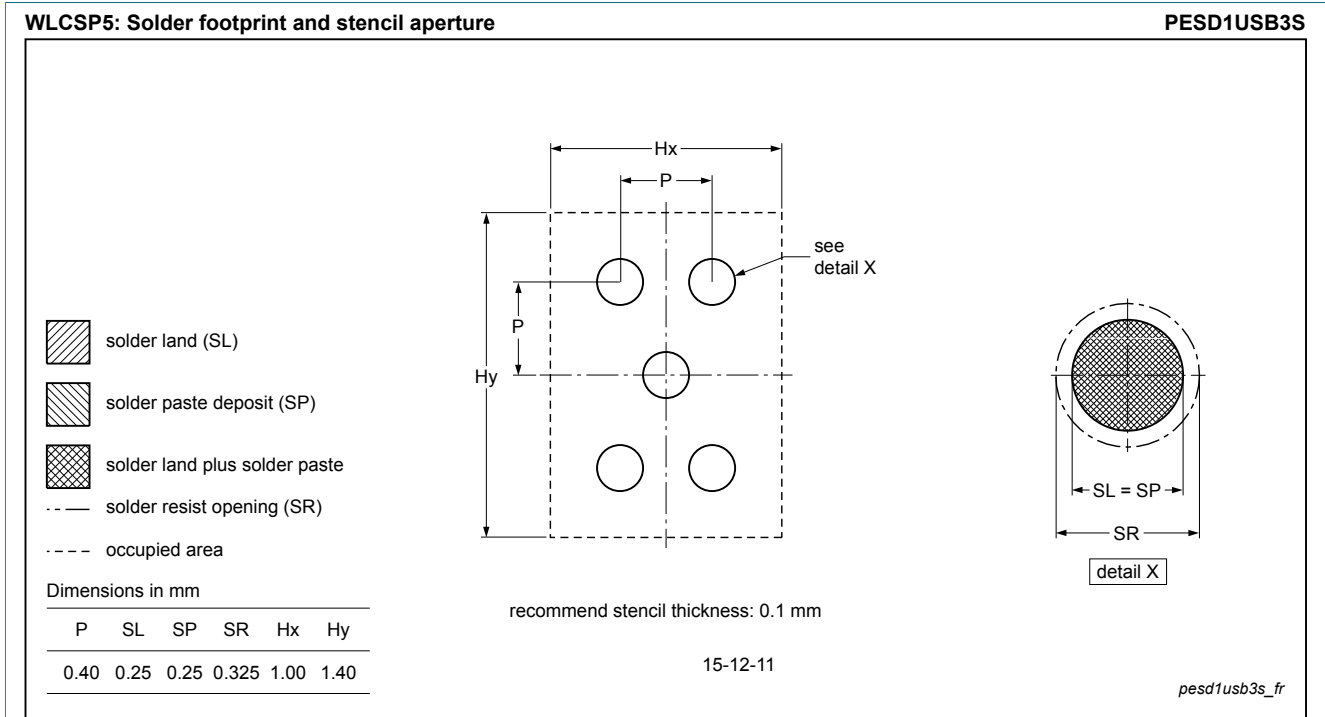


Fig. 18. Soldering footprint WLCSP5 (PESD1USB3S)

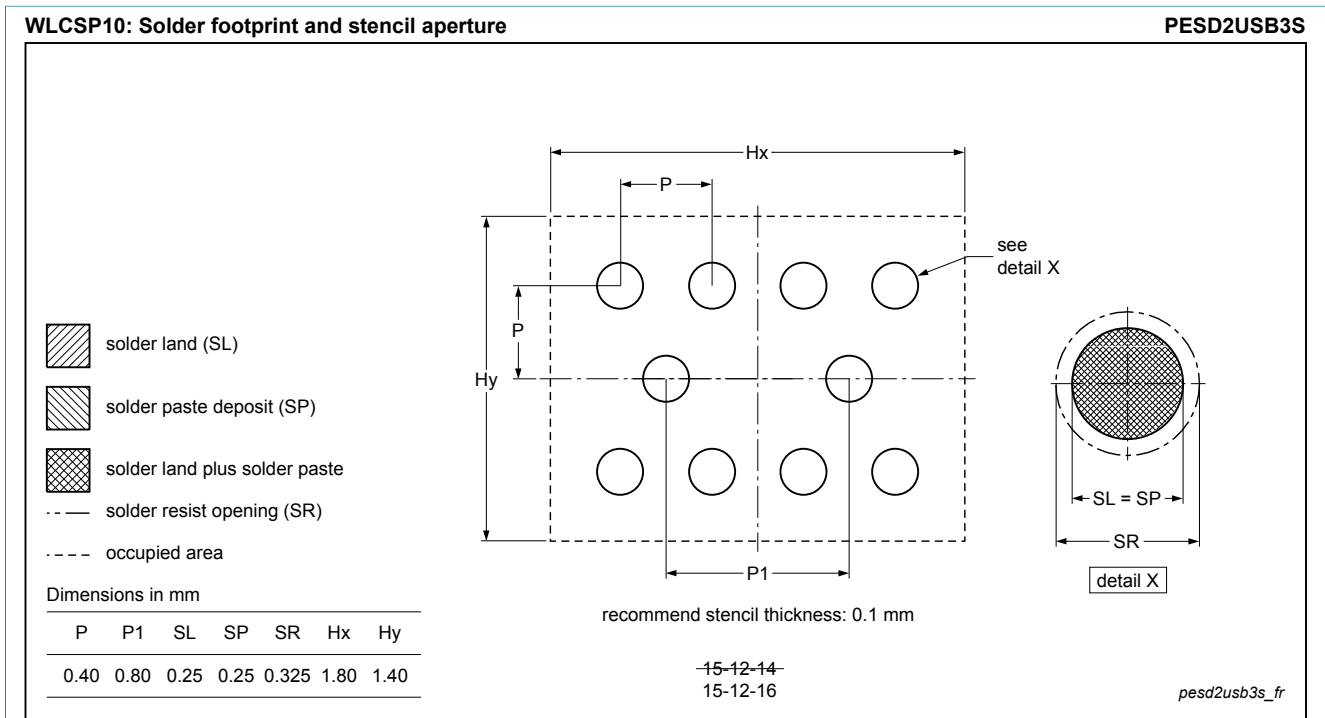


Fig. 19. Soldering footprint WLCSP10 (PESD2USB3S)

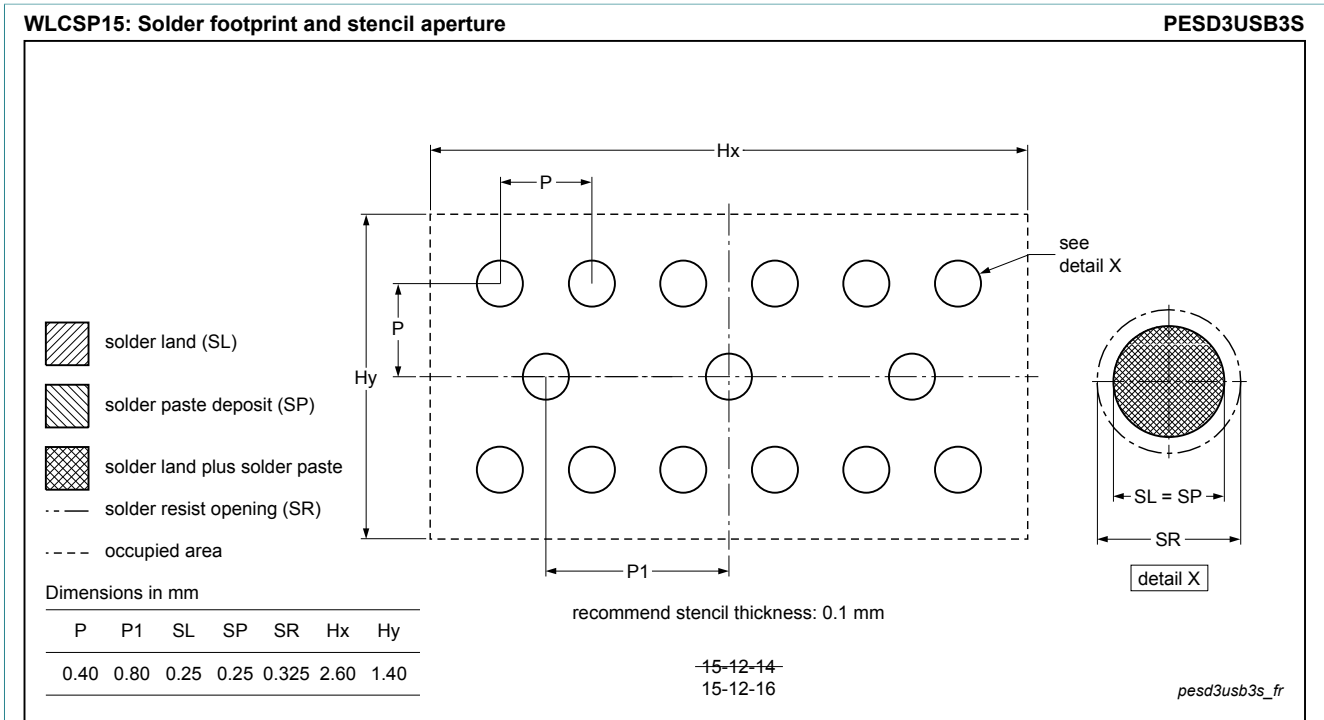


Fig. 20. Soldering footprint WLCSP15 (PESD3USB3S)

10. Revision history

Table 8. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|--------------------|---|--------------------|---------------|--------------------|
| PESDXUSB3S_SER v.4 | 20190130 | Product data sheet | - | PESDXUSB3S_SER v.3 |
| Modifications: | <ul style="list-style-type: none"> Limiting values: maximum value for T_{amb} updated Frequency characteristics: table and Fig 2 + 3: S_{21dd} changed to S_{dd21} | | | |
| PESDXUSB3S_SER v.3 | 20160426 | Product data sheet | - | PESDXUSB3S_SER v.2 |
| PESDXUSB3S_SER v.2 | 20160127 | Product data sheet | - | PESDXUSB3S_SER v.1 |
| PESDXUSB3S_SER v.1 | 20151216 | | | |

11. Legal information

Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
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| Product [short] data sheet | Production | This document contains the product specification. |

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[P6KE8.2A](#) [SA110CA](#) [SA60CA](#) [SA64CA](#) [SMBJ12CATR](#) [SMBJ8.0A](#) [SMLJ30CA-TP](#) [ESD101-B1-02ELS E6327](#) [ESD112-B1-02EL E6327](#)
[ESD119B1W01005E6327XTSA1](#) [ESD5V0L1B02VH6327XTSA1](#) [ESD7451N2T5G](#) [19180-510](#) [CPDT-5V0USP-HF](#) [3.0SMCJ33CA-F](#)
[3.0SMCJ36A-F](#) [HSPC16701B02TP](#) [D3V3Q1B2DLP3-7](#) [D55V0M1B2WS-7](#) [DESD5V0U1BL-7B](#) [DRTR5V0U4SL-7](#) [SCM1293A-04SO](#)
[ESD200-B1-CSP0201 E6327](#) [ESD203-B1-02EL E6327](#) [SM12-7](#) [SMF8.0A-TP](#) [SMLJ45CA-TP](#) [CEN955 W/DATA](#) [82350120560](#)
[82356240030](#) [VESD12A1A-HD1-GS08](#) [CPDUR5V0R-HF](#) [CPDUR24V-HF](#) [CPDQC5V0U-HF](#) [CPDQC5V0USP-HF](#) [CPDQC5V0-HF](#)
[D1213A-01LP4-7B](#) [D1213A-02WL-7](#) [ESDLIN1524BJ-HQ](#) [5KP100A](#) [5KP15A](#)