1. General description

Ultra low capacitance bidirectional ElectroStatic Discharge (ESD) protection diode in a DSN0603-2 (SOD962) leadless ultra small Surface-Mounted Device (SMD) package. The device is designed to protect one signal line from the damage caused by ESD and other transients.

2. Features and benefits

- · Bidirectional ESD protection of one line
- Ultra small leadless package with a height of 0.3 mm
- IEC 61000-4-5 (surge); I_{PPM} = 8.3 A (average measured)
- Very low clamping voltage: V_{CL} = 8.9 V max for 7.1 A, 8/20 μs pulse
- Ultra low leakage current: I_{RM} < 1 nA
- ESD protection up to 27 kV

3. Applications

ESD and surge protection for:

- very sensitive interface lines
- · generic interface lines

in portable electronics, communication, consumer and computing devices.

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
C _d	diode capacitance	f = 1 MHz; V _R = 0 V; T _{amb} = 25 °C		-	8.5	10	pF
I _{PPM}	rated peak pulse current	$t_p = 8/20 \ \mu s$	[1] [2]	-	-	7.1	Α
V _{RWM}	reverse standoff voltage	T _{amb} = 25 °C		-	-	3.3	V

- [1] According to IEC 61000-4-5.
- [2] Average measured $I_{PPM} = 8.3 A$.



5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K1	cathode (diode 1)		K1 K2
2	K2	cathode (diode 2)		sym045
			Transparent top view	
			DSN0603-2 (SOD962-2)	

6. Ordering information

Table 3. Ordering information

Type number	Package					
	Name	Description	Version			
PESD3V3V1BCSF		silicon, leadless ultra small package; 2 terminals; 0.4 mm pitch; 0.6 mm x 0.3 mm x 0.3 mm body	SOD962-2			

7. Marking

Table 4. Marking codes

Type number	Marking code
PESD3V3V1BCSF	T

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
I_{PPM}	rated peak pulse current	t _p = 8/20 μs	[1] [2]	-	7.1	Α
Tj	junction temperature			-	150	°C
T _{amb}	ambient temperature			-40	125	°C
T _{stg}	storage temperature			-65	150	°C
ESD maximum	ratings			•		
V _{ESD}	lta.a.a	IEC 61000-4-2; contact discharge	[3]	-	27	kV
		IEC 61000-4-2; air discharge	[3]	-	27	kV

- [1] According to IEC 61000-4-5.
- [2] Average measured I_{PPM} = 8.3 A.
- [3] Device stressed with ten non-repetitive ESD pulses.

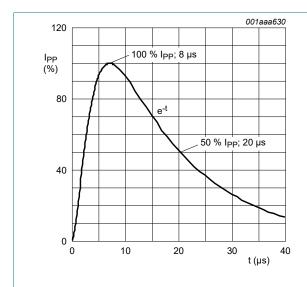


Fig. 1. 8/20 μs pulse waveform according to IEC 61000-4-5

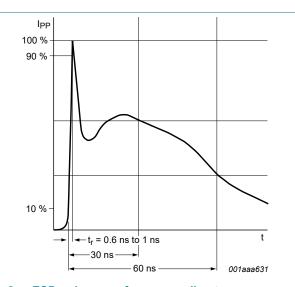


Fig. 2. ESD pulse waveform according to IEC 61000-4-2

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V_{RWM}	reverse standoff voltage	T _{amb} = 25 °C		-	-	3.3	V
V_{BR}	breakdown voltage	I _R = 5 mA; T _{amb} = 25 °C		4.5	5.5	8	V
I _{RM}	reverse leakage current	V _R = 3.3 V; T _{amb} = 25 °C		-	0.1	50	nA
C_d	diode capacitance	f = 1 MHz; V _R = 0 V; T _{amb} = 25 °C		-	8.5	10	pF
V_{CL}	clamping voltage	I_{PPM} = 7.1 A; t_p = 8/20 µs; T_{amb} = 25 °C	[1]	-	-	8.9	V
		I_{PP} = 8 A; t_p = TLP; T_{amb} = 25 °C	[2]	-	5.5	7.5	V
		I _{PP} = 16 A; t _p = TLP; T _{amb} = 25 °C	[2]	-	9	11	V

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
R_{dyn}	dynamic resistance	I _R = 10 A; T _{amb} = 25 °C	[2]	-	0.17	-	Ω

- [1] Device stressed with 8/20 μs exponential decay waveform according to IEC 61000-4-5.
- [2] Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008.

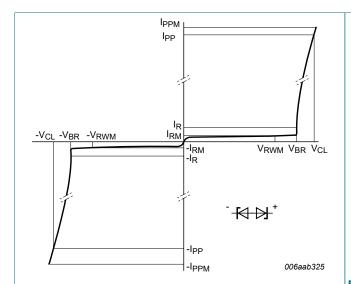


Fig. 3. V-I characteristics for a bidirectional ESD protection diode

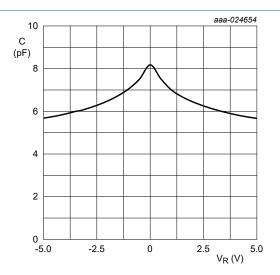


Fig. 4. Diode capacitance as a function of reverse voltage; typical values

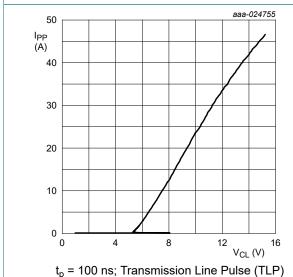


Fig. 5. Positive clamping voltage (TLP); typical values

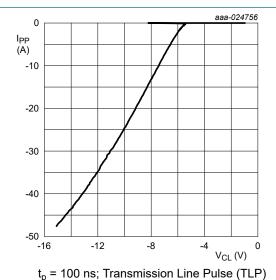
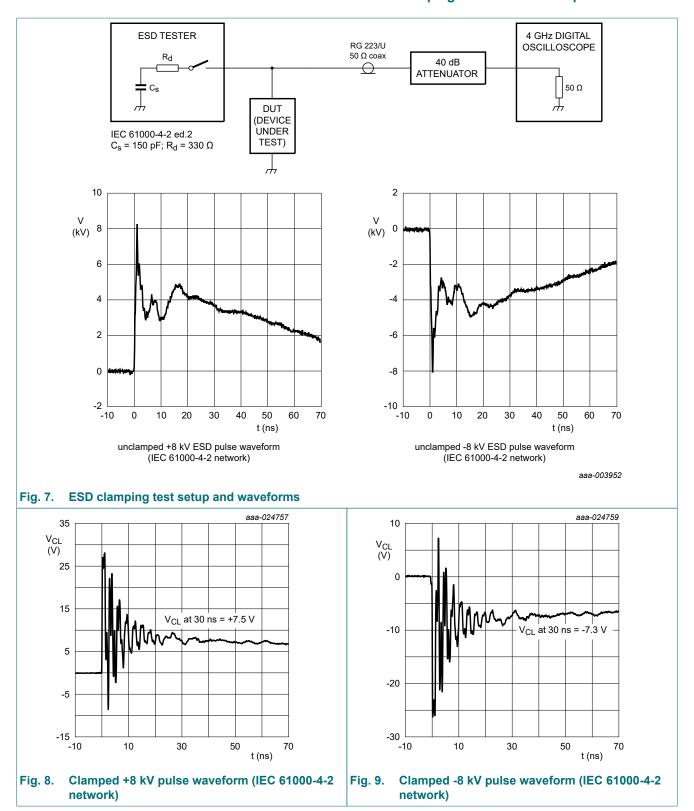
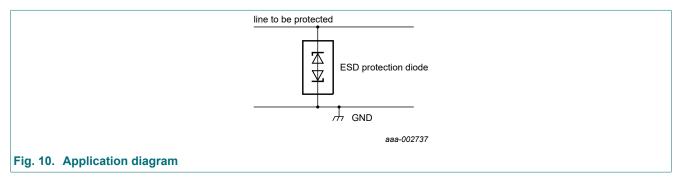


Fig. 6. Negative clamping voltage (TLP); typical values



10. Application information

The device is designed for the protection of one bidirectional data line from surge pulses and ESD damage. The device is suitable on lines where the signal polarities are both positive and negative with respect to ground. The device is not designed to be used on lines connected to a DC supply.

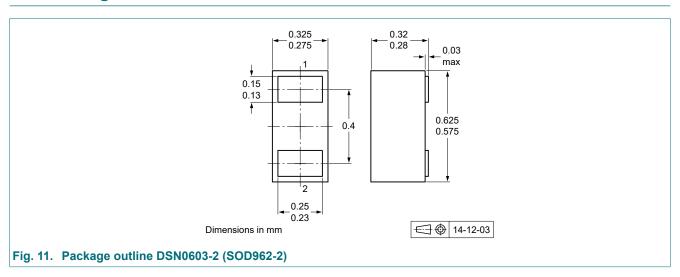


Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

- 1. Place the device as close to the input terminal or connector as possible.
- 2. Minimize the path length between the device and the protected line.
- **3.** Keep parallel signal paths to a minimum.
- 4. Avoid running protected conductors in parallel with unprotected conductors.
- 5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
- 6. Minimize the length of the transient return path to ground.
- 7. Avoid using shared transient return paths to a common ground point.
- 8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

11. Package outline



12. Soldering

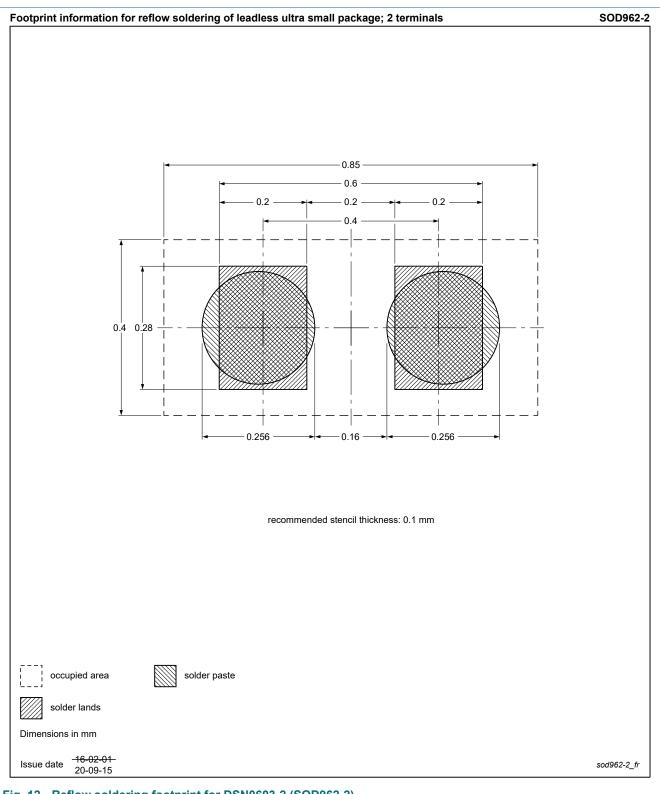


Fig. 12. Reflow soldering footprint for DSN0603-2 (SOD962-2)

13. Revision history

Table 7. Revision history

Table 11 Novicion motory							
Data sheet ID	Release date	Data sheet status	Change notice	Supersedes			
PESD3V3V1BCSF v.3	20210408	Product data sheet	-	PESD3V3V1BCSF v.2			
Modifications:	Figure "Reflow solde	Figure "Reflow soldering footprint" updated					
PESD3V3V1BCSF v.2	20170721	Product data sheet	-	PESD3V3V1BCSF v.1			
PESD3V3V1BCSF v.1	20160929	Product data sheet	-	-			

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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