

8 April 2021

**Product data sheet** 

## 1. General description

Extremely low capacitance bidirectional ElectroStatic Discharge (ESD) protection diode, part of the TrEOS protection family. This device is housed in a DSN0603-2 (SOD962-2) leadless ultra small Surface-Mounted Device (SMD) package designed to protect one signal line from the damage caused by ESD and other transients.

#### 2. Features and benefits

- · Bidirectional ESD protection of one line
- Extremely low trigger-voltage V<sub>t1</sub> of 7 V TLP
- Extremely low diode capacitance C<sub>d</sub> = 0.24 pF
- Extremely low clamping voltage to protect sensitive I/Os
- Extremely low-inductance protection path to ground
- ESD protection up to ±15 kV according to IEC 61000-4-2
- Ultra small SMD package

## 3. Applications

- USB 3.2, HDMI2, and Universal Flash Storage (UFS) data lines
- · Cellular handsets and accessories
- · Portable electronics
- Communication systems
- · Computers and peripherals

#### 4. Quick reference data

#### Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
$V_{RWM}$	reverse standoff voltage			-	-	4	V
C <sub>d</sub>	diode capacitance	f = 1 MHz; V <sub>R</sub> = 0 V; T <sub>amb</sub> = 25 °C	[1]	-	0.24	0.29	pF

[1] Guaranteed by design.



# 5. Pinning information

#### **Table 2. Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K1	cathode (diode 1)		K1   K2
2	K2	cathode (diode 2)		sym045
			Transparent top view	
			DSN0603-2 (SOD962-2)	

# 6. Ordering information

#### **Table 3. Ordering information**

Type number			
	Name	Description	Version
PESD4V0Y1BSF		silicon, leadless ultra small package; 2 terminals; 0.4 mm pitch; 0.6 mm x 0.3 mm x 0.3 mm body	SOD962-2

# 7. Marking

#### Table 4. Marking codes

Type number	Marking code
PESD4V0Y1BSF	C5

# 8. Limiting values

#### **Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{RWM}$	reverse standoff voltage			-	4	V
T <sub>amb</sub>	ambient temperature			-40	125	°C
T <sub>stg</sub>	storage temperature			-65	150	°C
ESD maximum	ratings					
V <sub>ESD</sub>	voltago	IEC 61000-4-2; contact discharge	[1]	-15	15	kV
		IEC 61000-4-2; air discharge	[1]	-15	15	kV

[1] Device stressed with ten non-repetitive ESD pulses.

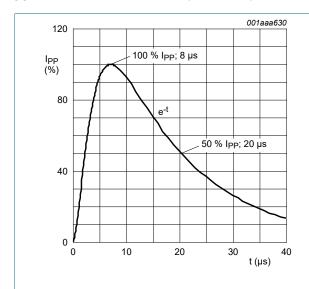


Fig. 1. 8/20 μs pulse waveform according to IEC 61000-4-5 and IEC 61643-321

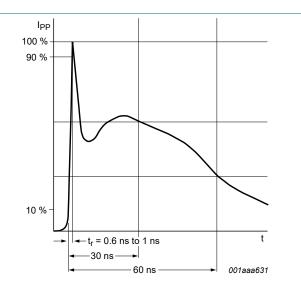


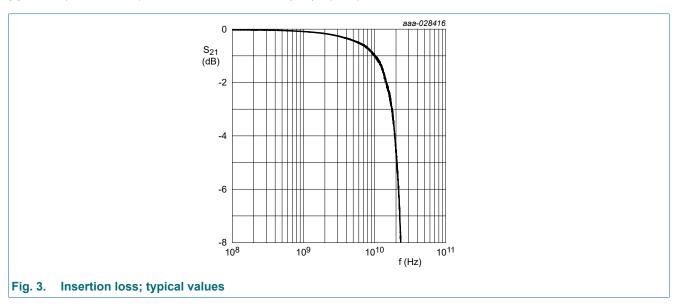
Fig. 2. ESD pulse waveform according to IEC 61000-4-2

## 9. Characteristics

**Table 6. Characteristics** 

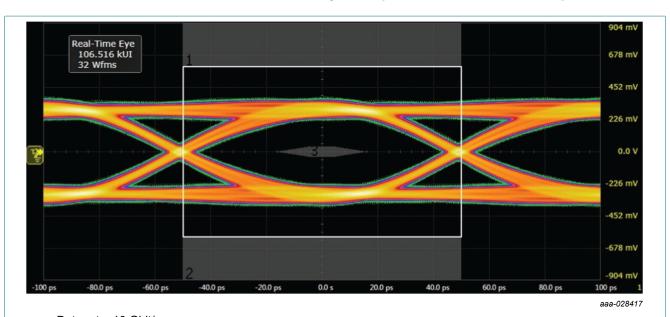
Symbol	Parameter	Conditions		Min	Тур	Max	Unit
$V_{BR}$	breakdown voltage	I <sub>R</sub> = 1 mA; T <sub>amb</sub> = 25 °C		4.2	6.2	8	V
I <sub>RM</sub>	reverse leakage current	V <sub>RWM</sub> = 4 V; T <sub>amb</sub> = 25 °C		-	1	50	nA
C <sub>d</sub>	diode capacitance	f = 1 MHz; V <sub>R</sub> = 0 V; T <sub>amb</sub> = 25 °C	[1]	-	0.24	0.29	pF
V <sub>CL</sub>	clamping voltage	I <sub>PPM</sub> = 4 A; T <sub>amb</sub> = 25 °C	[2]	-	3.7	-	V
R <sub>dyn</sub>	dynamic resistance	I <sub>R</sub> = 10 A; T <sub>amb</sub> = 25 °C	[3]	-	0.25	-	Ω
		I <sub>R</sub> = -10 A; T <sub>amb</sub> = 25 °C	[3]	-	0.25	-	Ω
f <sub>-3dB</sub>	-3 dB cut-off frequency	$T_{amb}$ = 25 °C; normalized to attenuation at 1 MHz		-	19.6	-	GHz

- Guaranteed by design. Device stressed with 8/20  $\mu$ s exponential decay waveform according to IEC 61000-4-5. Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008.



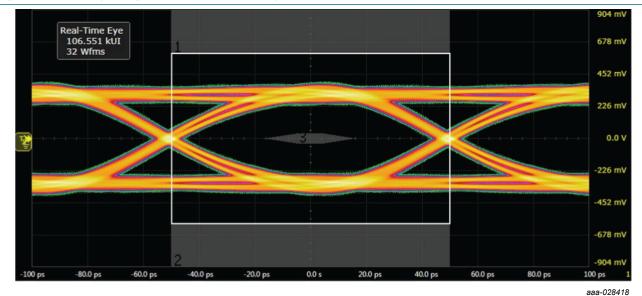
Nexperia PESD4V0Y1BSF

#### Extremely low capacitance bidirectional ESD protection diode



Data rate: 10 Gbit/s

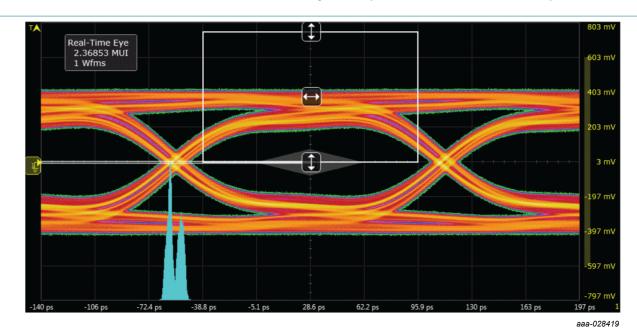
Fig. 4. USB 3.2 eye diagram, PCB with device; typical values



Data rate: 10 Gbit/s

Fig. 5. USB 3.2 eye diagram, PCB without device; typical values

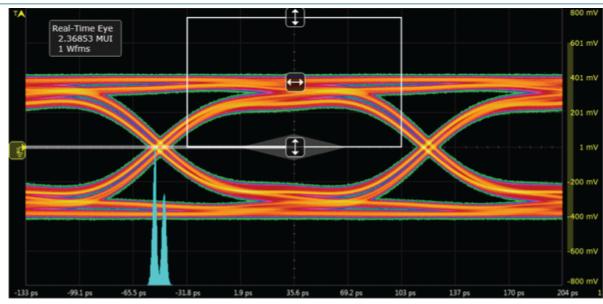
5 / 15



1080p

Data rate: 6 Gbit/s

Fig. 6. HDMI TP1 eye diagram, PCB with device; typical values



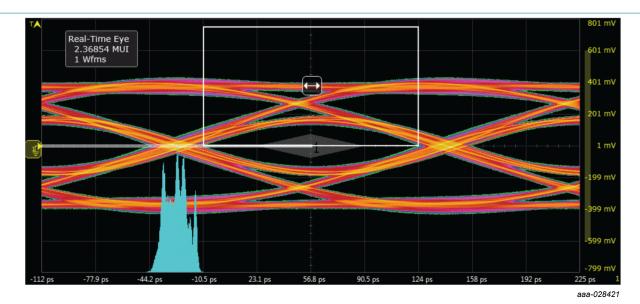
aaa-028420

1080p Data rate: 6 Gbit/s

ig. 7. HDMI TP1 eye diagram, PCB without device; typical values

Nexperia PESD4V0Y1BSF

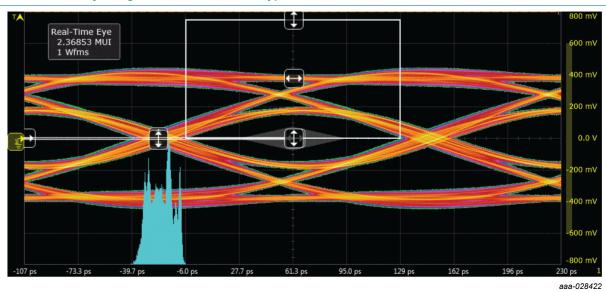
## Extremely low capacitance bidirectional ESD protection diode



1080p

Data rate: 6 Gbit/s

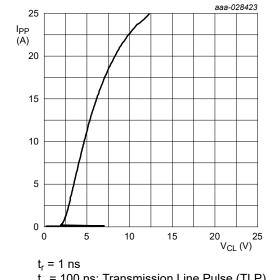
Fig. 8. HDMI TP2 eye diagram, PCB with device; typical values

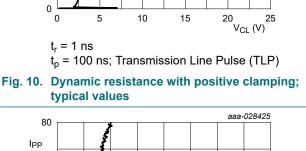


1080p

Data rate: 6 Gbit/s

Fig. 9. HDMI TP2 eye diagram, PCB without device; typical values





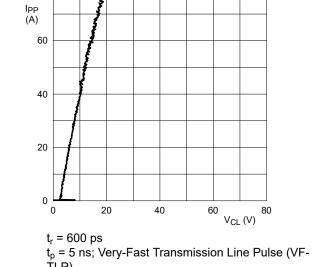
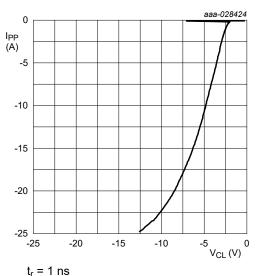
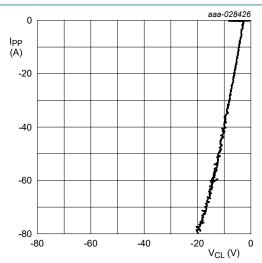


Fig. 12. Dynamic resistance with positive clamping; typical values



t<sub>p</sub> = 100 ns; Transmission Line Pulse (TLP)

Fig. 11. Dynamic resistance with negative clamping; typical values



 $t_{r} = 600 \text{ ps}$  $t_p$  = 5 ns; Very Fast Transmission Line Pulse (VF-

Fig. 13. Dynamic resistance with negative clamping; typical values

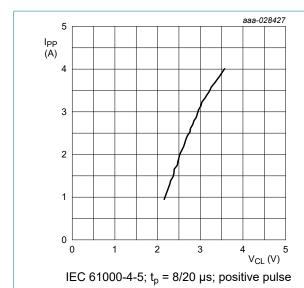


Fig. 14. Dynamic resistance with positive clamping; typical values

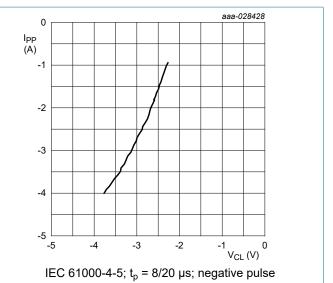
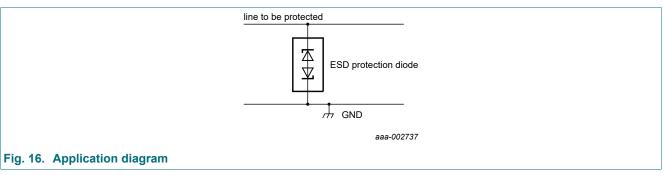


Fig. 15. Dynamic resistance with negative clamping; typical values

## 10. Application information

The device is designed for the protection of one bidirectional data line from surge pulses and ESD damage. The device is suitable on lines where the signal polarities are both positive and negative with respect to ground.

The device uses an advanced clamping structure showing a negative dynamic resistance. This snap-back behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid keeping the ESD protection device in snap-back state after exceeding breakdown voltage (due to an ESD pulse for instance).



## Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

- 1. Place the device as close to the input terminal or connector as possible.
- 2. Minimize the path length between the device and the protected line.
- 3. Keep parallel signal paths to a minimum.
- 4. Avoid running protected conductors in parallel with unprotected conductors.
- 5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
- **6.** Minimize the length of the transient return path to ground.
- 7. Avoid using shared transient return paths to a common ground point.
- 8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

# 11. Package outline

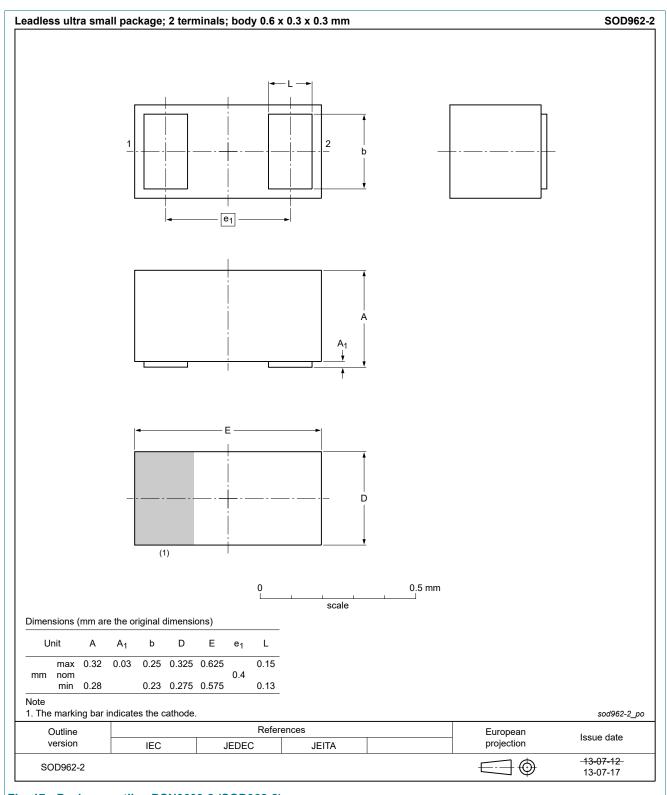


Fig. 17. Package outline DSN0603-2 (SOD962-2)

# 12. Soldering

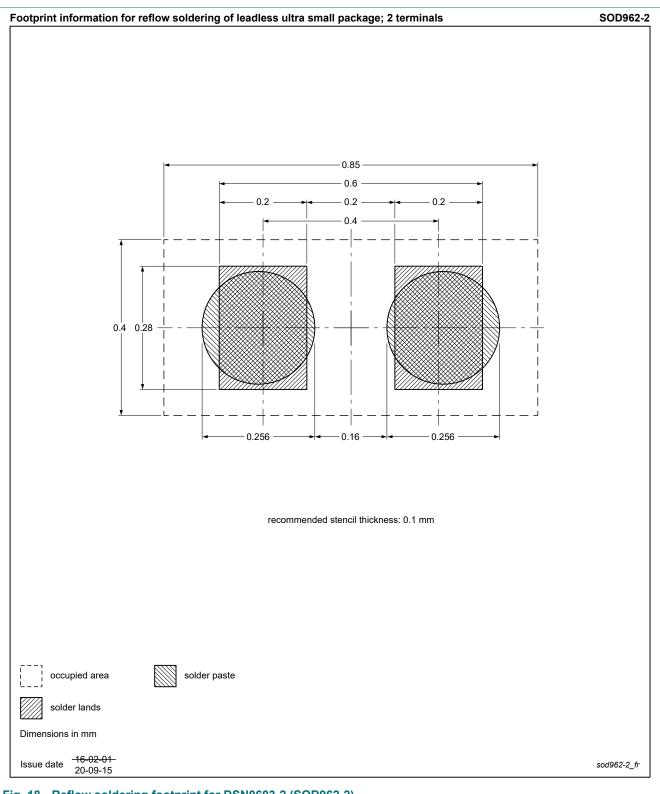


Fig. 18. Reflow soldering footprint for DSN0603-2 (SOD962-2)

# 13. Revision history

#### **Table 7. Revision history**

able 7. Revision history							
Data sheet ID	Release date	Data sheet status	Change notice	Supersedes			
PESD4V0Y1BSF v.4	20210408	Product data sheet	-	PESD4V0Y1BSF v.3			
Modifications:	Figure "Reflow solder	ering footprint" updated					
PESD4V0Y1BSF v.3	20190403	Product data sheet	-	PESD4V0Y1BSF v.2			
PESD4V0Y1BSF v.2	20180820	Product data sheet	-	PESD4V0Y1BSF v.1			
PESD4V0Y1BSF v.1	20180509	Product data sheet	-	-			

## 14. Legal information

#### **Data sheet status**

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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