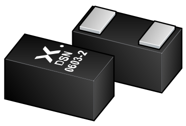


PESD4V0Z1BSF

Extremely low capacitance bidirectional ESD protection diode

2 March 2021 — Product data sheet

1. General description

Extremely low capacitance bidirectional ElectroStatic Discharge (ESD) protection diode, which is part of the TrEOS protection family. The device is housed in a DSN0603-2 (SOD962-2) leadless ultra small Surface-Mounted Device (SMD) package designed to protect one signal line from damage caused by ESD and other transients.

2. Features and benefits

- Bidirectional ESD protection of one line
- Extremely low diode capacitance C_d = 0.28 pF
- Extremely low clamping voltage to protect sensitive I/Os
- Extremely low inductance protection path to ground
- ESD protection up to 20 kV according to IEC 61000-4-2
- Ultra small SMD package
- 9.5 A maximum 8/20 µs peak pulse current

3. Applications

- Cellular handsets and accessories
- Portable electronics
- Communication systems
- Computers and peripherals

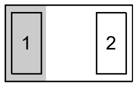
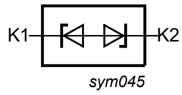
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage	T_{amb} = 25 °C		-	-	4	V
C_d	diode capacitance	f = 1 MHz; V_R = 0 V; T_{amb} = 25 °C		-	0.28	0.35	pF

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K1	cathode	 Transparent top view **DSN0603-2 (SOD962-2)**	
2	K2	cathode		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD4V0Z1BSF	DSN0603-2	silicon, leadless ultra small package; 2 terminals; 0.4 mm pitch; 0.6 mm x 0.3 mm x 0.3 mm body	SOD962-2

7. Marking

Table 4. Marking codes

Type number	Marking code
PESD4V0Z1BSF	U

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134)

Symbol	Parameter	Conditions		Min	Max	Unit
I_{PPM}	rated peak pulse current	t_p = 8/20 µs	[1]	-	9.5	A
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-40	125	°C
T_{stg}	storage temperature			-65	150	°C
ESD maximum ratings						
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2; contact discharge	[2]	-20	20	kV
		IEC 61000-4-2; air discharge	[2]	-20	20	kV

[1] Non-repetitive current pulse 8/20 µs exponentially decaying waveform according to IEC61000-4-5.
[2] Device stressed with ten non-repetitive ESD pulses.

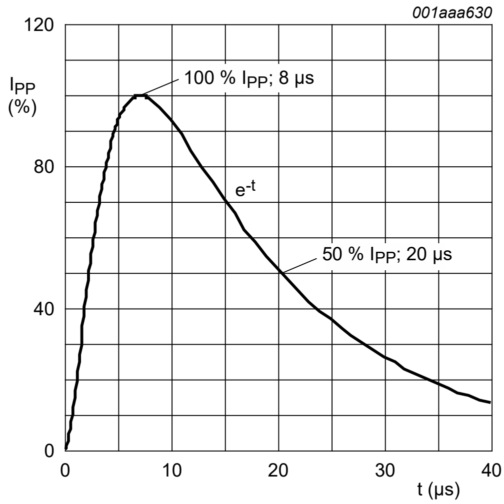


Fig. 1. 8/20 μs pulse waveform according to IEC 61000-4-5

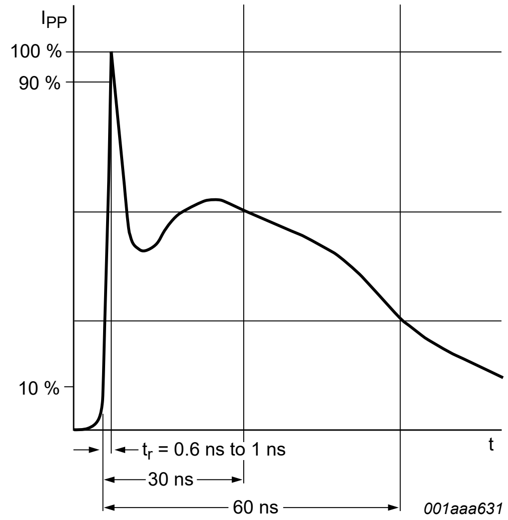


Fig. 2. ESD pulse waveform according to IEC 61000-4-2

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage	T_{amb} = 25 °C		-	-	4	V
V_{BR}	breakdown voltage	I_R = 1 mA; T_{amb} = 25 °C		-	6.9	-	V
I_{RM}	reverse leakage current	V_{RWM} = 4 V; T_{amb} = 25 °C		-	1	50	nA
C_d	diode capacitance	f = 1 MHz; V_R = 0 V; T_{amb} = 25 °C		-	0.28	0.35	pF
		f = 1 MHz; V_R = 1.5 V; T_{amb} = 25 °C		-	0.25	-	pF
V_{CL}	clamping voltage	I_{PP} = 4 A; T_{amb} = 25 °C	[1]	-	3.7	-	V
		I_{PPM} = 9.5 A; T_{amb} = 25 °C	[1]	-	5.3	-	V
R_{dyn}	dynamic resistance	4 A ≤ I_R ≤ 16 A; T_{amb} = 25 °C	[2]	-	0.19	-	Ω
		-4 A ≤ I_R ≤ -16 A; T_{amb} = 25 °C	[2]	-	0.19	-	Ω
f_{-3dB}	-3 dB cut-off frequency	T_{amb} = 25 °C; Normalized to attenuation at 1 MHz		-	17	-	GHz

[1] Non-repetitive current pulse 8/20 μs exponential decay waveform according to IEC 61000-4-5.
[2] Non-repetitive current pulse, Transmission Line Pulse (TLP) tp = 100 ns; square pulse; pulser at 70 ns to 90 ns; ANSI / ESD STM5.5.1-2008.

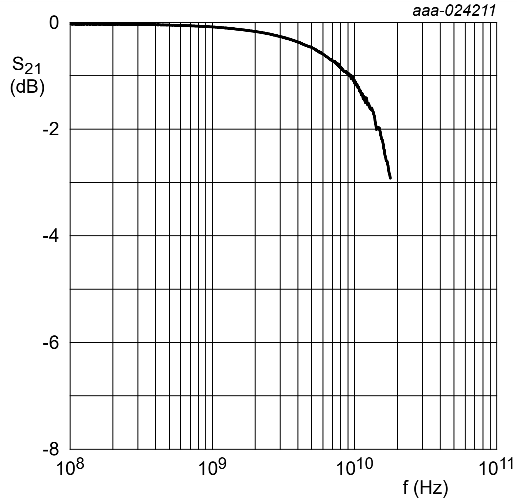
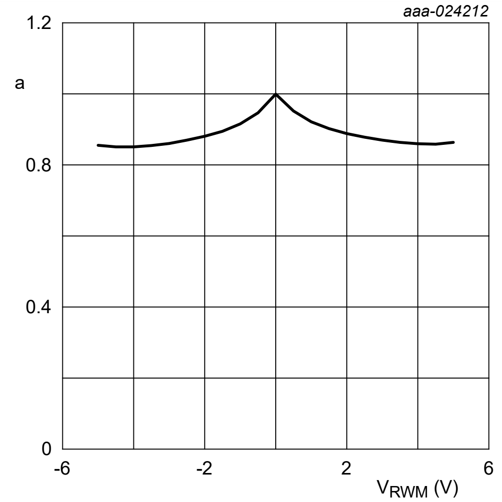
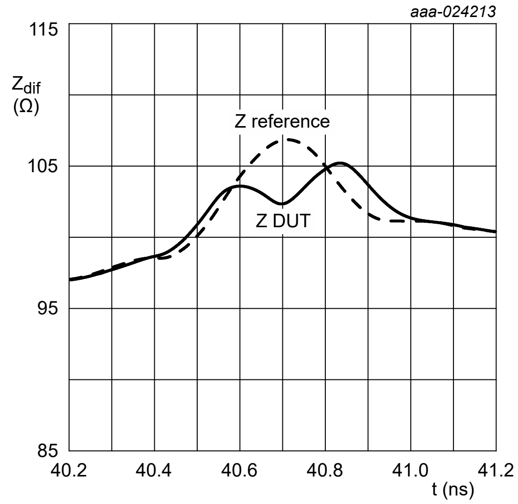


Fig. 3. Insertion loss; typical values



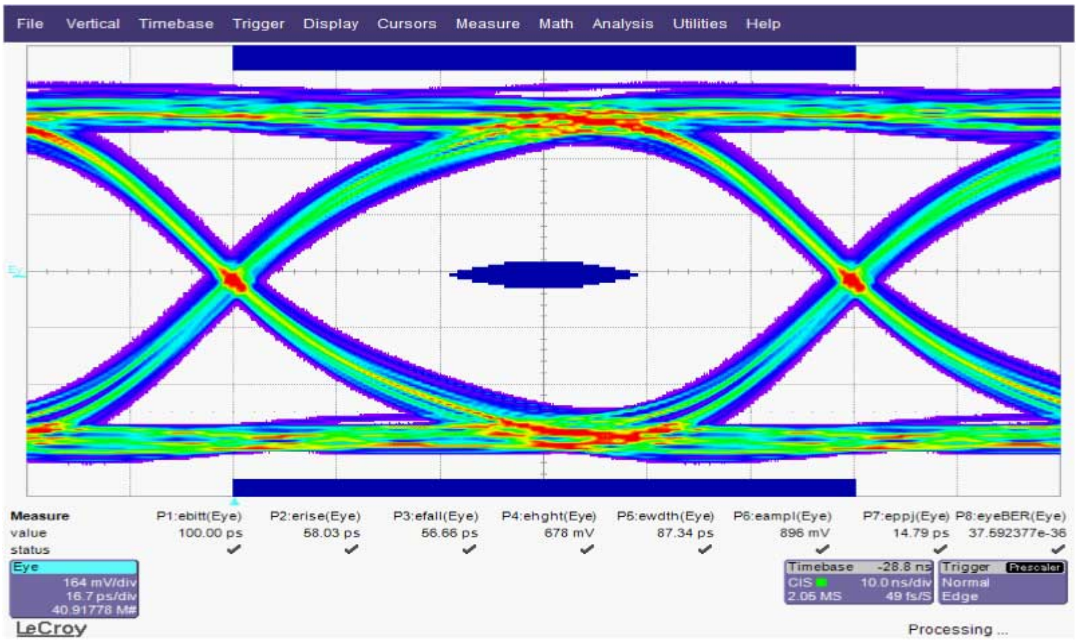
$$a = \frac{C_d}{C_d(V_{RWM} = 0\ \ V)}$$

Fig. 4. Relative capacitance as a function of reverse standoff voltage; typical values



Rise time = 200 ps

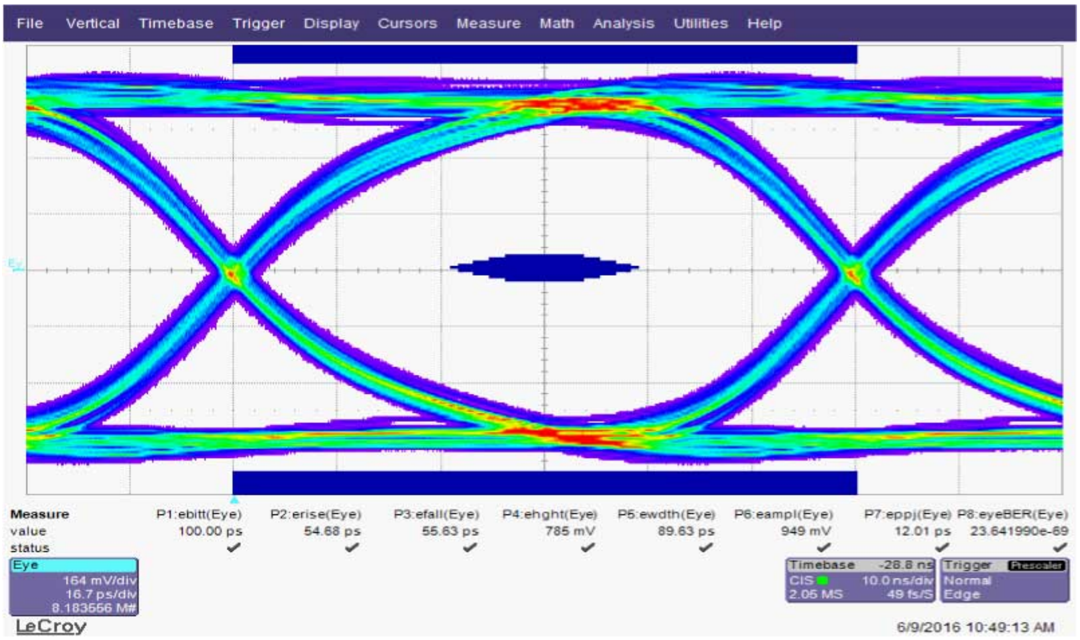
Fig. 5. Differential Time Domain Reflectometer (TDR) plot; typical values



aaa-024214

Data rate: 10 Gbit/s

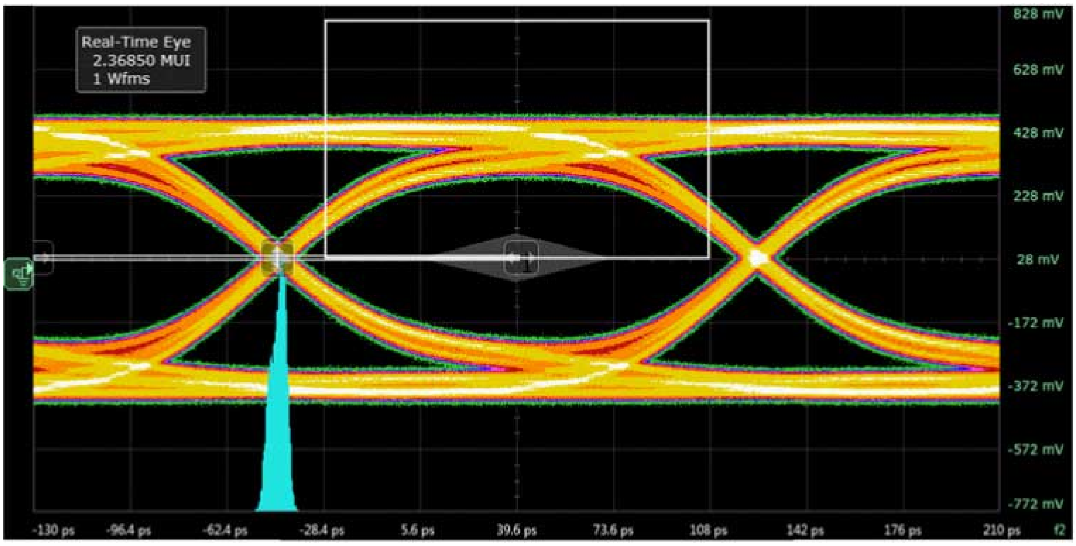
Fig. 6. USB 3.2 eye diagram, PCB with device; typical values



aaa-024215

Data rate: 10 Gbit/s

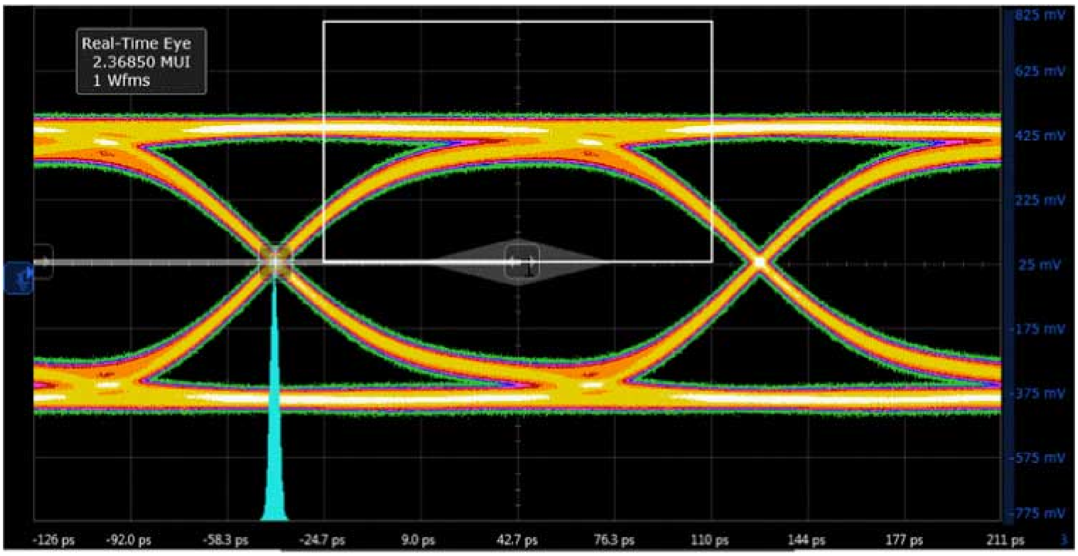
Fig. 7. USB 3.2 eye diagram, PCB without device; typical values



aaa-025117

Test frequency: 148.5 MHz
Differential swing voltage: 845 mV
Horizontal scale: 34 ps/div
Vertical scale: 200 mV/div

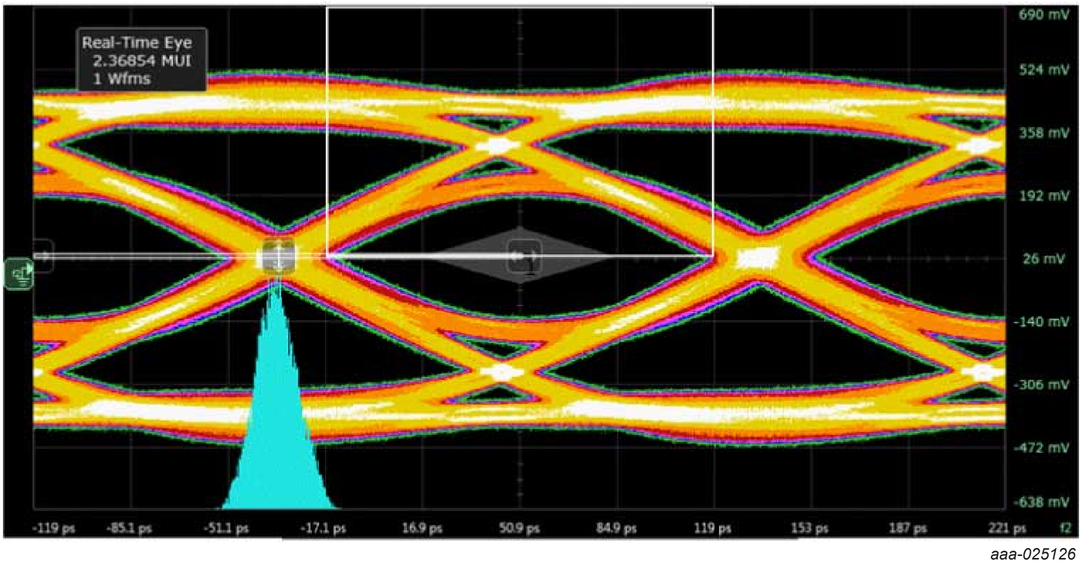
Fig. 8. HDMI 2.0 TP1 eye diagram, PCB with device; typical values



aaa-025119

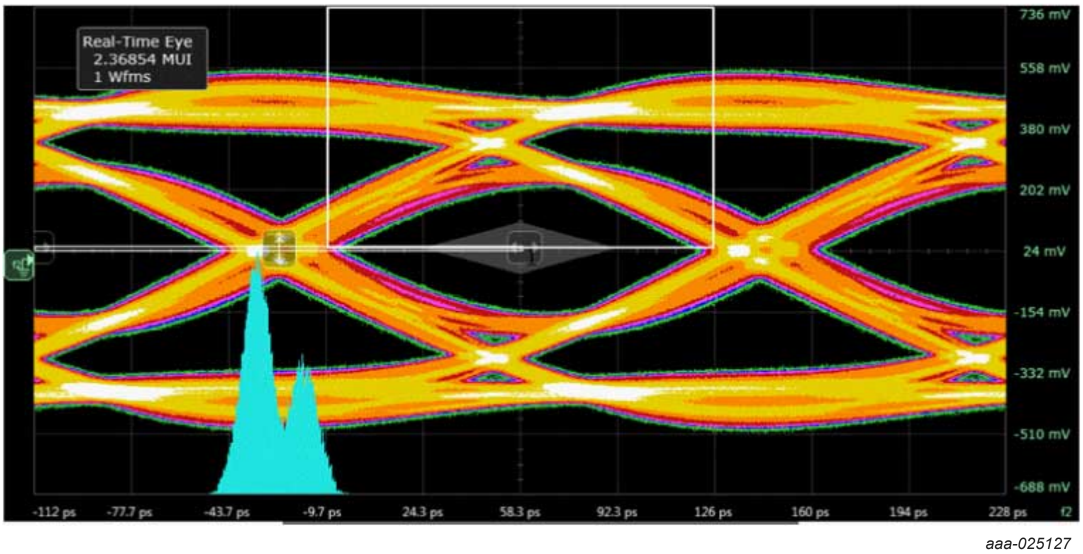
Test frequency: 148.5 MHz
Differential swing voltage: 844 mV
Horizontal scale: 34 ps/div
Vertical scale: 200 mV/div

Fig. 9. HDMI 2.0 TP1 eye diagram, PCB without device; typical values



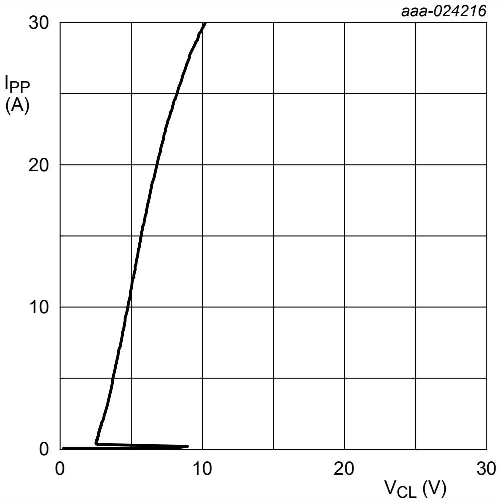
Test frequency: 148.5 MHz
Differential swing voltage: 806 mV
Horizontal scale: 34 ps/div
Vertical scale: 266 mV/div
Remark: Measured at Test Point 2 (TP2) worst cable emulator, reference cable equalizer and worst case positive skew

Fig. 10. HDMI 2.0 TP2 eye diagram, PCB with device; typical values



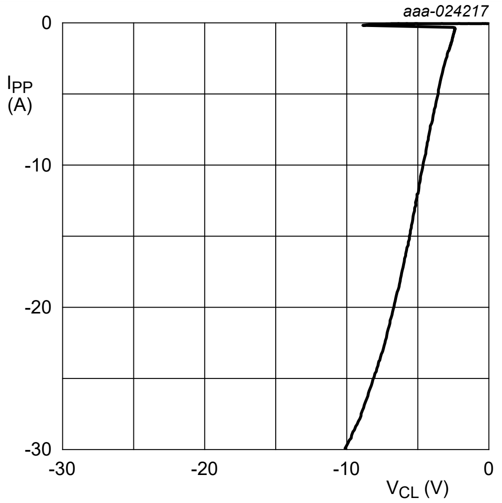
Test frequency: 148.5 MHz
Differential swing voltage: 823 mV
Horizontal scale: 34 ps/div
Vertical scale: 178 mV/div
Remark: Measured at Test Point 2 (TP2) worst cable emulator, reference cable equalizer and worst case positive skew

Fig. 11. HDMI 2.0 TP2 eye diagram, PCB without device; typical values



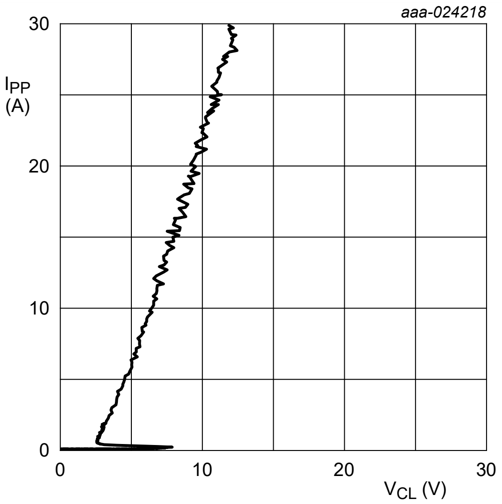
Transmission Line Pulse (TLP) = 100 ns;
rise time = 1 ns

Fig. 12. Positive clamping voltage (TLP); typical values



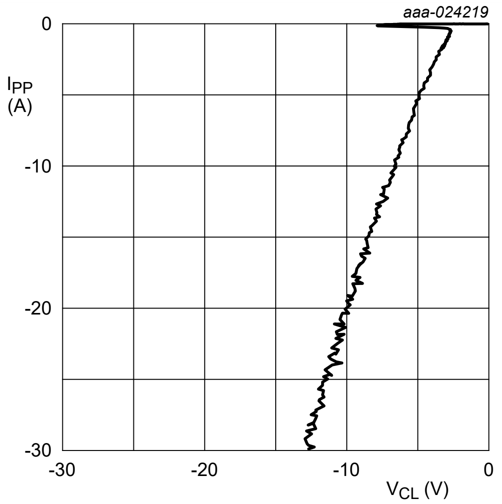
Transmission Line Pulse (TLP) = 100 ns;
rise time = 1 ns

Fig. 13. Negative clamping voltage (TLP); typical values



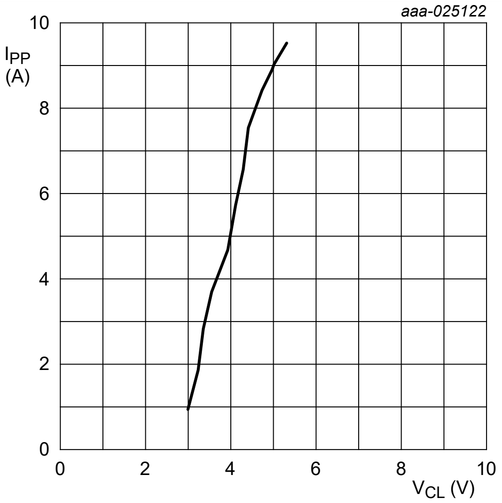
Very Fast Transmission Line Pulse (VF-TLP) = 5 ns

Fig. 14. Positive clamping voltage (VF-TLP); typical values



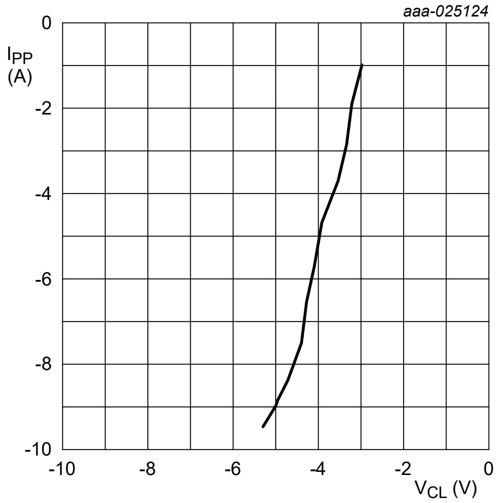
Very Fast Transmission Line Pulse (VF-TLP) = 5 ns

Fig. 15. Negative clamping voltage (VF-TLP); typical values



IEC 61000-4-5; t_p = 8/20 μs; positive pulse

Fig. 16. Dynamic resistance with positive clamping; typical values



IEC 61000-4-5; t_p = 8/20 μs; negative pulse

Fig. 17. Dynamic resistance with negative clamping; typical values

10. Application information

The device is designed for the protection of one bidirectional data line from surge pulses and ESD damage. The device is suitable on lines where the signal polarities are both positive and negative with respect to ground.

The device uses an advanced clamping structure showing a negative dynamic resistance. This snap-back behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid keeping the ESD protection device in snap-back state after exceeding breakdown voltage (due to an ESD pulse for instance).

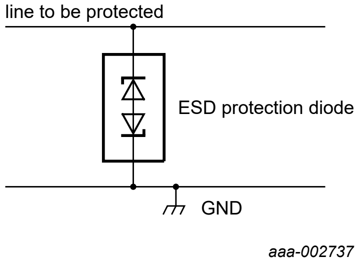


Fig. 18. Application diagram

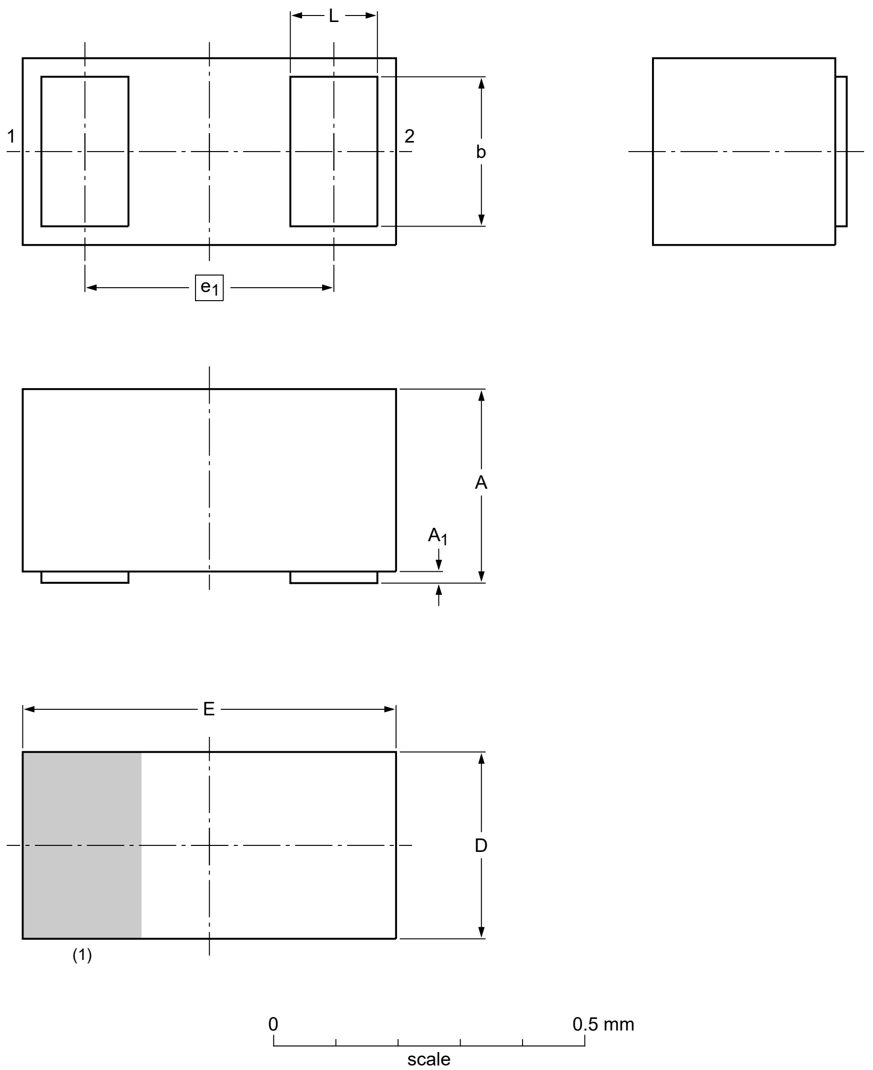
Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

11. Package outline

Leadless ultra small package; 2 terminals; body 0.6 x 0.3 x 0.3 mm **SOD962-2**



Dimensions (mm are the original dimensions)

Unit		A	A_1	b	D	E	e_1	L
mm	max	0.32	0.03	0.25	0.325	0.625		0.15
	nom						0.4	
	min	0.28		0.23	0.275	0.575		0.13

Note
1. The marking bar indicates the cathode.

sod962-2_po

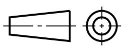
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOD962-2						~~13-07-12~~ 13-07-17

Fig. 19. Package outline DSN0603-2 (SOD962-2)

12. Soldering

Footprint information for reflow soldering of leadless ultra small package; 2 terminals **SOD962-2**

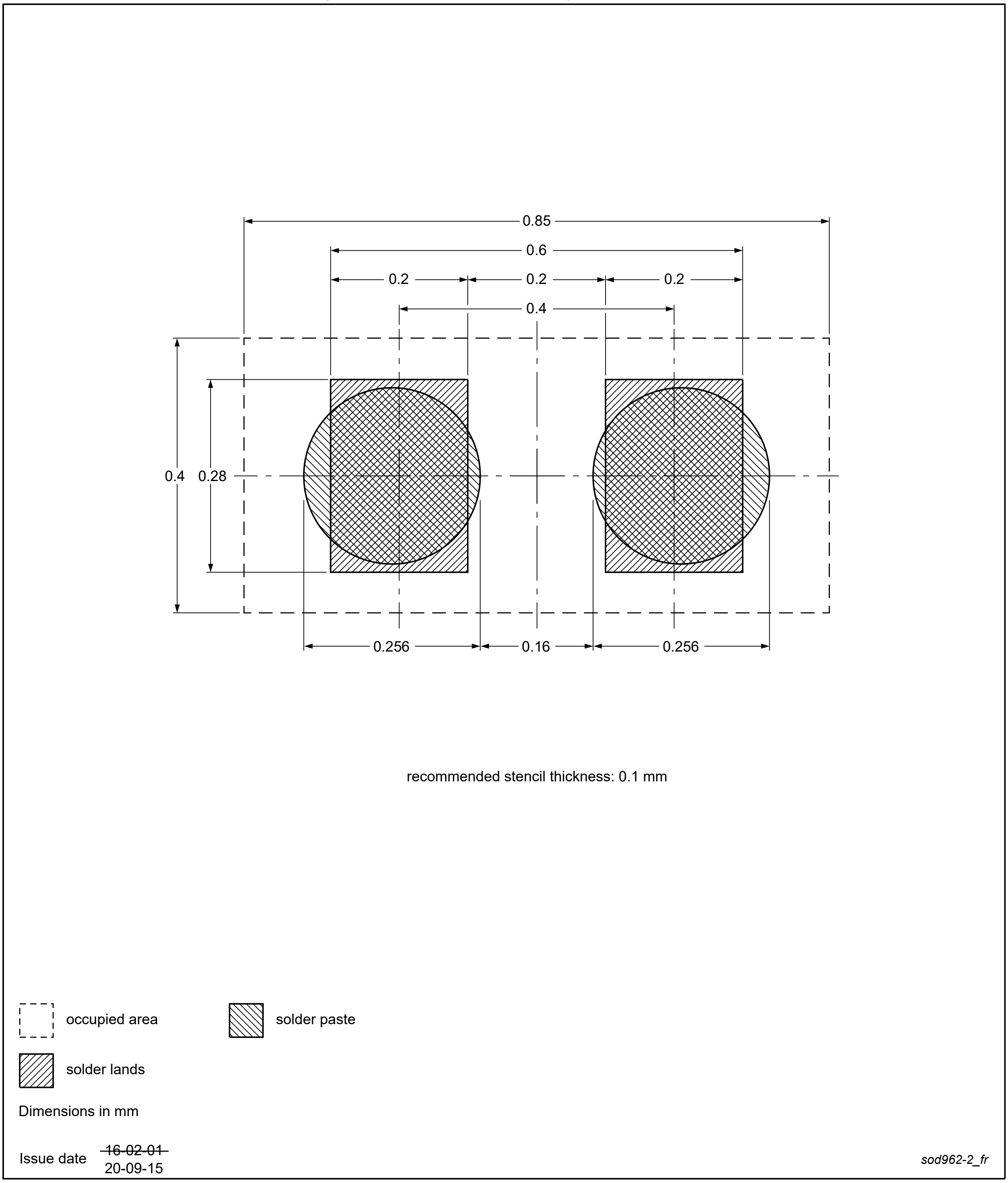


Fig. 20. Reflow soldering footprint for DSN0603-2 (SOD962-2)

13. Revision history

Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PESD4V0Z1BSF v.2	20210302	Product data sheet	-	PESD4V0Z1BSF v.1
Modifications:	• Figure "Reflow soldering footprint" updated			
PESD4V0Z1BSF v.1	20181120	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 2 March 2021