PHPT610030NPK

NPN/PNP high power double bipolar transistor

10 September 2020 Product data sheet

1. General description

NPN/PNP high power double bipolar transistor in a SOT1205 (LFPAK56D) Surface-Mounted Device (SMD) power plastic package.

NPN/NPN complement: PHPT610030NK

PNP/PNP complement: PHPT610030PK

2. Features and benefits

- High thermal power dissipation capability
- Suitable for high temperature applications up to 175 °C
- Reduced Printed-Circuit Board (PCB) requirements comparing to transistors in DPAK
- High energy efficiency due to less heat generation
- AEC-Q101 qualified

3. Applications

- Motor control
- Power management
- Load switch
- Linear mode voltage regulator
- Backlighting applications
- Relay replacement

4. Quick reference data

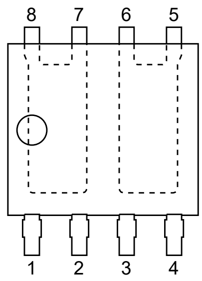
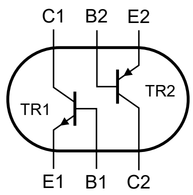
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor; for the PNP transistor with negative polarity							
V_{CEO}	collector-emitter voltage	open base		-	-	100	V
I_C	collector current			-	-	3	A
TR1 (NPN)							
R_{CEsat}	collector-emitter saturation resistance	I_C = 3 A; I_B = 300 mA; $t_p \leq$ 300 µs; pulsed; $\delta \leq$ 0.02; T_{amb} = 25 °C		-	75	110	mΩ
TR2 (PNP)							
R_{CEsat}	collector-emitter saturation resistance	I_C = -2 A; I_B = -200 mA; $t_p \leq$ 300 µs; pulsed; $\delta \leq$ 0.02; T_{amb} = 25 °C		-	110	180	mΩ

nexperia

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	E1	emitter TR1	 **LFPAK56D; Dual LFPAK (SOT1205)**	 *sym139*
2	B1	base TR1		
3	E2	emitter TR2		
4	B2	base TR2		
5	C2	collector TR2		
6	C2	collector TR2		
7	C1	collector TR1		
8	C1	collector TR1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PHPT610030NPK	LFPAK56D; Dual LFPAK	plastic, single ended surface mounted package (LFPAK56D); 8 leads	SOT1205

7. Marking

Table 4. Marking codes

Type number	Marking code
PHPT610030NPK	1003NPK

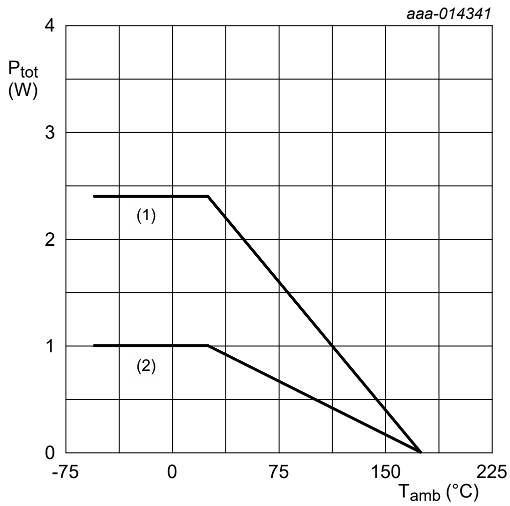
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor; for the PNP transistor with negative polarity						
V_{CBO}	collector-base voltage	open emitter		-	100	V
V_{CEO}	collector-emitter voltage	open base		-	100	V
V_{EBO}	emitter-base voltage	open collector		-	7	V
I_C	collector current			-	3	A
I_{CM}	peak collector current	single pulse; $t_p \leq$ 1 ms		-	8	A
I_B	base current			-	0.5	A
P_{tot}	total power dissipation	$T_{amb} \leq$ 25 °C	[1]	-	1	W
			[2]	-	2.4	W
			[3]	-	25	W
Per device						
P_{tot}	total power dissipation	$T_{amb} \leq$ 25 °C	[1]	-	1.25	W
			[2]	-	3	W
			[4]	-	5	W
T_j	junction temperature			-	175	°C
T_{amb}	ambient temperature			-55	175	°C
T_{stg}	storage temperature			-65	175	°C

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 6 cm^2.
[3] Power dissipation from junction to mounting base.
[4] Device mounted on a ceramic PCB, Al_2O_3, standard footprint.



(1) FR4 PCB, mounting pad for collector 6 cm^2
(2) FR4 PCB, standard footprint

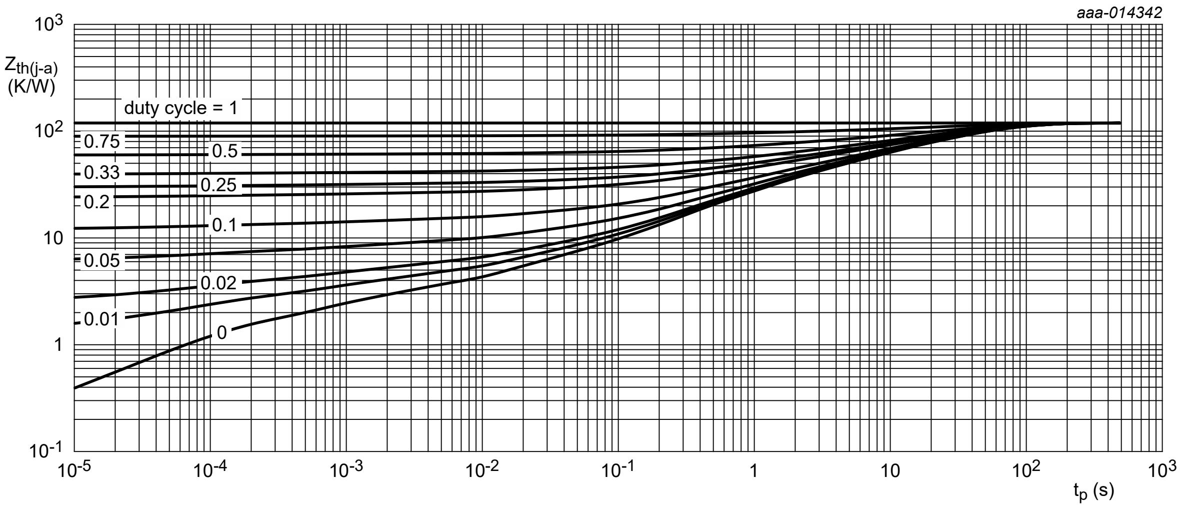
Fig. 1. Per transistor: power derating curves

9. Thermal characteristics

Table 6. Thermal characteristics

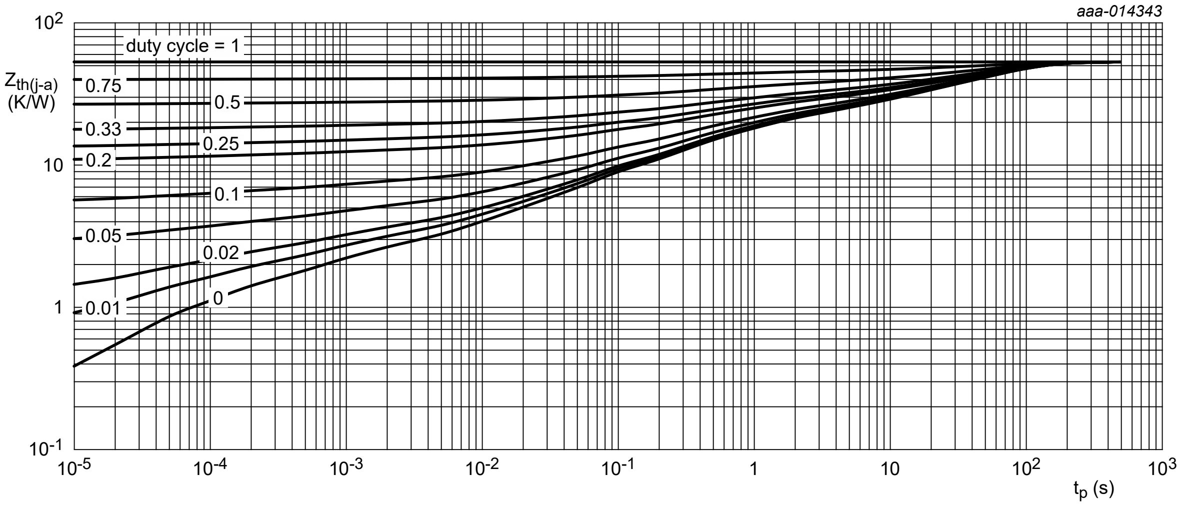
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	150	K/W
			[2]	-	-	62.5	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	-	6	K/W
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	120	K/W
			[2]	-	-	50	K/W
			[3]	-	-	30	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 6 cm^2.
[3] Device mounted on a ceramic PCB, Al_2O_3, standard footprint.



FR4 PCB, standard footprint

Fig. 2. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, mounting pad for collector 6 cm^2

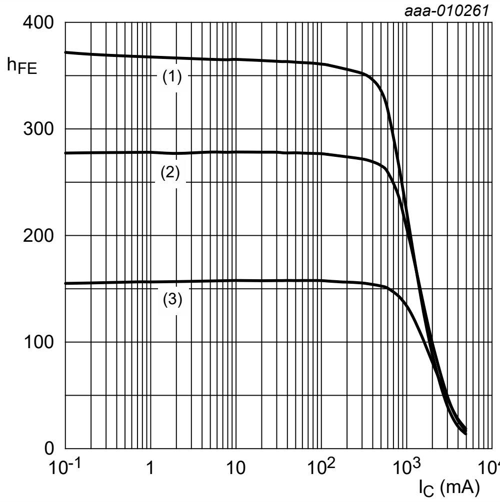
Fig. 3. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

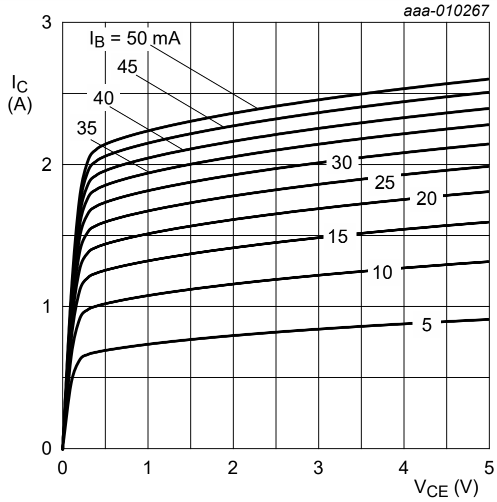
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
TR1 (NPN)							
I_{CBO}	collector-base cut-off current	V_{CB} = 80 V; I_E = 0 A; T_{amb} = 25 °C		-	-	100	nA
		V_{CB} = 80 V; I_E = 0 A; T_j = 150 °C		-	-	50	μA
I_{CES}	collector-emitter cut-off current	V_{CE} = 80 V; V_{BE} = 0 V		-	-	100	nA
I_{EBO}	emitter-base cut-off current	V_{EB} = 7 V; I_C = 0 A; T_{amb} = 25 °C		-	-	100	nA
h_{FE}	DC current gain	V_{CE} = 10 V; I_C = 500 mA; $t_p \leq$ 300 μs; pulsed; $\delta \leq$ 0.02; T_{amb} = 25 °C		150	250	-	
		V_{CE} = 10 V; I_C = 1 A; $t_p \leq$ 300 μs; pulsed; $\delta \leq$ 0.02; T_{amb} = 25 °C		80	250	-	
		V_{CE} = 10 V; I_C = 2 A; $t_p \leq$ 300 μs; pulsed; $\delta \leq$ 0.02; T_{amb} = 25 °C		20	100	-	
		V_{CE} = 10 V; I_C = 3 A; $t_p \leq$ 300 μs; pulsed; $\delta \leq$ 0.02; T_{amb} = 25 °C		10	40	-	
V_{CEsat}	collector-emitter saturation voltage	I_C = 1 A; I_B = 50 mA; $t_p \leq$ 300 μs; pulsed; $\delta \leq$ 0.02; T_{amb} = 25 °C		-	90	150	mV
		I_C = 3 A; I_B = 0.3 A; $t_p \leq$ 300 μs; pulsed; $\delta \leq$ 0.02; T_{amb} = 25 °C		-	225	330	mV
R_{CEsat}	collector-emitter saturation resistance	I_C = 3 A; I_B = 300 mA; $t_p \leq$ 300 μs; pulsed; $\delta \leq$ 0.02; T_{amb} = 25 °C		-	75	110	mΩ
V_{BEsat}	base-emitter saturation voltage	I_C = 1 A; I_B = 50 mA; $t_p \leq$ 300 μs; pulsed; $\delta \leq$ 0.02; T_{amb} = 25 °C		-	0.86	1	V
		I_C = 2 A; I_B = 200 mA; $t_p \leq$ 300 μs; pulsed; $\delta \leq$ 0.02; T_{amb} = 25 °C		-	1	1.2	V
V_{BEon}	base-emitter turn-on voltage	V_{CE} = 2 V; I_C = 100 mA; $t_p \leq$ 300 μs; pulsed; $\delta \leq$ 0.02; T_{amb} = 25 °C		-	0.67	0.85	V
t_d	delay time	V_{CC} = 12.5 V; I_C = 1 A; I_{Bon} = 50 mA; I_{Boff} = -50 mA; T_{amb} = 25 °C		-	20	-	ns
t_r	rise time			-	300	-	ns
t_{on}	turn-on time			-	320	-	ns
t_s	storage time			-	830	-	ns
t_f	fall time			-	470	-	ns
t_{off}	turn-off time			-	1300	-	ns
f_T	transition frequency	V_{CE} = 10 V; I_C = 100 mA; f = 100 MHz; T_{amb} = 25 °C		-	140	-	MHz
C_c	collector capacitance	V_{CB} = 10 V; I_E = 0 A; i_e = 0 A; f = 1 MHz; T_{amb} = 25 °C		-	11	-	pF
TR2 (PNP)							
I_{CBO}	collector-base cut-off current	V_{CB} = -80 V; I_E = 0 A		-	-	-100	nA
		V_{CB} = -80 V; I_E = 0 A; T_j = 150 °C		-	-	-50	μA
I_{CES}	collector-emitter cut-off current	V_{CE} = -80 V; V_{BE} = 0 V		-	-	-100	nA
I_{EBO}	emitter-base cut-off current	V_{EB} = -7 V; I_C = 0 A		-	-	-100	nA

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
h_{FE}	DC current gain	V_{CE} = -10 V; I_C = -500 mA; T_{amb} = 25 °C		150	200	-	
		V_{CE} = -10 V; I_C = -1 A; $t_p \leq$ 300 µs; pulsed; $\delta \leq$ 0.02; T_{amb} = 25 °C		80	210	-	
		V_{CE} = -10 V; I_C = -2 A; $t_p \leq$ 300 µs; pulsed; $\delta \leq$ 0.02; T_{amb} = 25 °C		20	100	-	
		V_{CE} = -10 V; I_C = -3 A; $t_p \leq$ 300 µs; pulsed; $\delta \leq$ 0.02; T_{amb} = 25 °C		10	40	-	
V_{CEsat}	collector-emitter saturation voltage	I_C = -500 mA; I_B = -50 mA; T_{amb} = 25 °C		-	-70	-110	mV
		I_C = -2 A; I_B = -0.2 A; $t_p \leq$ 300 µs; pulsed; $\delta \leq$ 0.02; T_{amb} = 25 °C		-	-220	-360	mV
R_{CEsat}	collector-emitter saturation resistance	I_C = -2 A; I_B = -200 mA; $t_p \leq$ 300 µs; pulsed; $\delta \leq$ 0.02; T_{amb} = 25 °C		-	110	180	mΩ
V_{BEsat}	base-emitter saturation voltage	I_C = -1 A; I_B = -50 mA; $t_p \leq$ 300 µs; pulsed; $\delta \leq$ 0.02; T_{amb} = 25 °C		-	-0.91	-1	V
		I_C = -2 A; I_B = -200 mA; $t_p \leq$ 300 µs; pulsed; $\delta \leq$ 0.02; T_{amb} = 25 °C		-	-1.02	-1.2	V
V_{BEon}	base-emitter turn-on voltage	V_{CE} = -2 V; I_C = -100 mA; $t_p \leq$ 300 µs; pulsed; $\delta \leq$ 0.02; T_{amb} = 25 °C		-	-0.68	-0.9	V
t_d	delay time	V_{CC} = -12.5 V; I_C = -1 A; I_{Bon} = -50 mA; I_{Boff} = 50 mA; T_{amb} = 25 °C		-	20	-	ns
t_r	rise time			-	180	-	ns
t_{on}	turn-on time			-	200	-	ns
t_s	storage time			-	350	-	ns
t_f	fall time			-	220	-	ns
t_{off}	turn-off time			-	570	-	ns
f_T	transition frequency	V_{CE} = -10 V; I_C = -100 mA; f = 100 MHz; T_{amb} = 25 °C		-	125	-	MHz
C_c	collector capacitance	V_{CB} = -10 V; I_E = 0 A; i_e = 0 A; f = 1 MHz; T_{amb} = 25 °C		-	30	-	pF



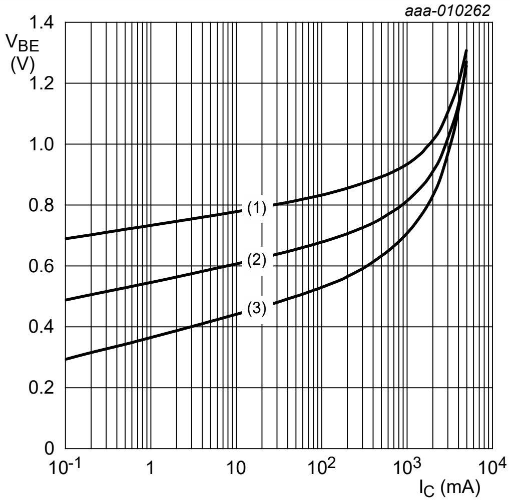
V_{CE} = 10 V
(1) T_{amb} = 100 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = −55 °C

Fig. 4. TR1 (NPN): DC current gain as a function of collector current; typical values



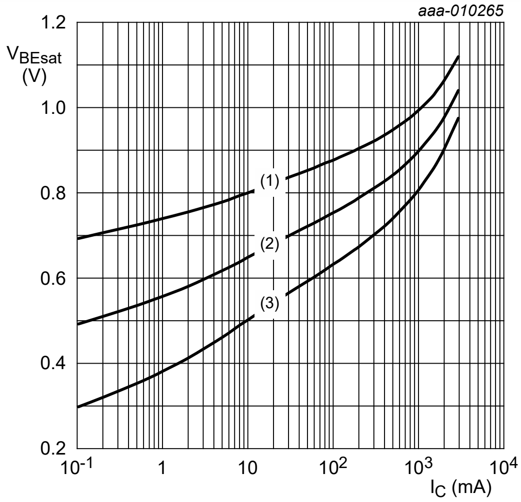
T_{amb} = 25 °C

Fig. 5. TR1 (NPN): Collector current as a function of collector-emitter voltage; typical values



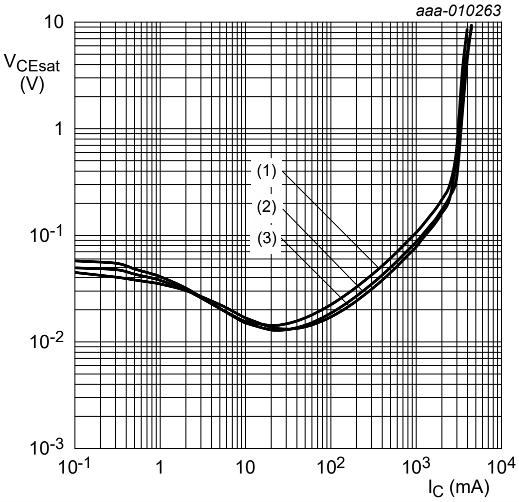
V_{CE} = 2 V
(1) T_{amb} = −55 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 100 °C

Fig. 6. TR1 (NPN): Base-emitter voltage as a function of collector current; typical values



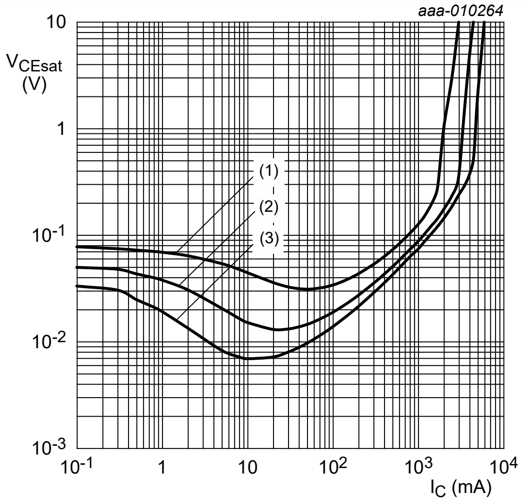
I_C/I_B = 20
(1) T_{amb} = −55 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 100 °C

Fig. 7. TR1 (NPN): Base-emitter saturation voltage as a function of collector current; typical values



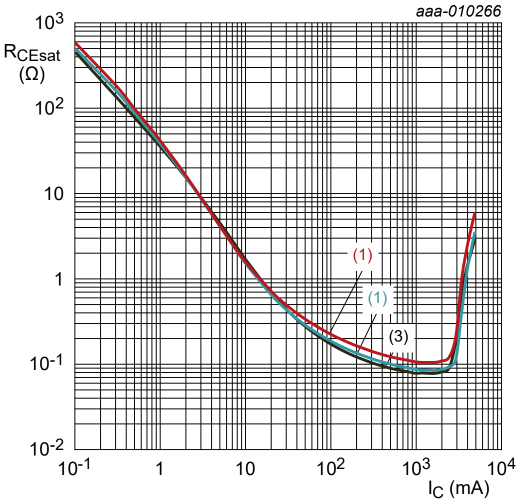
I_C/I_B = 20
(1) T_{amb} = 100 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = −55 °C

Fig. 8. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values



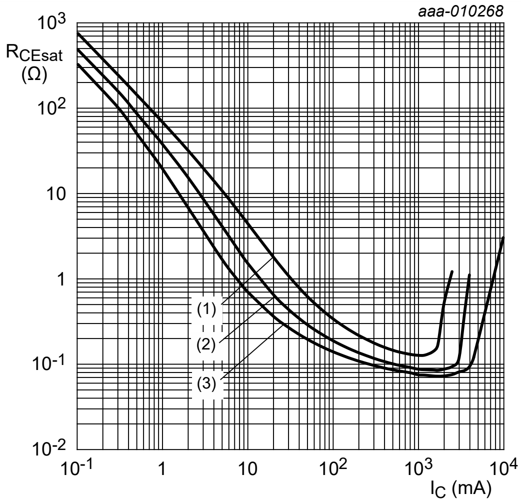
T_{amb} = 25 °C
(1) I_C/I_B = 50
(2) I_C/I_B = 20
(3) I_C/I_B = 10

Fig. 9. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values



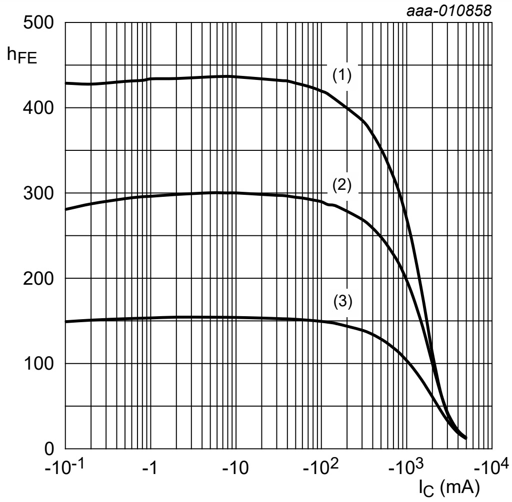
I_C/I_B = 20
(1) T_{amb} = 100 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = −55 °C

Fig. 10. TR1 (NPN): Collector-emitter saturation resistance as a function of collector current; typical values



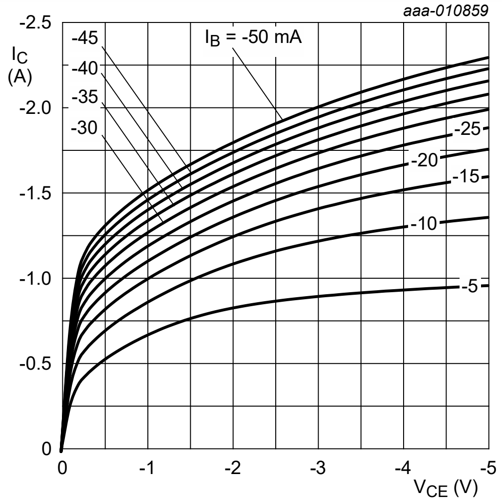
T_{amb} = 25 °C
(1) I_C/I_B = 50
(2) I_C/I_B = 20
(3) I_C/I_B = 10

Fig. 11. TR1 (NPN): Collector-emitter saturation resistance as a function of collector current; typical values



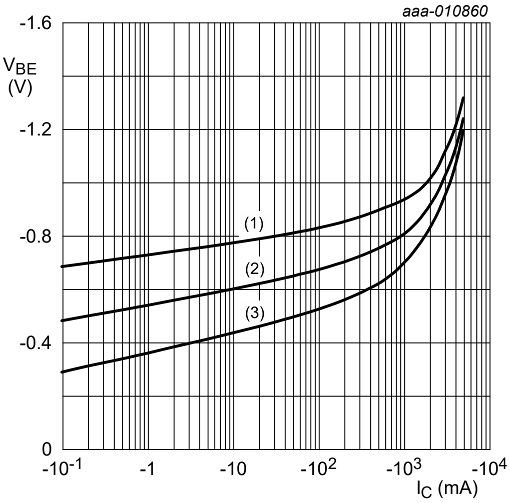
V_{CE} = −10 V
(1) T_{amb} = 100 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = −55 °C

Fig. 12. TR2 (PNP): DC current gain as a function of collector current; typical values



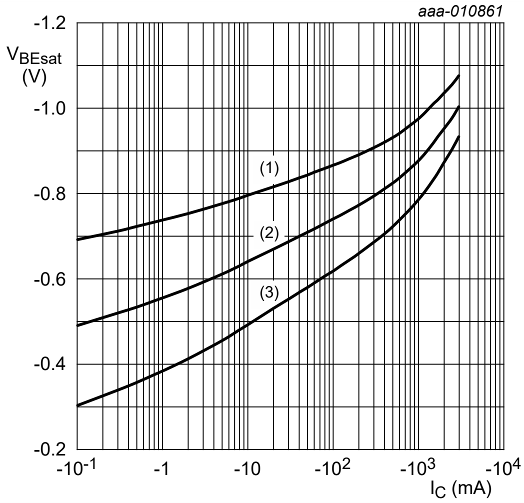
T_{amb} = 25 °C

Fig. 13. TR2 (PNP): Collector current as a function of collector-emitter voltage; typical values



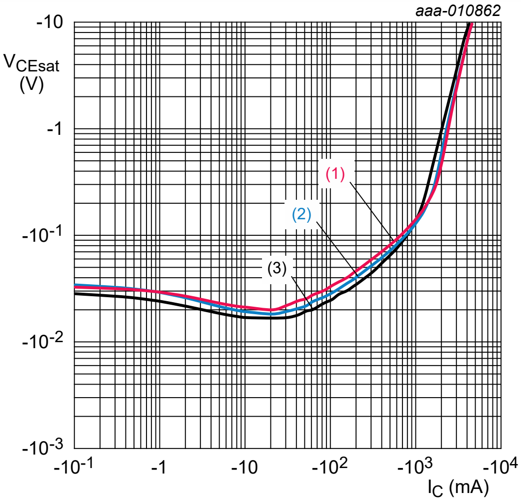
$V_{CE} = -2$ V
(1) $T_{amb} = -55$ °C
(2) $T_{amb} = 25$ °C
(3) $T_{amb} = 100$ °C

Fig. 14. TR2 (PNP): Base-emitter voltage as a function of collector current; typical values



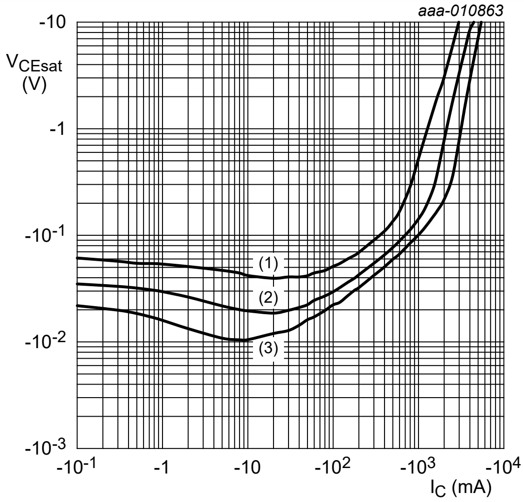
$I_C/I_B = 20$
(1) $T_{amb} = -55$ °C
(2) $T_{amb} = 25$ °C
(3) $T_{amb} = 100$ °C

Fig. 15. TR2 (PNP): Base-emitter saturation voltage as a function of collector current; typical values



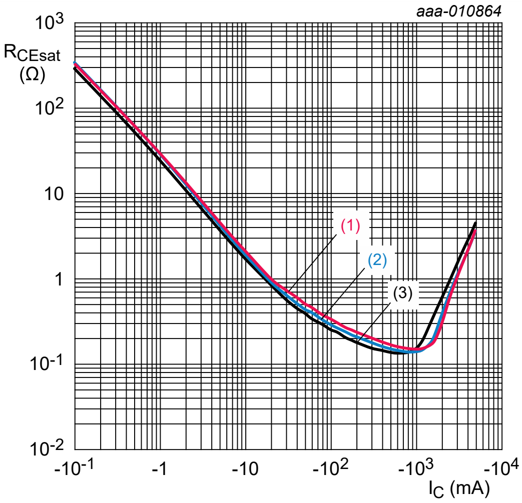
$I_C/I_B = 20$
(1) $T_{amb} = 100$ °C
(2) $T_{amb} = 25$ °C
(3) $T_{amb} = -55$ °C

Fig. 16. TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values



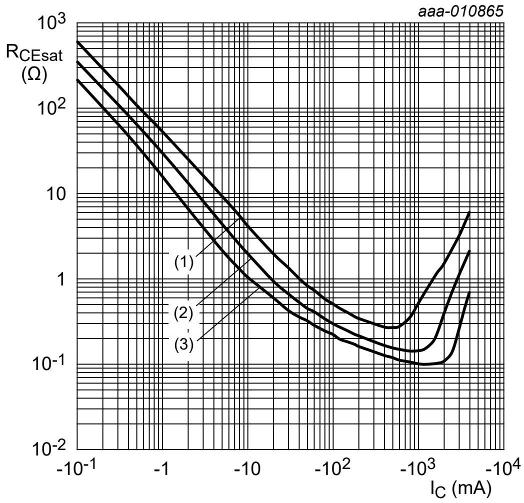
$T_{amb} = 25$ °C
(1) $I_C/I_B = 50$
(2) $I_C/I_B = 20$
(3) $I_C/I_B = 10$

Fig. 17. TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values



$I_C/I_B = 20$
(1) T_{amb} = 100 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = −55 °C

Fig. 18. TR2 (PNP): Collector-emitter saturation resistance as a function of collector current; typical values



T_{amb} = 25 °C
(1) $I_C/I_B = 50$
(2) $I_C/I_B = 20$
(3) $I_C/I_B = 10$

Fig. 19. TR2 (PNP): Collector-emitter saturation resistance as a function of collector current; typical values

11. Test information

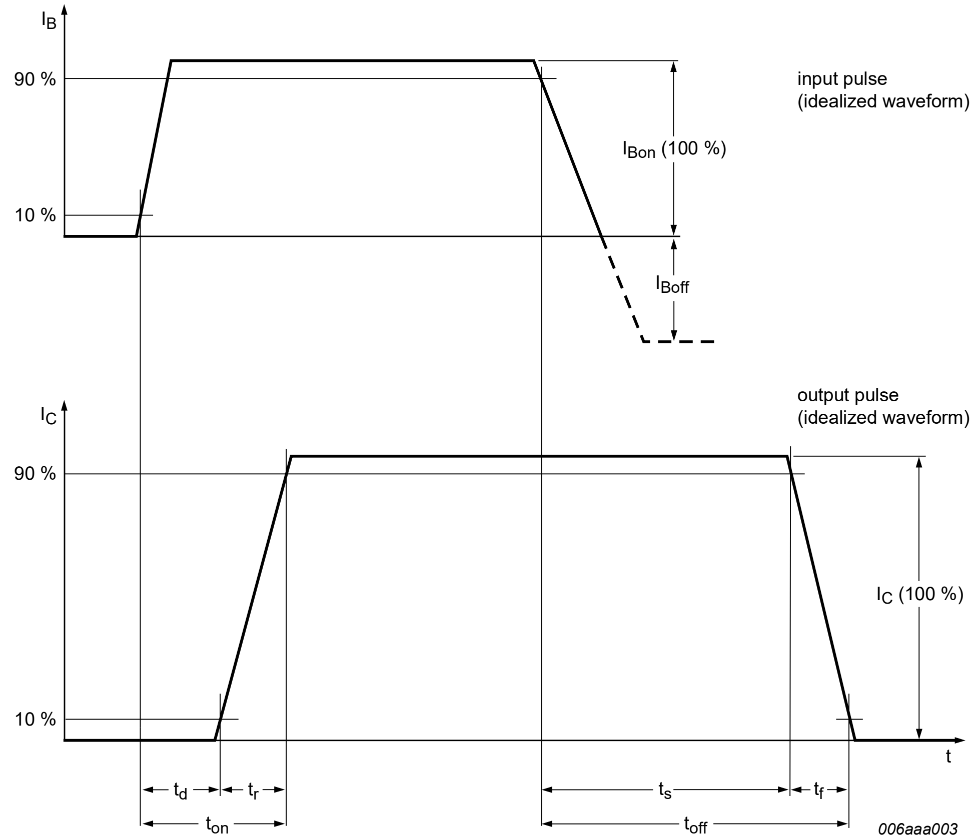


Fig. 20. TR1 (NPN): BISS transistor switching time definition

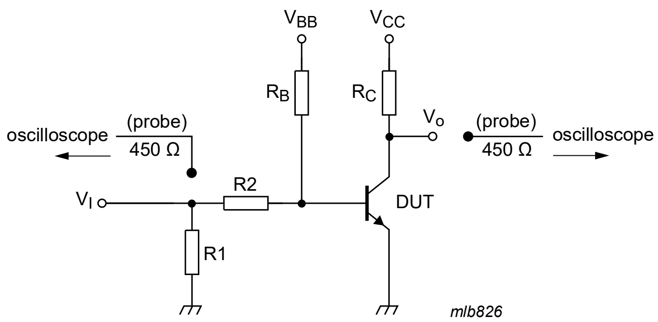


Fig. 21. TR1 (NPN): Test circuit for switching times

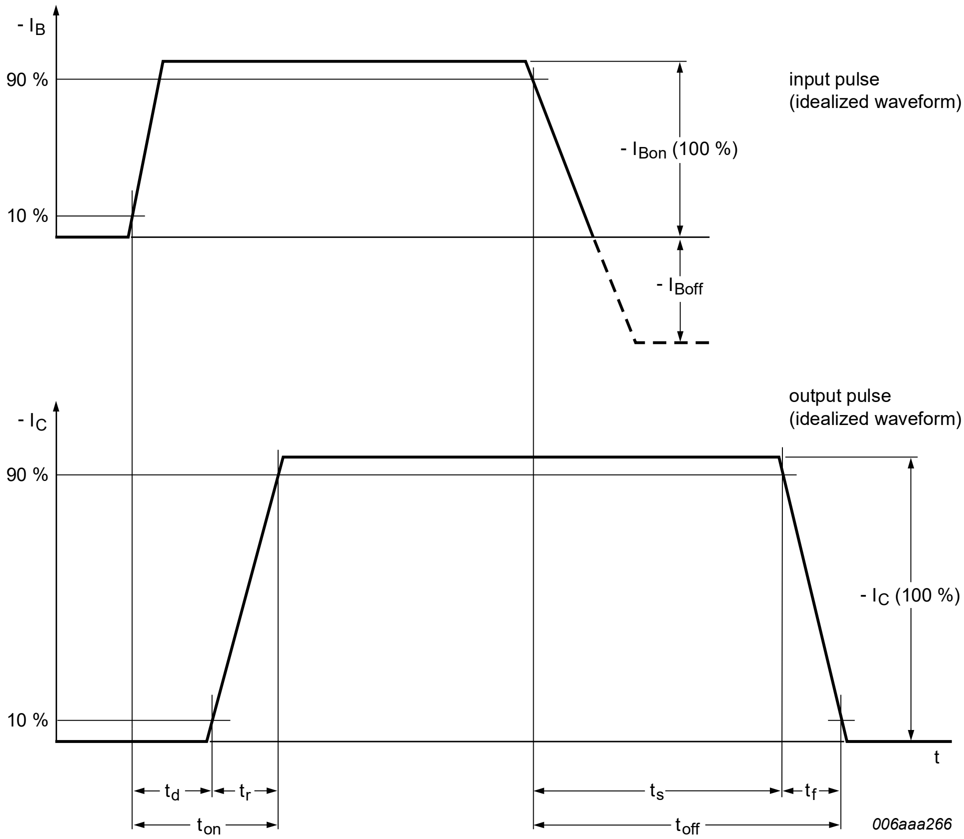


Fig. 22. TR2 (PNP): BISS transistor switching time definition

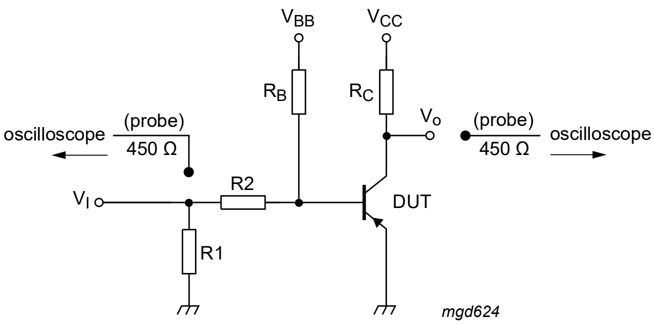


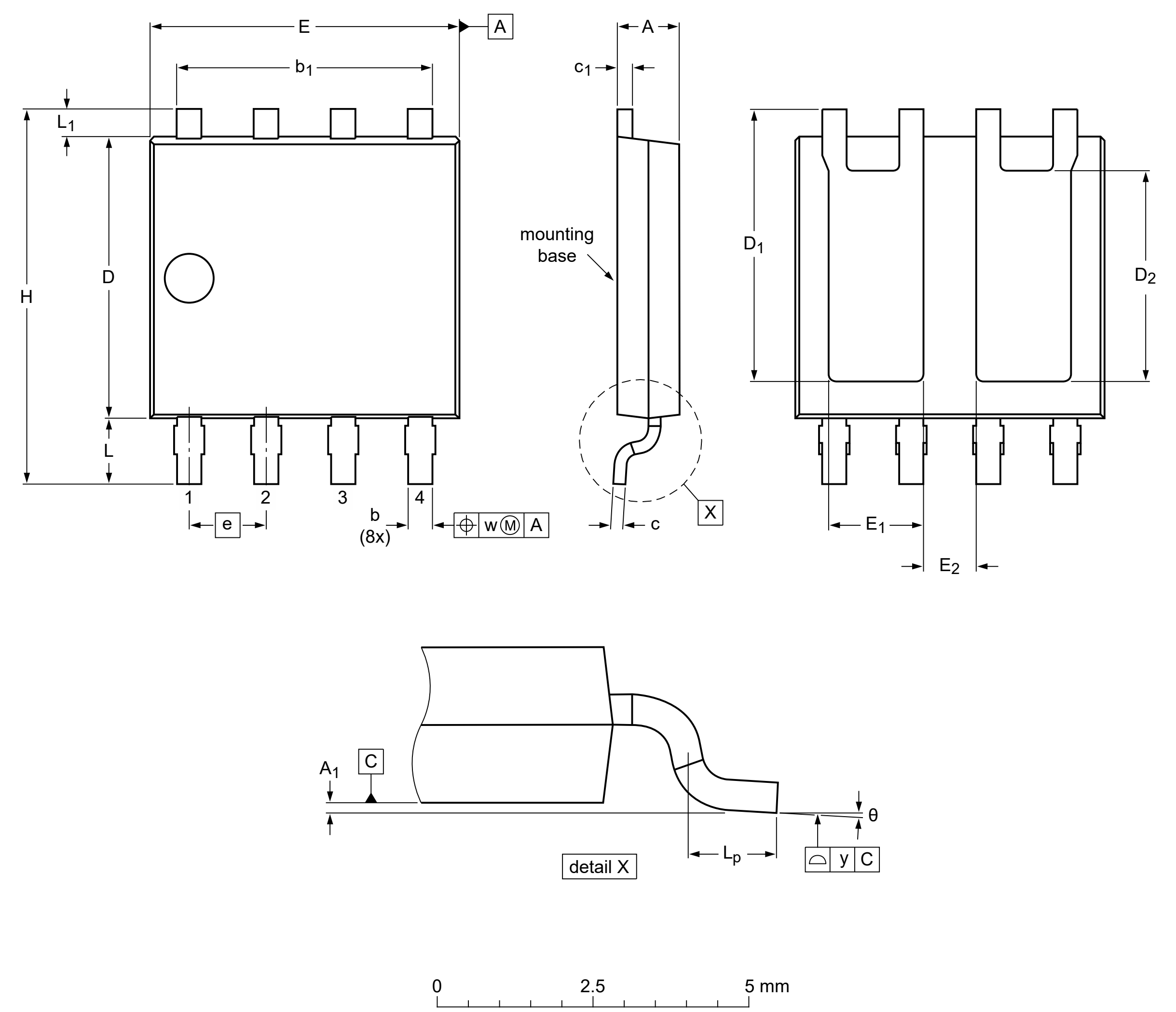
Fig. 23. TR2 (PNP): Test circuit for switching times

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

Plastic single ended surface mounted package LFPAK56D; 8 leads **SOT1205**



Dimensions

Unit		A	A_1	b	b_1	c	c_1	$D^{(1)}$	$D_1^{(1)}$	D_2 (ref)	$E^{(1)}$	$E_1^{(1)}$	E_2	e	H	L	L_1	L_p	w	y	θ
mm	max	1.05	0.1	0.50	4.4	0.25	0.30	4.70	4.55	3.5	5.30	1.8	0.85		6.2	1.3	0.55	0.85			8°
	nom													1.27					0.25	0.1	
	min	1.02	0.0	0.35	4.1	0.19	0.24	4.45	4.35	3.4	4.95	1.6	0.60		5.9	0.8	0.30	0.40			0°

Note
1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

sot1205_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1205						~~14-08-21~~ 14-10-28

Fig. 24. Package outline LFPAK56D; Dual LFPAK (SOT1205)

13. Soldering

Footprint information for reflow soldering of LFPAK56D package **SOT1205**

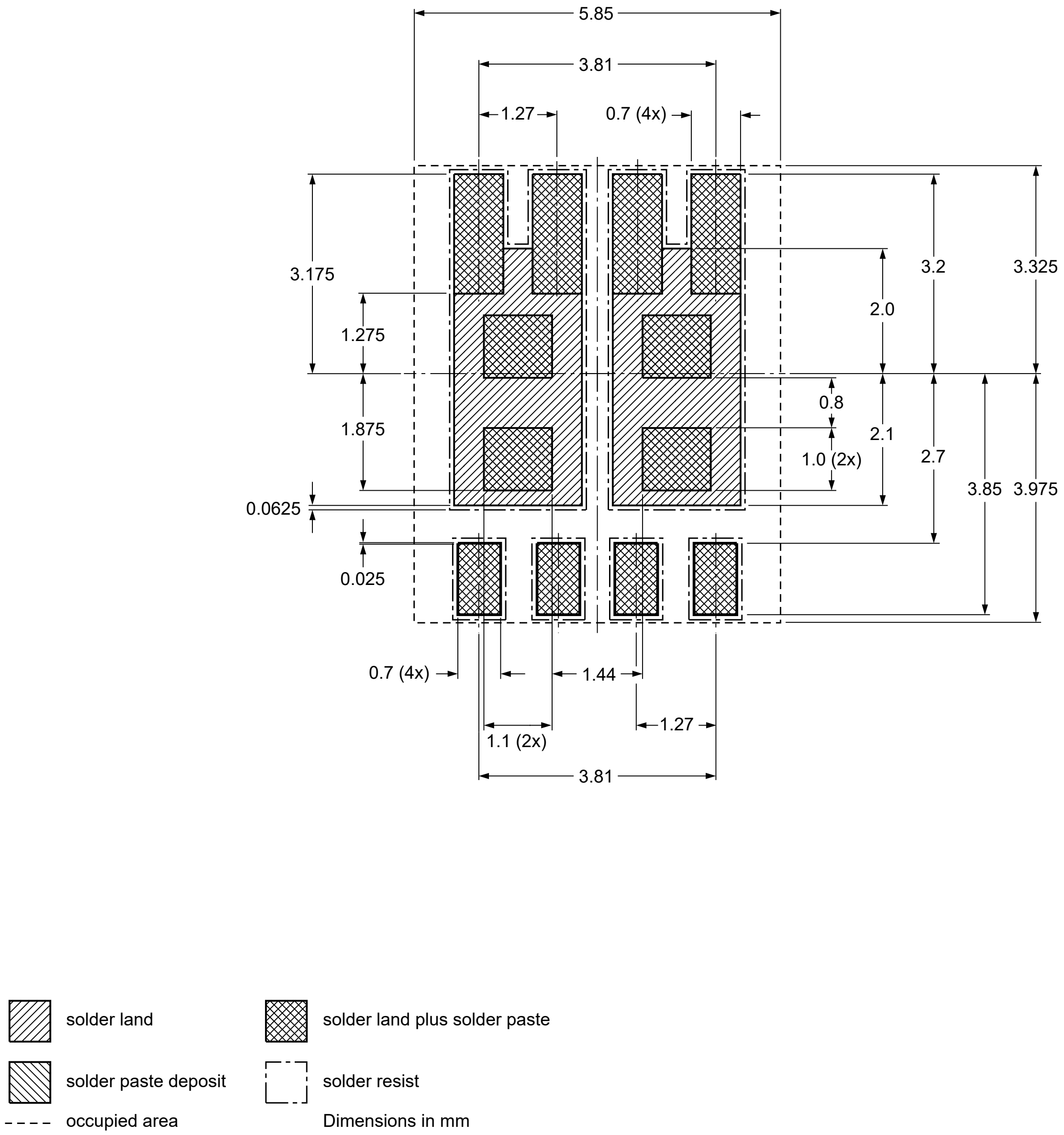


Fig. 25. Reflow soldering footprint for LFPAK56D; Dual LFPAK (SOT1205)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PHPT610030NPK v.2	20200910	Product data sheet	-	PHPT610030NPK v.1
Modifications:	• Characteristics: Figures 6, 7, 8 and 10 corrected			
PHPT610030NPK v.1	20141014	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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