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Kind regards,

Team Nexperia



# NPN/NPN high-voltage double transistors Rev. 02 — 27 August 2009

Product data sheet

#### 1. **Product profile**

### **1.1 General description**

NPN/NPN high-voltage double transistors in a small SOT457 (SC-74) Surface Mounted Device (SMD) plastic package.

### 1.2 Features

- High breakdown voltage
- Two electrically isolated transistors
- Small SMD plastic package

### 1.3 Applications

- Automotive:
  - High- and low-side switches
  - Voltage regulators
- Communication: Telecom line interface
- Consumer: CRT TV
- Computing: Monitors

### 1.4 Quick reference data

#### Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Per transis	tor					
V <sub>CEO</sub>	collector-emitter voltage	open base	-	-	300	V
I <sub>C</sub>	collector current		-	-	100	mA
I <sub>CM</sub>	peak collector current	single pulse; $t_p \leq 1 \text{ ms}$	-	-	200	mA



NPN/NPN high-voltage double transistors

# 2. Pinning information

Table 2.	Pinning		
Pin	Description	Simplified outline	Symbol
1	emitter TR1		
2	base TR2		
3	collector TR2	0	
4	emitter TR2		
5	base TR1		
6	collector TR1		1 2 3 <i>006aaa677</i>

# 3. Ordering information

Table 3. Order	ing informa	ition	
Type number	Package		
	Name	Description	Version
PMBTA42DS	SC-74	plastic surface mounted package (TSOP6); 6 leads	SOT457

### 4. Marking

Table 4.	Marking codes	
Type num	iber	Marking code
PMBTA42	DS	P4

# 5. Limiting values

#### Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Per transis	stor				
V <sub>CBO</sub>	collector-base voltage	open emitter	-	300	V
V <sub>CEO</sub>	collector-emitter voltage	open base	-	300	V
V <sub>EBO</sub>	emitter-base voltage	open collector	-	6	V
I <sub>C</sub>	collector current		-	100	mA
I <sub>CM</sub>	peak collector current	single pulse; t <sub>p</sub> ≤ 1 ms	-	200	mA
I <sub>BM</sub>	peak base current	single pulse; t <sub>p</sub> ≤ 1 ms	-	100	mA
P <sub>tot</sub>	total power dissipation	$T_{amb} \le 25 \ ^{\circ}C$	<u>[1]</u> _	290	mW
			[2] _	370	mW
			[3] _	450	mW

#### NPN/NPN high-voltage double transistors

Table 5.	Limiting	values	continued
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In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Per device					
P <sub>tot</sub>	total power dissipation	$T_{amb} \le 25 \ ^{\circ}C$	<u>[1]</u> _	420	mW
			[2] _	560	mW
			<u>[3]</u>	700	mW
Tj	junction temperature		-	150	°C
T <sub>amb</sub>	ambient temperature		-65	+150	°C
T <sub>stg</sub>	storage temperature		-65	+150	°C
-					

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1cm<sup>2</sup>.

[3] Device mounted on a ceramic PCB, Al<sub>2</sub>O<sub>3</sub>, standard footprint.

### 6. Thermal characteristics

Thermal characteristics					
Parameter	Conditions	Min	Тур	Max	Unit
istor					
thermal resistance from	in free air	<u>[1]</u> _	-	431	K/W
junction to ambient		[2] _	-	338	K/W
		[3] _	-	278	K/W
thermal resistance from junction to solder point		-	-	105	K/W
e					
thermal resistance from	in free air	<u>[1]</u> _	-	298	K/W
junction to ambient		[2] _	-	223	K/W
		[3] _	-	179	K/W
	Parameter         istor         thermal resistance from junction to ambient         thermal resistance from junction to solder point         e         thermal resistance from	Parameter       Conditions         istor       in free air         thermal resistance from junction to ambient       in free air         thermal resistance from junction to solder point       e         thermal resistance from in free air       in free air	ParameterConditionsMinistorthermal resistance from junction to ambientin free air[1] -[2] -[3] -thermal resistance from junction to solder point-ethermal resistance from junction to ambientin free air[1] -[2] -[1] -[2] -[1] -[2] -[1] -[2] -[1] -[2] -[2] -	ParameterConditionsMinTypistorthermal resistance from junction to ambientin free air[1]-[2][3][3]thermal resistance from junction to solder pointethermal resistance from junction to ambientin free air[1]-e[2][2]	ParameterConditionsMinTypMaxistorthermal resistance from junction to ambientin free air[1]431[2]338[3]278thermal resistance from junction to solder point-105e-298junction to ambient[1]223

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

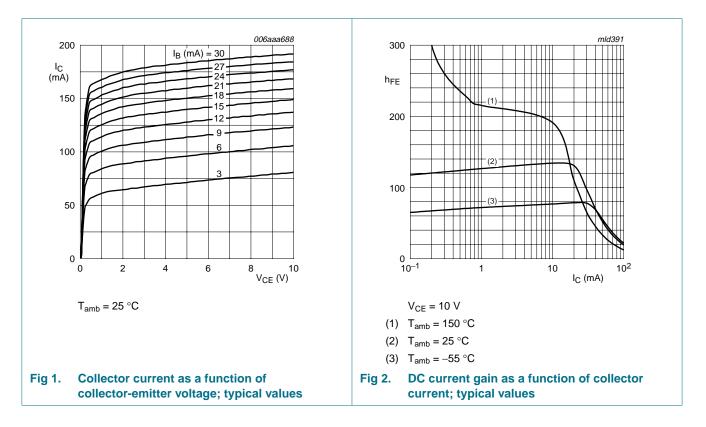
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1cm<sup>2</sup>.

[3] Device mounted on a ceramic PCB, Al<sub>2</sub>O<sub>3</sub>, standard footprint.

NPN/NPN high-voltage double transistors

### 7. Characteristics

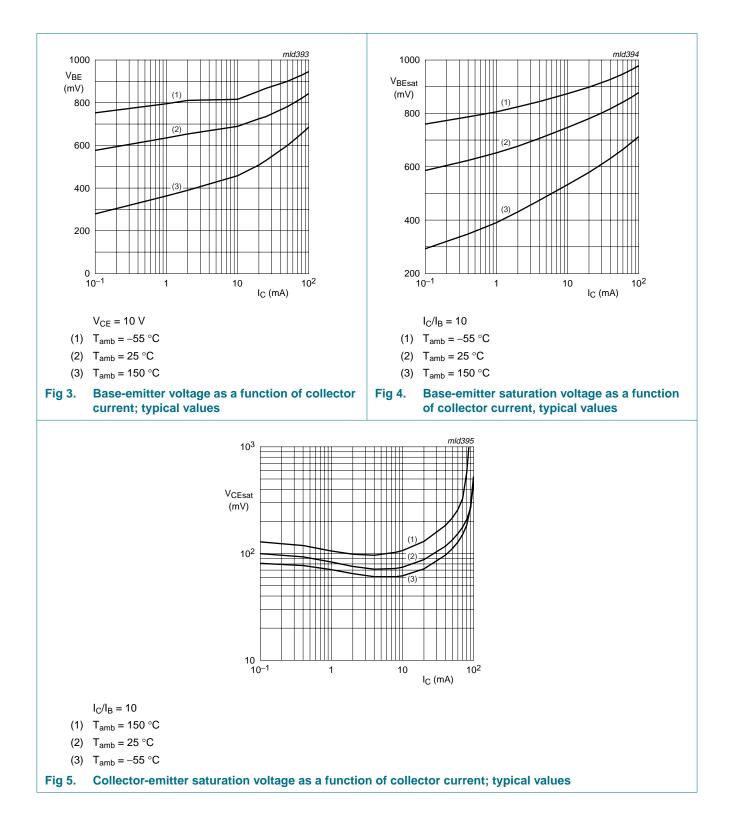
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Per trans	istor					
I <sub>CBO</sub>	collector-base cut-off current	$V_{CB} = 200 \text{ V}; I_E = 0 \text{ A}$	-	-	100	nA
I <sub>EBO</sub>	emitter-base cut-off current	$V_{EB} = 6 V; I_C = 0 A$	-	-	100	nA
h <sub>FE</sub> DC current gain	DC current gain	$V_{CE} = 10 \text{ V}; I_{C} = 1 \text{ mA}$	25	-	-	
	$V_{CE} = 10 \text{ V}; I_{C} = 10 \text{ mA}$	40	-	-		
		$V_{CE}$ = 10 V; $I_{C}$ = 30 mA	40	-	-	
V <sub>CEsat</sub>	collector-emitter saturation voltage	$I_{C} = 20 \text{ mA}; I_{B} = 2 \text{ mA}$	-	-	500	mV
V <sub>BEsat</sub>	base-emitter saturation voltage	$I_{C} = 20 \text{ mA}; I_{B} = 2 \text{ mA}$	-	-	900	mV
C <sub>re</sub>	feedback capacitance	$\label{eq:VCB} \begin{array}{l} V_{CB} = 20 \; V; \; I_{C} = i_{c} = 0 \; A; \\ f = 1 \; MHz \end{array}$	-	-	3	pF
f <sub>T</sub>	transition frequency	V <sub>CE</sub> = 20 V; I <sub>C</sub> = 10 mA; f = 100 MHz	50	-	-	MHz



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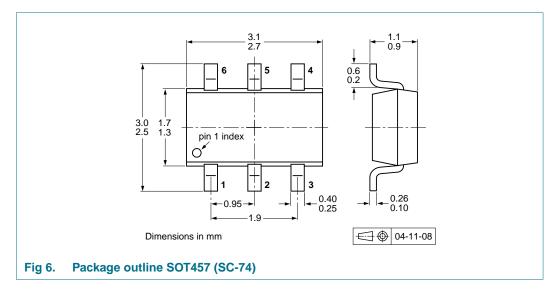
# PMBTA42DS

#### NPN/NPN high-voltage double transistors



NPN/NPN high-voltage double transistors

### 8. Package outline



# 9. Packing information

#### Table 8.Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code.[1]

Type number Package		Description		Packing quantity	
				3000	10000
PMBTA42DS	SOT457	4 mm pitch, 8 mm tape and reel; T1	[2]	-115	-135
		4 mm pitch, 8 mm tape and reel; T2	[3]	-125	-165

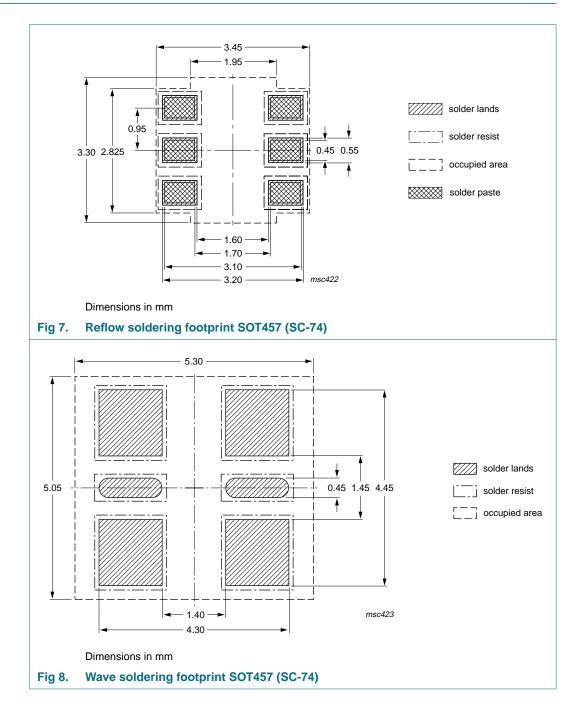
[1] For further information and the availability of packing methods, see <u>Section 13</u>.

[2] T1: normal taping

[3] T2: reverse taping

#### NPN/NPN high-voltage double transistors

### **10. Soldering**



### NPN/NPN high-voltage double transistors

# **11. Revision history**

Table 9. Revision hi	story			
Document ID	Release date	Data sheet status	Change notice	Supersedes
PMBTA42DS_2	20090827	Product data sheet	-	PMBTA42DS_1
Modifications:		eet was changed to reflect w legal definitions and disc	• •	
	<ul> <li>Figure 8 "Wa</li> </ul>	ave soldering footprint SOT	457 (SC-74)":updated	l
PMBTA42DS_1	20060106	Product data sheet	-	-

#### NPN/NPN high-voltage double transistors

### **12. Legal information**

### 12.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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PMBTA42DS\_2 Product data sheet

#### NPN/NPN high-voltage double transistors

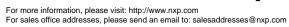
### 14. Contents

1	Product profile 1
1.1	General description
1.2	Features
1.3	Applications 1
1.4	Quick reference data 1
2	Pinning information 2
3	Ordering information 2
4	Marking 2
5	Limiting values 2
6	Thermal characteristics 3
7	Characteristics 4
8	Package outline 6
9	Packing information 6
10	Soldering 7
11	Revision history 8
12	Legal information 9
12.1	Data sheet status 9
12.2	Definitions
12.3	Disclaimers
12.4	Trademarks
13	Contact information
14	Contents 10

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Date of release: 27 August 2009 Document identifier: PMBTA42DS\_2



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