

PMCXB290UE

20 V, complementary N/P-channel Trench MOSFET

30 May 2023

Product data sheet

1. General description

Complementary N/P-channel enhancement mode Field-Effect Transistor (FET) in a leadless ultra small DFN1010B-6 (SOT1216) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Low threshold voltage
- Very fast switching
- Trench MOSFET technology
- ElectroStatic Discharge (ESD) protection typically > 2 kV HBM

3. Applications

- Relay driver
- High-speed line driver
- Level shifter
- Power management in battery-driven portables

4. Quick reference data

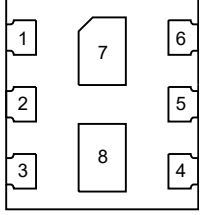
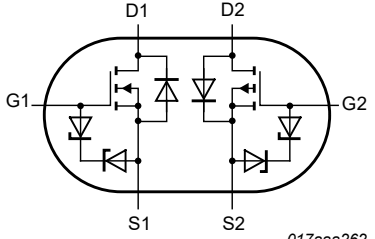
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TR1 (N-channel), Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 1.2 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	270	320	m Ω
TR2 (P-channel), Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = -4.5 \text{ V}; I_D = -1.2 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	590	770	m Ω
TR1 (N-channel)						
V_{DS}	drain-source voltage	$T_j = 25 \text{ }^\circ\text{C}$	-	-	20	V
I_D	drain current	$V_{GS} = 4.5 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}$	[1]	-	930	mA
TR2 (P-channel)						
V_{DS}	drain-source voltage	$T_j = 25 \text{ }^\circ\text{C}$	-	-	-20	V
I_D	drain current	$V_{GS} = -4.5 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}$	[1]	-	-570	mA

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm².

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source TR1	 <p>Transparent top view DFN1010B-6 (SOT1216)</p>	 <p>017aaa262</p>
2	G1	gate TR1		
3	D2	drain TR2		
4	S2	source TR2		
5	G2	gate TR2		
6	D1	drain TR1		
7	D1	drain TR1		
8	D2	drain TR2		

6. Ordering information

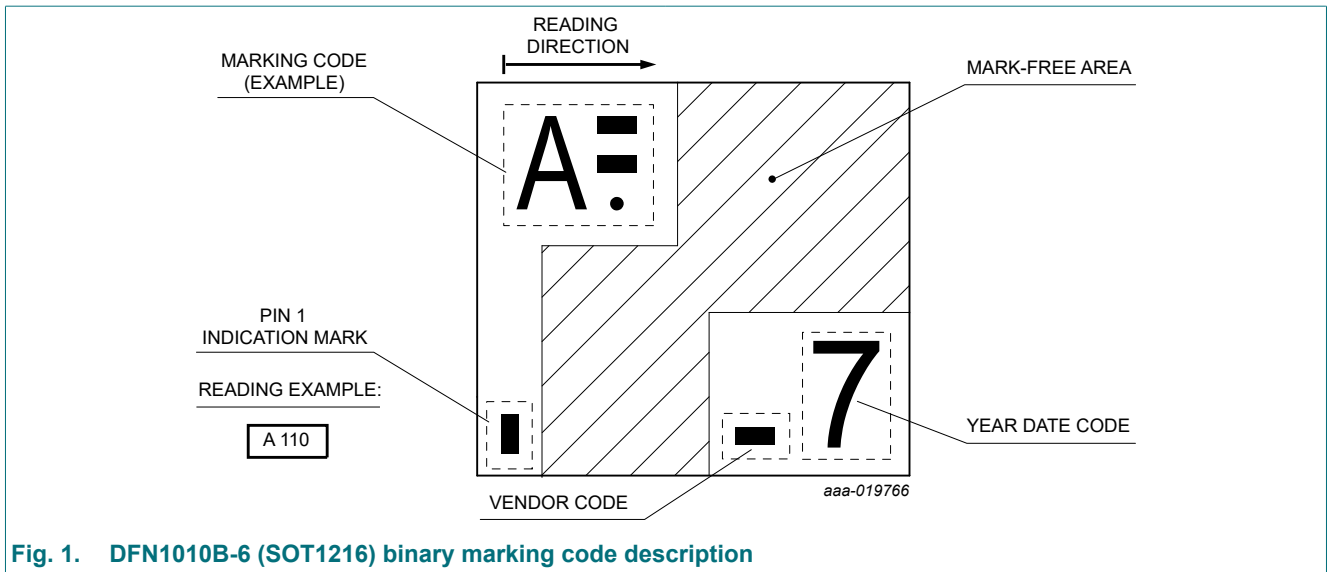
Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMCXB290UE	DFN1010B-6	plastic, leadless thermal enhanced ultra thin small outline package; 6 terminals; 0.35 mm pitch; 1.1 mm x 1 mm x 0.37 mm body	SOT1216

7. Marking

Table 4. Marking codes

Type number	Marking code
PMCXB290UE	C 111



8. Limiting values

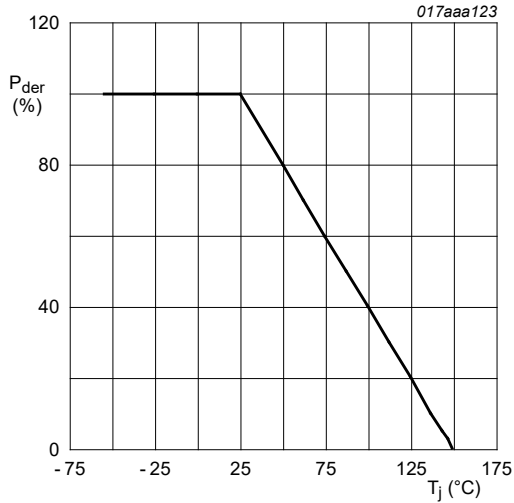
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
TR1 (N-channel)						
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$		-	20	V
V_{GS}	gate-source voltage			-8	8	V
I_D	drain current	$V_{GS} = 4.5\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	930	mA
		$V_{GS} = 4.5\text{ V}; T_{sp} = 25\text{ °C}$		-	3.5	A
		$V_{GS} = 4.5\text{ V}; T_{amb} = 100\text{ °C}$	[1]	-	590	mA
		$V_{GS} = 4.5\text{ V}; T_{sp} = 100\text{ °C}$		-	2.2	A
I_{DM}	peak drain current	$T_{amb} = 25\text{ °C}; \text{single pulse}; t_p \leq 10\text{ }\mu\text{s}$		-	14	A
P_{tot}	total power dissipation	$T_{amb} = 25\text{ °C}$	[2]	-	280	mW
			[1]	-	370	mW
		$T_{sp} = 25\text{ °C}$		-	6	W
TR1 (N-channel), Source-drain diode						
I_S	source current	$T_{amb} = 25\text{ °C}$	[1]	-	300	mA
TR2 (P-channel)						
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$		-	-20	V
V_{GS}	gate-source voltage			-8	8	V
I_D	drain current	$V_{GS} = -4.5\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	-570	mA
		$V_{GS} = -4.5\text{ V}; T_{sp} = 25\text{ °C}$		-	-2.3	A
		$V_{GS} = -4.5\text{ V}; T_{amb} = 100\text{ °C}$	[1]	-	-360	mA
		$V_{GS} = -4.5\text{ V}; T_{sp} = 100\text{ °C}$		-	-1.5	A
I_{DM}	peak drain current	$T_{amb} = 25\text{ °C}; \text{single pulse}; t_p \leq 10\text{ }\mu\text{s}$		-	-9.2	A
P_{tot}	total power dissipation	$T_{amb} = 25\text{ °C}$	[2]	-	280	mW
			[1]	-	370	mW
		$T_{sp} = 25\text{ °C}$		-	6	W
TR2 (P-channel), Source-drain diode						
I_S	source current	$T_{amb} = 25\text{ °C}$	[1]	-	-350	mA
Per device						
T_j	junction temperature			-55	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C

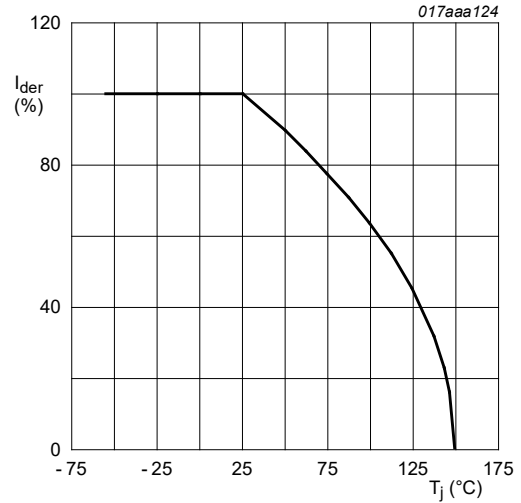
[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm^2 .

[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100 \%$$

Fig. 2. MOSFET transistor: Normalized total power dissipation as a function of junction temperature



$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100 \%$$

Fig. 3. MOSFET transistor: Normalized continuous drain current as a function of junction temperature

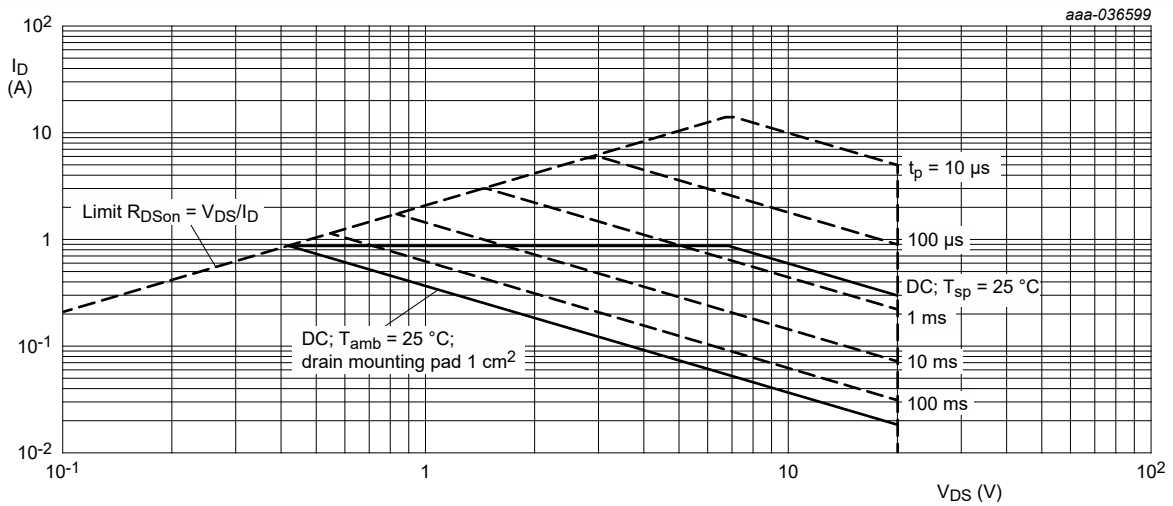
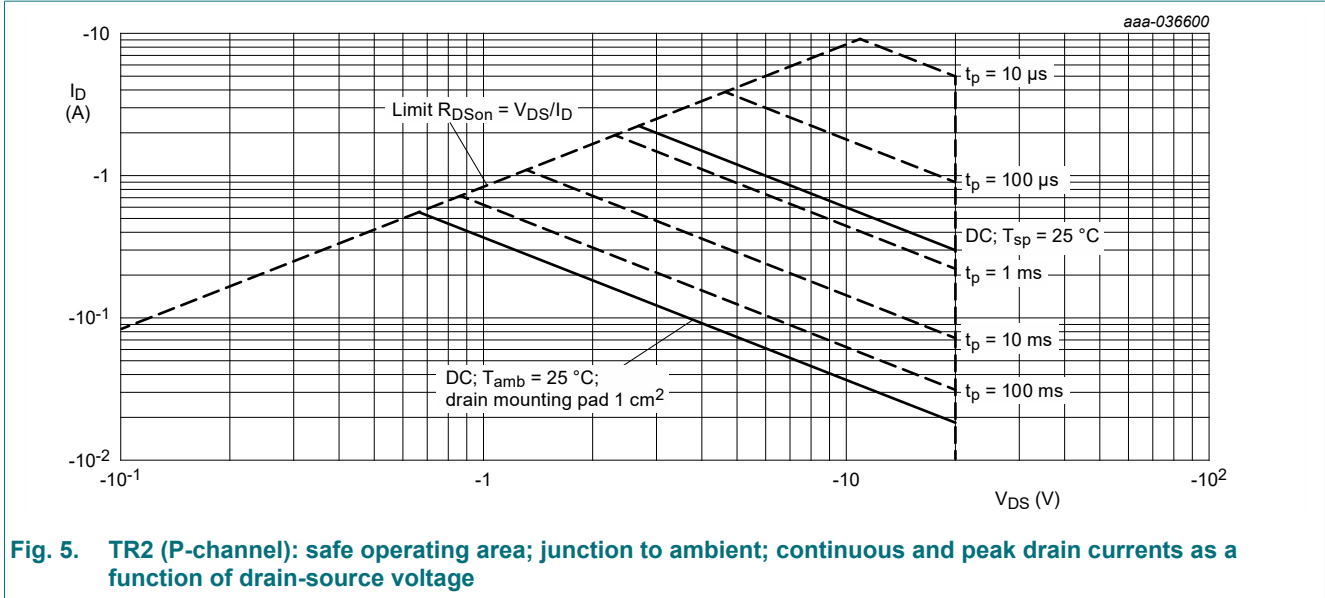


Fig. 4. TR1 (N-channel): safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage



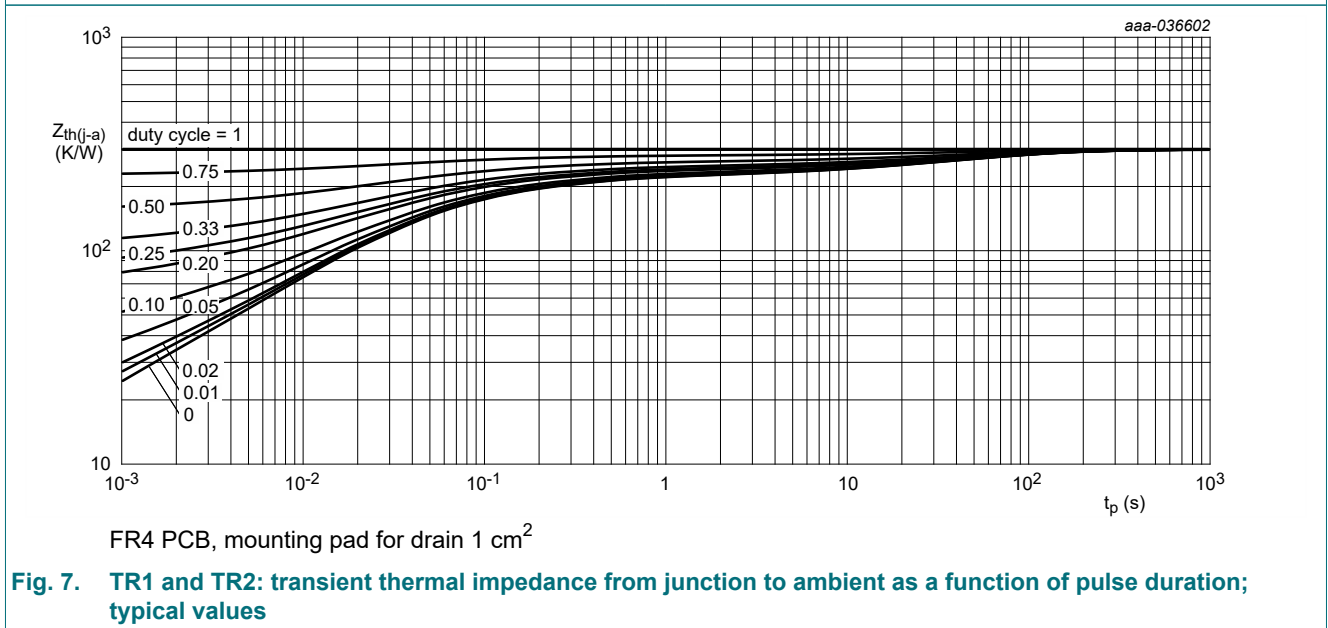
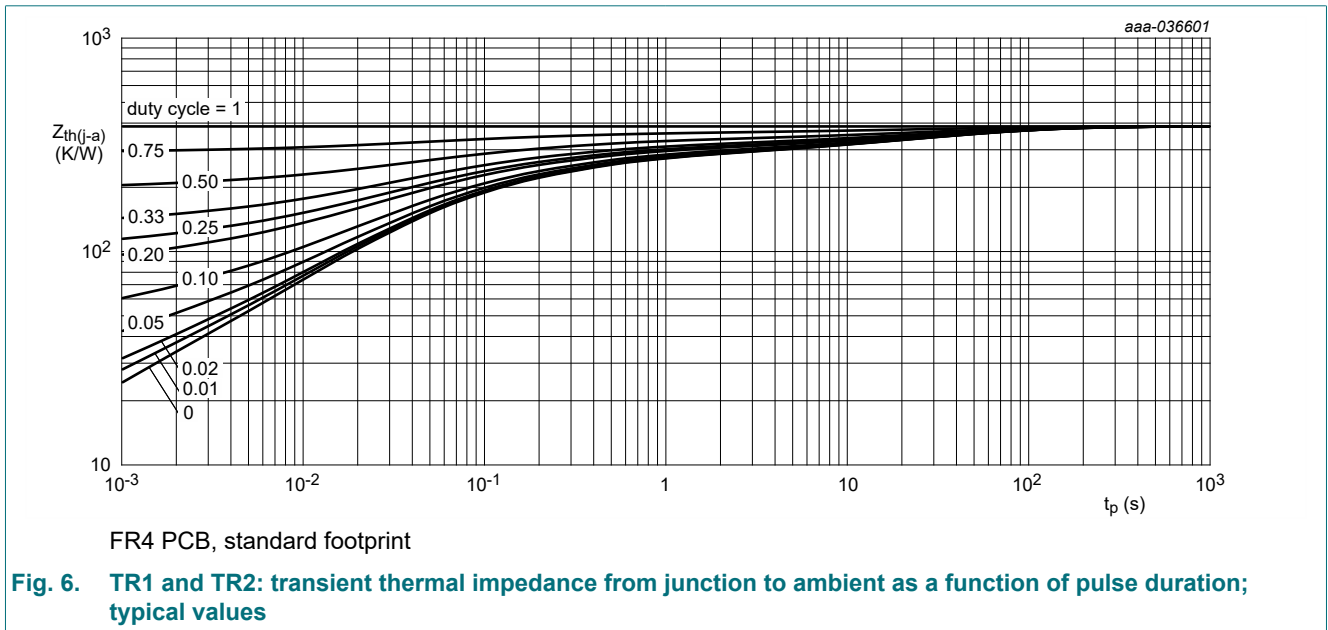
9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	386	444	K/W
			[2]	-	297	342	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	18	21	K/W

[1] Device mounted on an FR4 PCB, single-sided copper; tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm².



10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TR1 (N-channel), Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	20	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = 250 \mu\text{A}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C}$	0.45	0.7	1	V
I_{DSS}	drain leakage current	$V_{DS} = 20 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	1	μA
		$V_{DS} = 20 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ }^\circ\text{C}$	-	-	20	μA
I_{GSS}	gate leakage current	$V_{GS} = 8 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	10	μA
		$V_{GS} = -8 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	-10	μA
		$V_{GS} = 4.5 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	1	μA
		$V_{GS} = -4.5 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	-1	μA
		$V_{GS} = 2.5 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	500	nA
		$V_{GS} = -2.5 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	-500	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 1.2 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	270	320	m Ω
		$V_{GS} = 4.5 \text{ V}; I_D = 1.2 \text{ A}; T_j = 150 \text{ }^\circ\text{C}$	-	400	480	m Ω
		$V_{GS} = 2.5 \text{ V}; I_D = 1 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	360	480	m Ω
		$V_{GS} = 1.8 \text{ V}; I_D = 120 \text{ mA}; T_j = 25 \text{ }^\circ\text{C}$	-	470	680	m Ω
		$V_{GS} = 1.5 \text{ V}; I_D = 10 \text{ mA}; T_j = 25 \text{ }^\circ\text{C}$	-	600	1190	m Ω
g_{fs}	forward transconductance	$V_{DS} = 5 \text{ V}; I_D = 600 \text{ mA}; T_j = 25 \text{ }^\circ\text{C}$	-	1.9	-	S
TR1 (N-channel), Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$V_{DS} = 10 \text{ V}; I_D = 1.2 \text{ A}; V_{GS} = 4.5 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.6	0.9	nC
Q_{GS}	gate-source charge		-	0.1	-	nC
Q_{GD}	gate-drain charge		-	0.2	-	nC
C_{iss}	input capacitance	$V_{DS} = 10 \text{ V}; f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	43.6	-	pF
C_{oss}	output capacitance		-	10.1	-	pF
C_{rss}	reverse transfer capacitance		-	8.2	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 10 \text{ V}; I_D = 1.2 \text{ A}; V_{GS} = 4.5 \text{ V}; R_{G(ext)} = 6 \text{ } \Omega; T_j = 25 \text{ }^\circ\text{C}$	-	1	-	ns
t_r	rise time		-	3	-	ns
$t_{d(off)}$	turn-off delay time		-	5	-	ns
t_f	fall time		-	3	-	ns
TR1 (N-channel), Source-drain diode characteristics						
V_{SD}	source-drain voltage	$I_S = 340 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.9	1.2	V

Table 8. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TR2 (P-channel), Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-20	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = -250 \mu A; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$	-0.45	-0.7	-1	V
I_{DSS}	drain leakage current	$V_{DS} = -20 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	-1	μA
		$V_{DS} = -20 V; V_{GS} = 0 V; T_j = 150 \text{ }^\circ C$	-	-	-20	μA
I_{GSS}	gate leakage current	$V_{GS} = 8 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	10	μA
		$V_{GS} = -8 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	-10	μA
		$V_{GS} = 4.5 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	1	μA
		$V_{GS} = -4.5 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	-1	μA
		$V_{GS} = 2.5 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	500	nA
		$V_{GS} = -2.5 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	-500	nA
		R_{DSon}	drain-source on-state resistance	$V_{GS} = -4.5 V; I_D = -1.2 A; T_j = 25 \text{ }^\circ C$	-	590
	$V_{GS} = -4.5 V; I_D = -1.2 mA; T_j = 150 \text{ }^\circ C$	-		890	1200	m Ω
	$V_{GS} = -2.5 V; I_D = -1 A; T_j = 25 \text{ }^\circ C$	-		980	1400	m Ω
	$V_{GS} = -1.8 V; I_D = -120 mA; T_j = 25 \text{ }^\circ C$	-		1170	1970	m Ω
g_{fs}	forward transconductance	$V_{DS} = -5 V; I_D = -600 mA; T_j = 25 \text{ }^\circ C$	-	1.2	-	S
TR2 (P-channel), Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$V_{DS} = -10 V; I_D = -600 mA; V_{GS} = -4.5 V; T_j = 25 \text{ }^\circ C$	-	0.6	0.8	nC
Q_{GS}	gate-source charge		-	0.1	-	nC
Q_{GD}	gate-drain charge		-	0.1	-	nC
C_{iss}	input capacitance	$V_{DS} = -10 V; f = 1 MHz; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	53.5	-	pF
C_{oss}	output capacitance		-	9.6	-	pF
C_{rss}	reverse transfer capacitance		-	7.8	-	pF
$t_{d(on)}$	turn-on delay time		$V_{DS} = -10 V; I_D = -1.2 A; V_{GS} = -4.5 V; R_{G(ext)} = 6 \Omega; T_j = 25 \text{ }^\circ C$	-	1	-
t_r	rise time	-		3	-	ns
$t_{d(off)}$	turn-off delay time	-		6	-	ns
t_f	fall time	-		3.7	-	ns
TR2 (P-channel), Source-drain diode characteristics						
V_{SD}	source-drain voltage	$I_S = -340 mA; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-0.9	-1.2	V

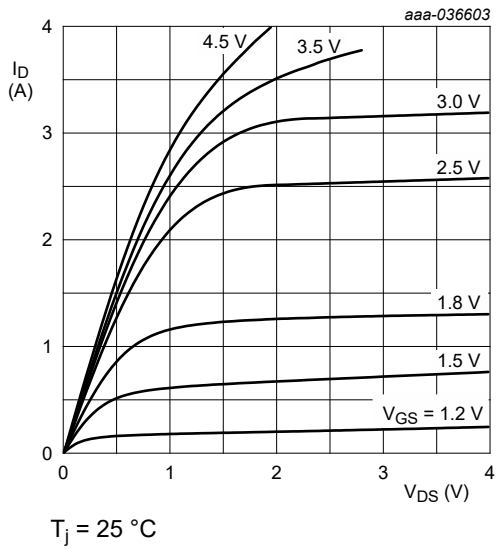


Fig. 8. TR1: output characteristics; drain current as a function of drain-source voltage; typical values

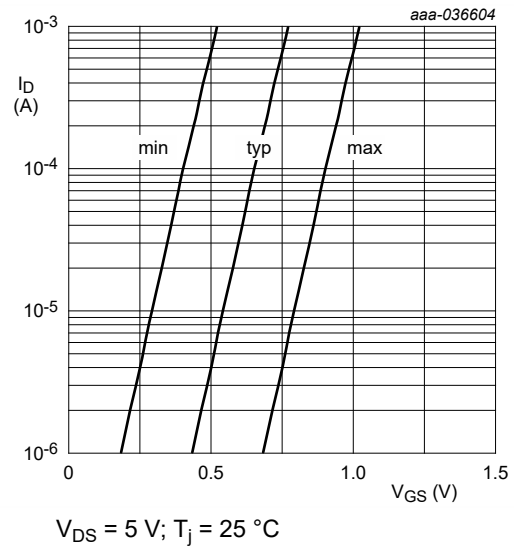


Fig. 9. TR1: sub-threshold drain current as a function of gate-source voltage

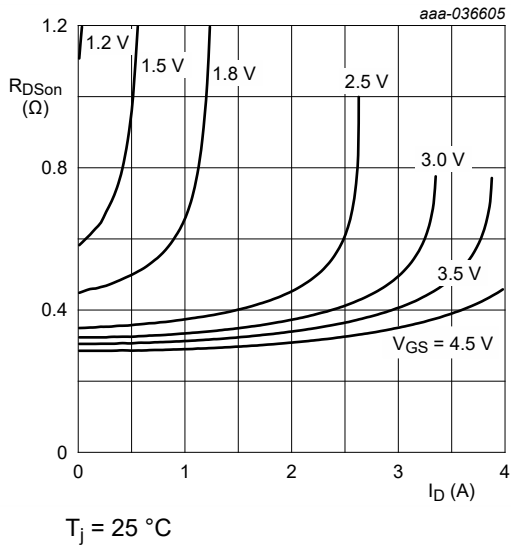


Fig. 10. TR1: drain-source on-state resistance as a function of drain current; typical values

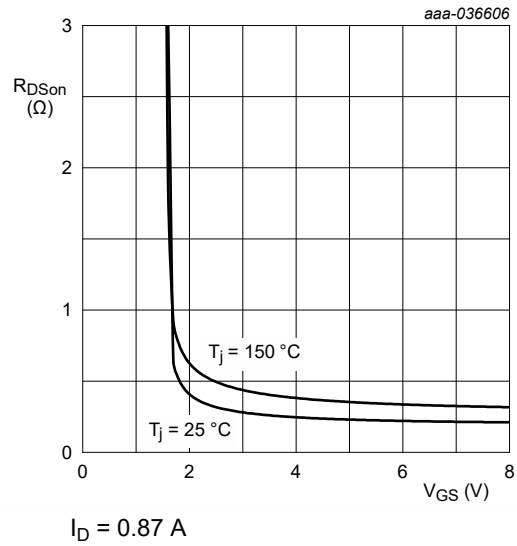
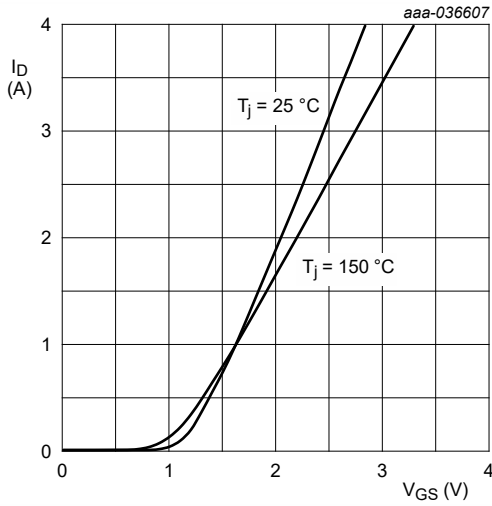
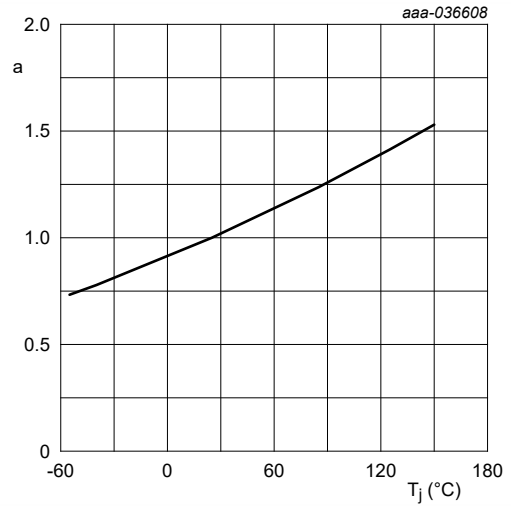


Fig. 11. TR1: drain-source on-state resistance as a function of gate-source voltage; typical values



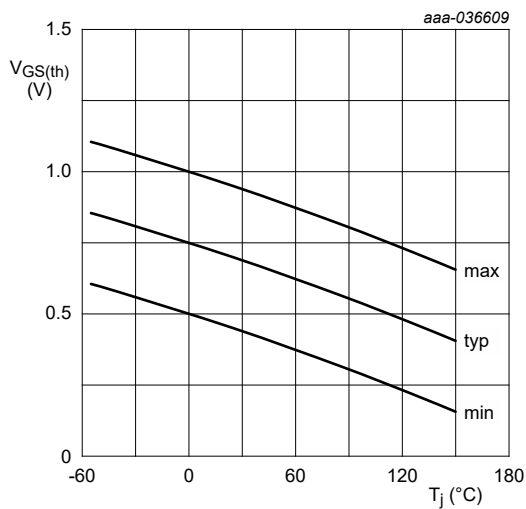
$$V_{DS} = I_D \times R_{DSon}$$

Fig. 12. TR1: transfer characteristics; drain current as a function of gate-source voltage; typical values



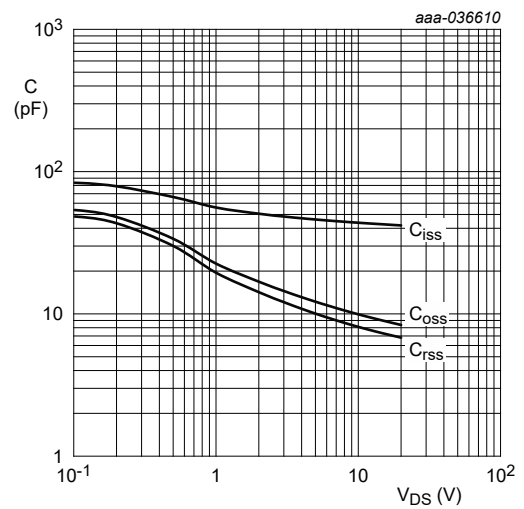
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ C)}}$$

Fig. 13. TR1: normalized drain-source on-state resistance as a function of junction temperature; typical values



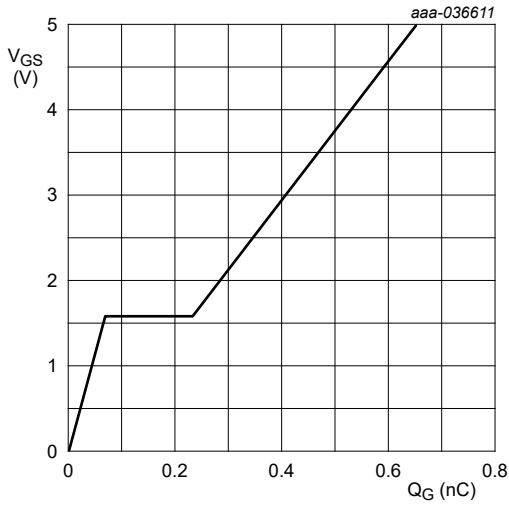
$$I_D = 250 \mu A; V_{DS} = V_{GS}$$

Fig. 14. TR1: gate-source threshold voltage as a function of junction temperature



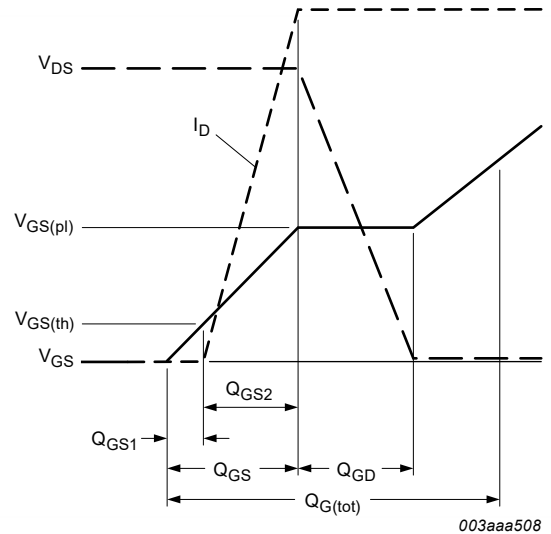
$$f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}$$

Fig. 15. TR1: input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



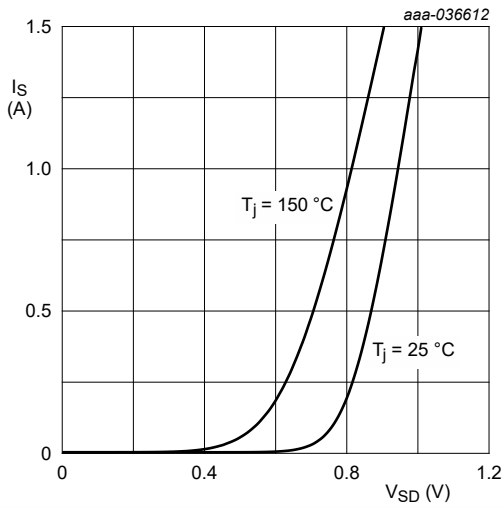
$I_D = 1.2 \text{ A}; V_{DS} = 10 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}$

Fig. 16. TR1: gate-source voltage as a function of gate charge; typical values



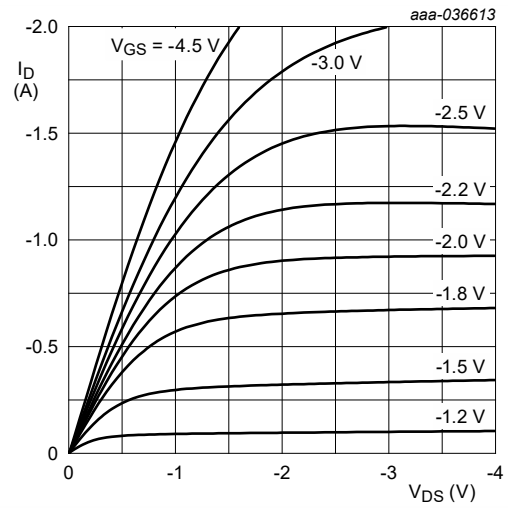
003aaa508

Fig. 17. Gate charge waveform definitions



$V_{GS} = 0 \text{ V}$

Fig. 18. TR1: source current as a function of source-drain voltage; typical values



$T_j = 25 \text{ }^\circ\text{C}$

Fig. 19. TR2: output characteristics; drain current as a function of drain-source voltage; typical values

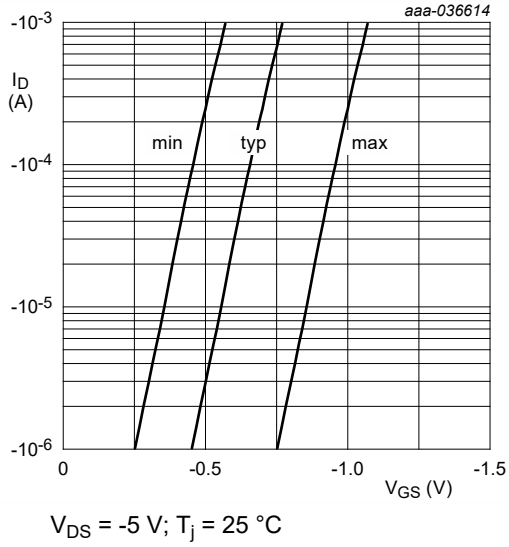


Fig. 20. TR2: sub-threshold drain current as a function of gate-source voltage

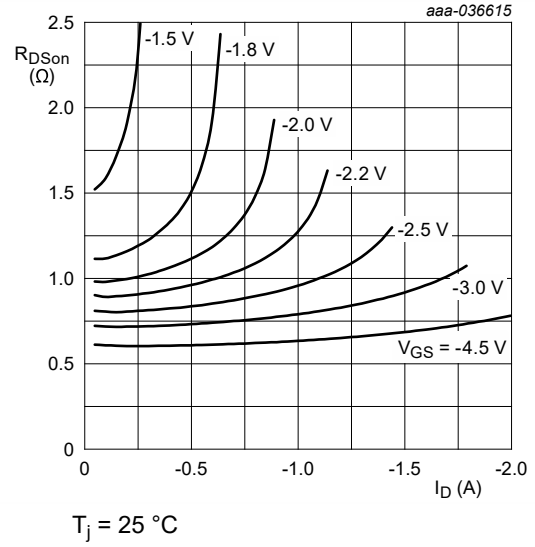


Fig. 21. TR2: drain-source on-state resistance as a function of drain current; typical values

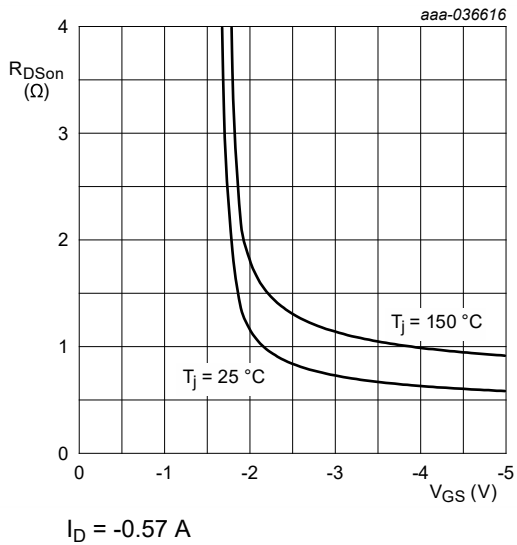


Fig. 22. TR2: drain-source on-state resistance as a function of gate-source voltage; typical values

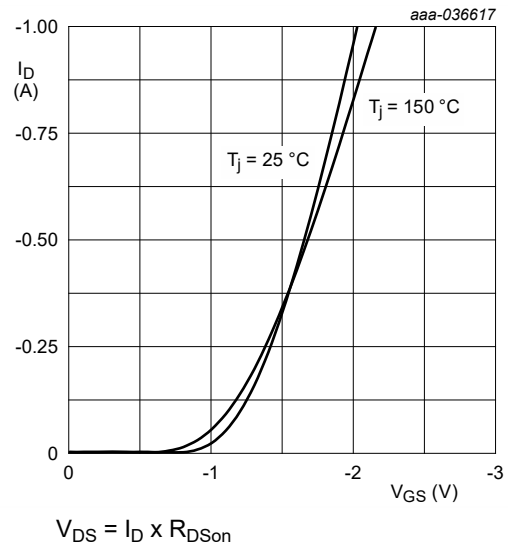
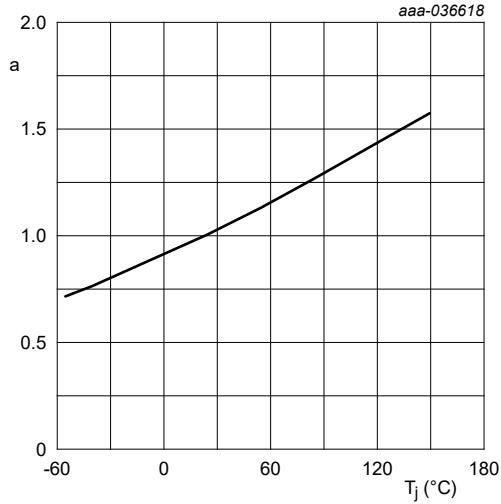
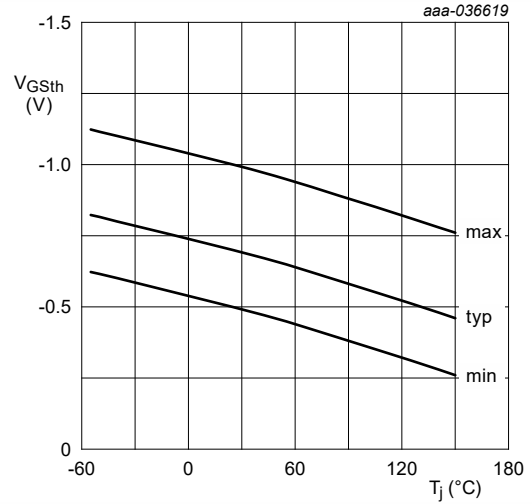


Fig. 23. TR2: transfer characteristics; drain current as a function of gate-source voltage; typical values



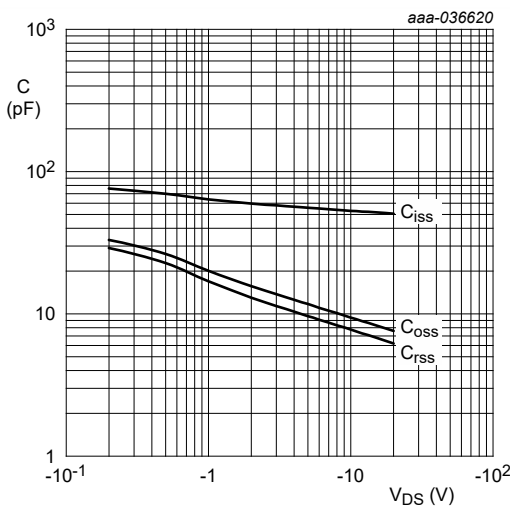
$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

Fig. 24. TR2: normalized drain-source on-state resistance as a function of junction temperature; typical values



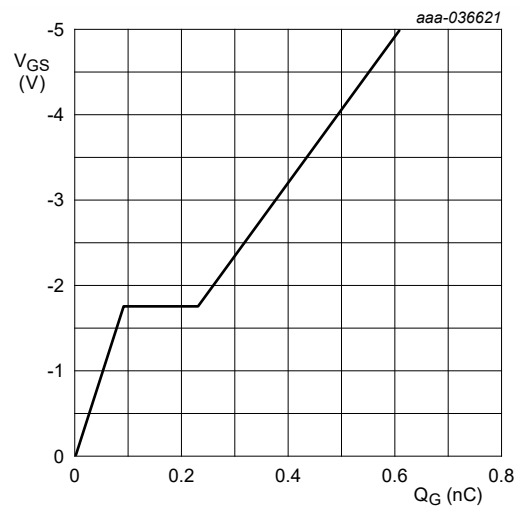
$I_D = -250 \mu A; V_{DS} = V_{GS}$

Fig. 25. TR2: gate-source threshold voltage as a function of junction temperature



$f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}$

Fig. 26. TR2: input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{DS} = -10 \text{ V}; I_D = -0.6 \text{ A}; T_j = 25^{\circ} \text{ C}$

Fig. 27. TR2: gate-source voltage as a function of gate charge; typical values

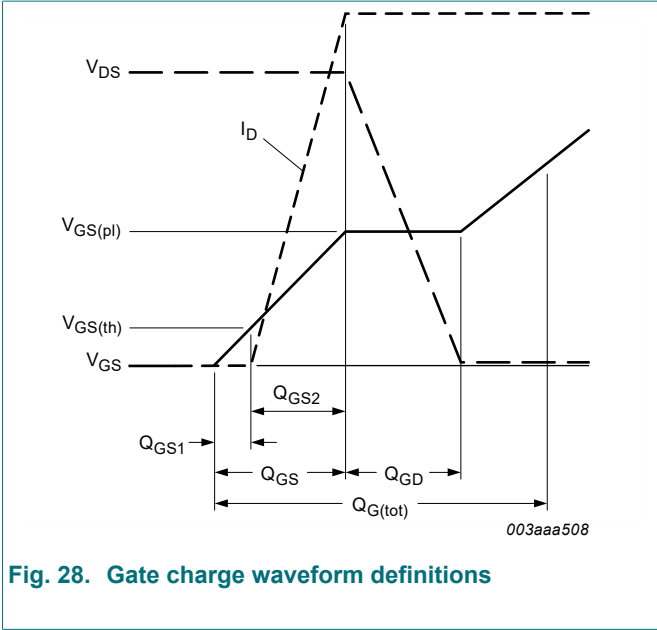


Fig. 28. Gate charge waveform definitions

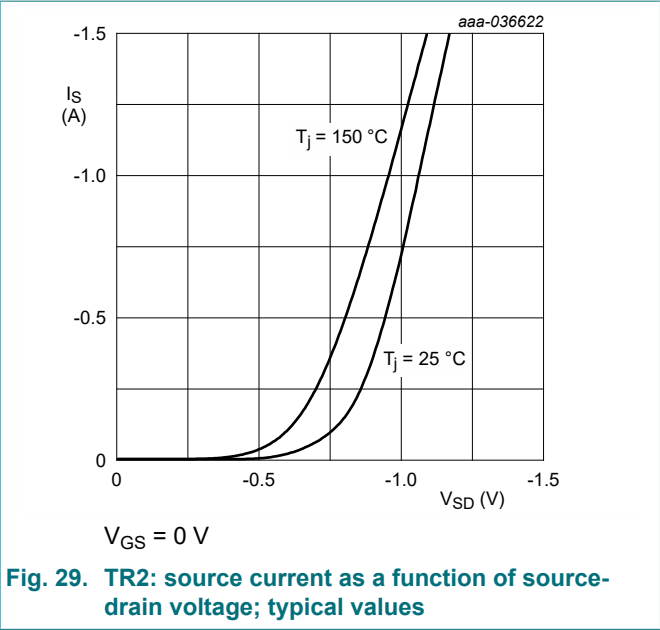


Fig. 29. TR2: source current as a function of source-drain voltage; typical values

11. Test information

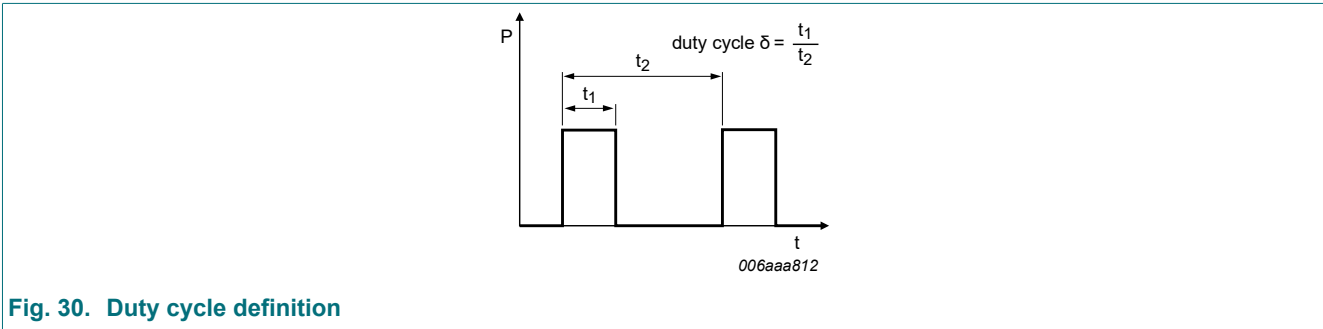


Fig. 30. Duty cycle definition

12. Package outline

DFN1010B-6: plastic thermal enhanced ultra thin small outline package; no leads;
6 terminals; body: 1.1 x 1.0 x 0.37 mm

SOT1216

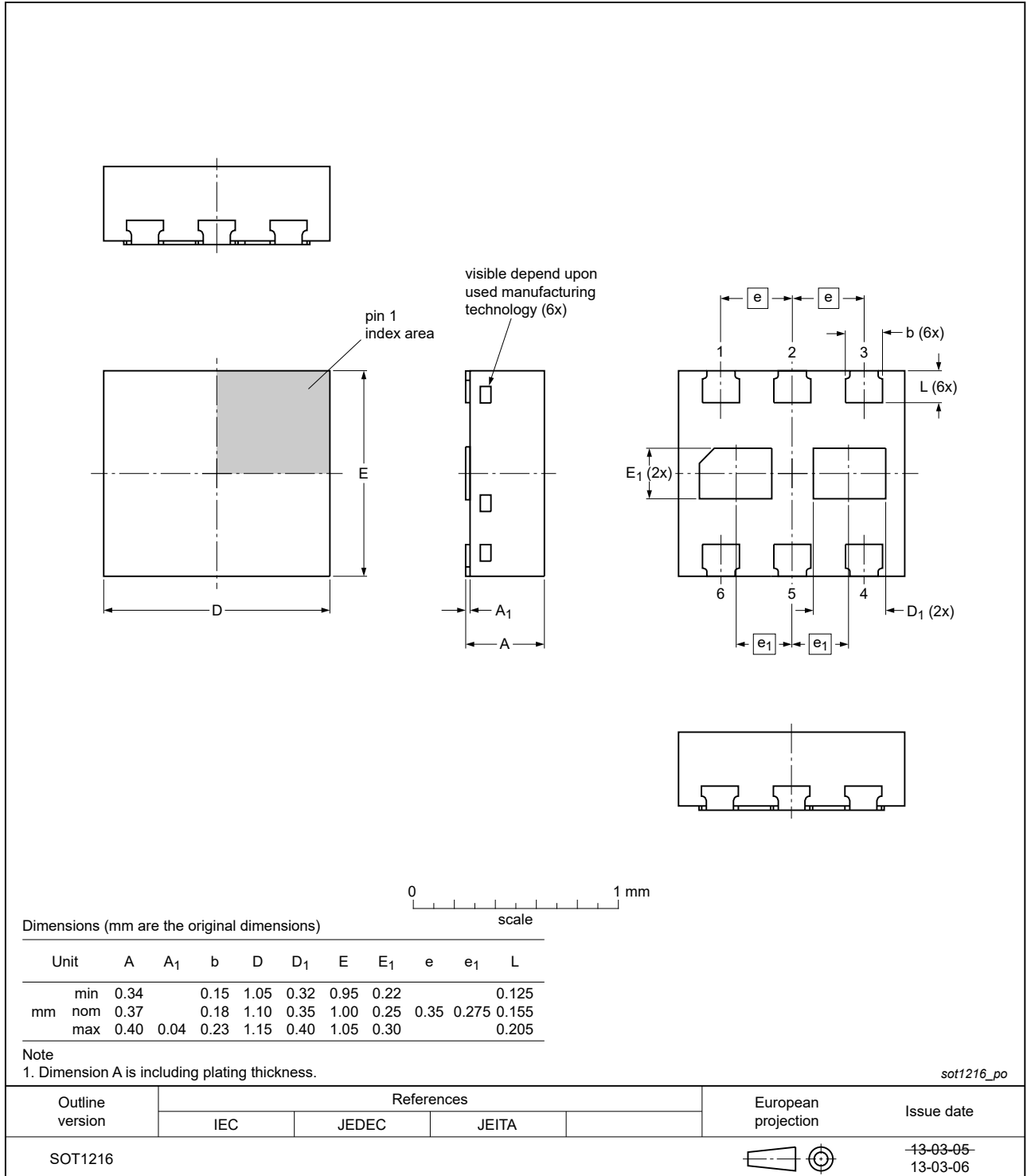


Fig. 31. Package outline DFN1010B-6 (SOT1216)

13. Soldering

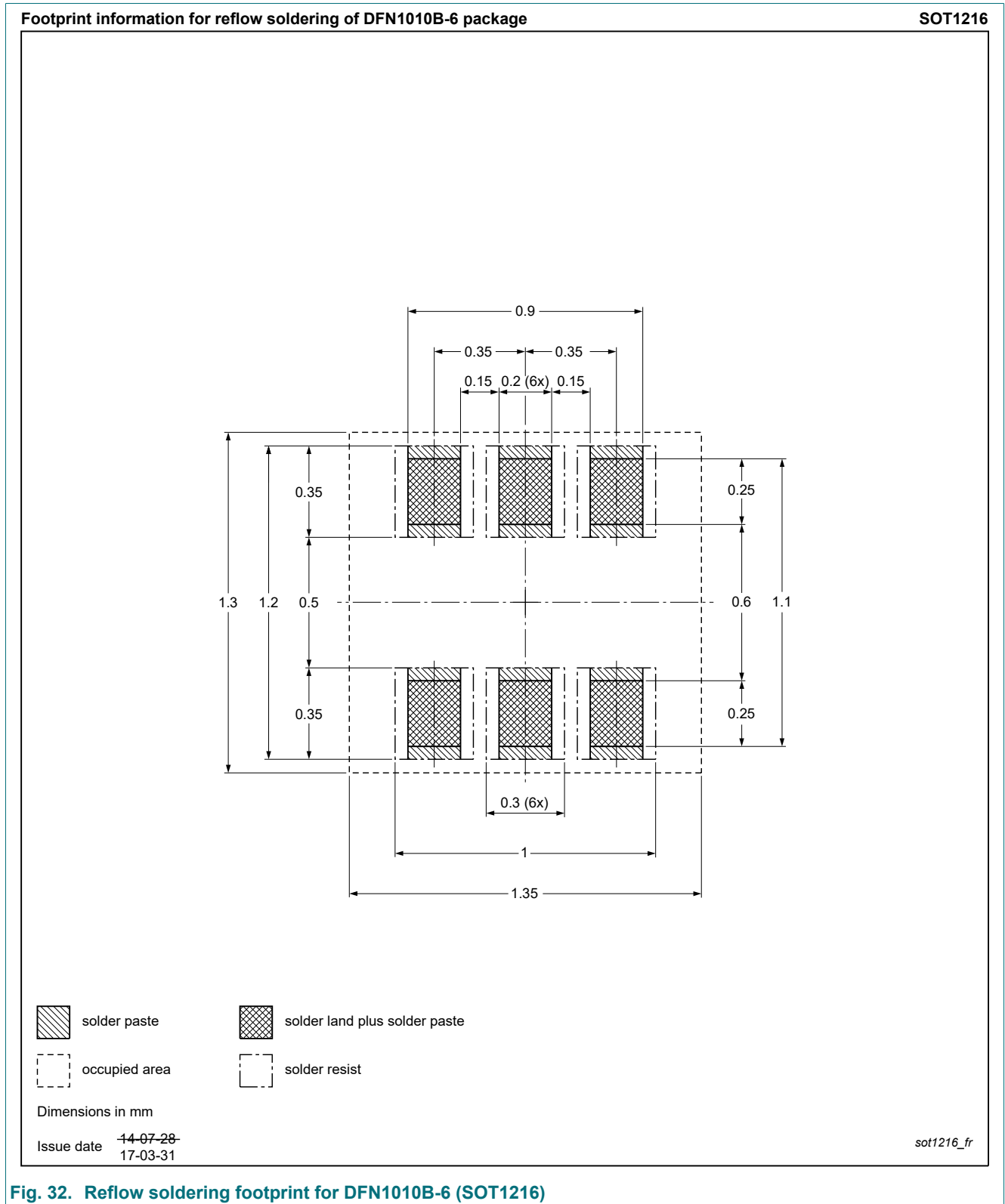


Fig. 32. Reflow soldering footprint for DFN1010B-6 (SOT1216)

14. Revision history

Table 9. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMCXB290UE v.1	20230530	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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