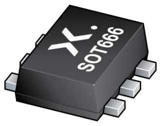


PMDT290UCE

20 / 20 V, 800 / 550 mA N/P-channel Trench MOSFET

Rev. 1 — 6 October 2011 Product data sheet

1. Product profile

1.1 General description

Complementary N/P-channel enhancement mode Field-Effect Transistor (FET) in an ultra small and flat lead SOT666 Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

1.2 Features and benefits

- Very fast switching
- Trench MOSFET technology
- ESD protection up to 2 kV
- AEC-Q101 qualified

1.3 Applications

- Relay driver
- High-speed line driver
- Low-side loadswitch
- Switching circuits

1.4 Quick reference data

Table 1. Quick reference data

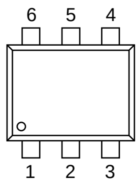
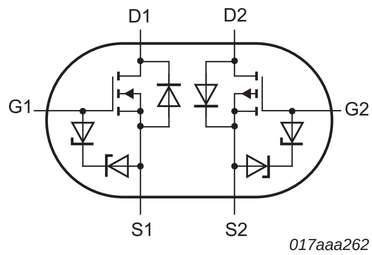
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
TR1 (N-channel), Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 500 mA; T_j = 25 °C		-	290	380	mΩ
TR2 (P-channel), Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = -4.5 V; I_D = -400 mA; T_j = 25 °C		-	0.67	0.85	Ω
TR1 (N-channel)							
V_{DS}	drain-source voltage	T_j = 25 °C		-	-	20	V
V_{GS}	gate-source voltage			-8	-	8	V
I_D	drain current	V_{GS} = 4.5 V; T_{amb} = 25 °C	[1]	-	-	800	mA
TR2 (P-channel)							
V_{DS}	drain-source voltage	T_j = 25 °C		-	-	-20	V
V_{GS}	gate-source voltage			-8	-	8	V
I_D	drain current	V_{GS} = -4.5 V; T_{amb} = 25 °C	[1]	-	-	-550	mA

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm^2.

nexperia

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source TR1		
2	G1	gate TR1		
3	D2	drain TR2		
4	S2	source TR2		
5	G2	gate TR2		
6	D1	drain TR1	SOT666	

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMDT290UCE	-	plastic surface-mounted package; 6 leads	SOT666

4. Marking

Table 4. Marking codes

Type number	Marking code
PMDT290UCE	AF

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
TR1 (N-channel)						
V_{DS}	drain-source voltage	T_j = 25 °C		-	20	V
V_{GS}	gate-source voltage			-8	8	V
I_D	drain current	V_{GS} = 4.5 V; T_{amb} = 25 °C	[1]	-	800	mA
		V_{GS} = 4.5 V; T_{amb} = 100 °C	[1]	-	500	mA
I_{DM}	peak drain current	T_{amb} = 25 °C; single pulse; $t_p \leq 10$ µs		-	3.2	A
P_{tot}	total power dissipation	T_{amb} = 25 °C	[2]	-	330	mW
			[1]	-	390	mW
		T_{sp} = 25 °C		-	1090	mW
TR1 (N-channel), Source-drain diode						
I_S	source current	T_{amb} = 25 °C	[1]	-	370	mA
TR1 N-channel), ESD maximum rating						
V_{ESD}	electrostatic discharge voltage	HBM	[3]	-	2000	V

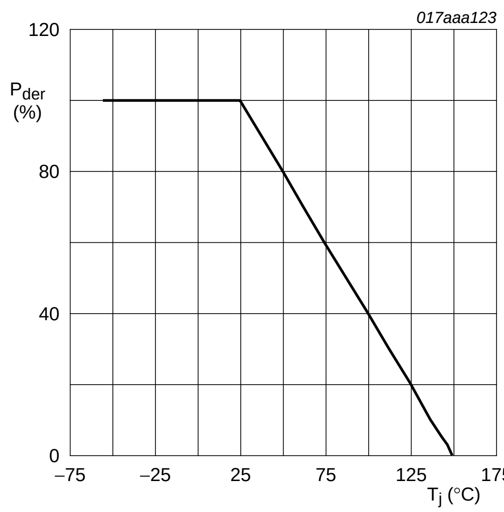
Table 5. Limiting values *...continued*
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
TR2 (P-channel)						
V_{DS}	drain-source voltage	T_j = 25 °C		-	-20	V
V_{GS}	gate-source voltage			-8	8	V
I_D	drain current	V_{GS} = -4.5 V; T_{amb} = 25 °C	[1]	-	-550	mA
		V_{GS} = -4.5 V; T_{amb} = 100 °C	[1]	-	-350	mA
I_{DM}	peak drain current	T_{amb} = 25 °C; single pulse; t_p ≤ 10 µs		-	-2.2	A
P_{tot}	total power dissipation	T_{amb} = 25 °C	[2]	-	330	mW
			[1]	-	390	mW
		T_{sp} = 25 °C		-	1090	mW
TR2 (P-channel), Source-drain diode						
I_S	source current	T_{amb} = 25 °C	[1]	-	-370	mA
TR2 (P-channel), ESD maximum rating						
V_{ESD}	electrostatic discharge voltage	HBM	[3]	-	2000	V
Per device						
P_{tot}	total power dissipation	T_{amb} = 25 °C	[2]	-	500	mW
T_j	junction temperature			-55	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm^2.

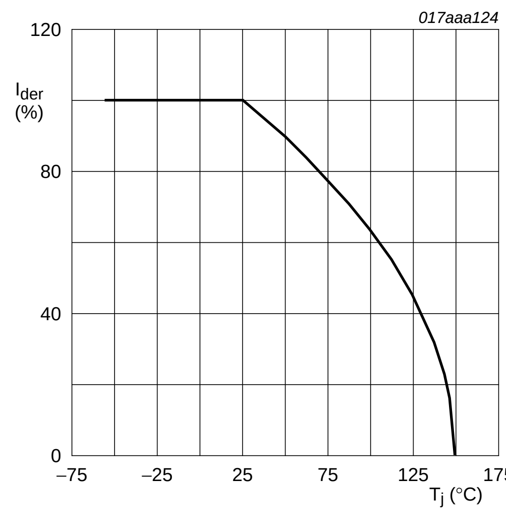
[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper; tin-plated and standard footprint.

[3] Measured between all pins.



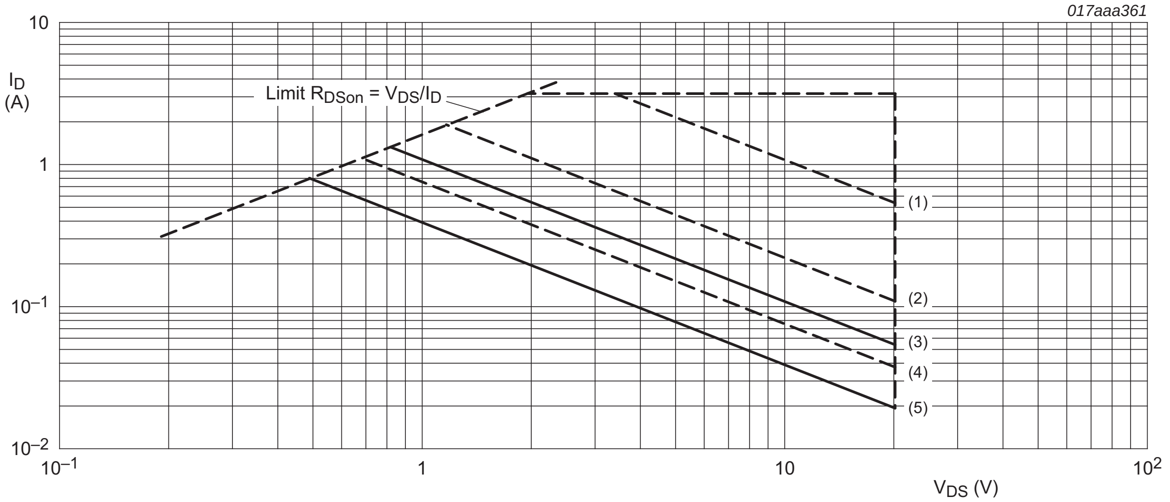
$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\ \%$$

Fig 1. Normalized total power dissipation as a function of junction temperature



$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\ \%$$

Fig 2. Normalized continuous drain current as a function of junction temperature



I_{DM} = single pulse

(1) t_p = 1 ms

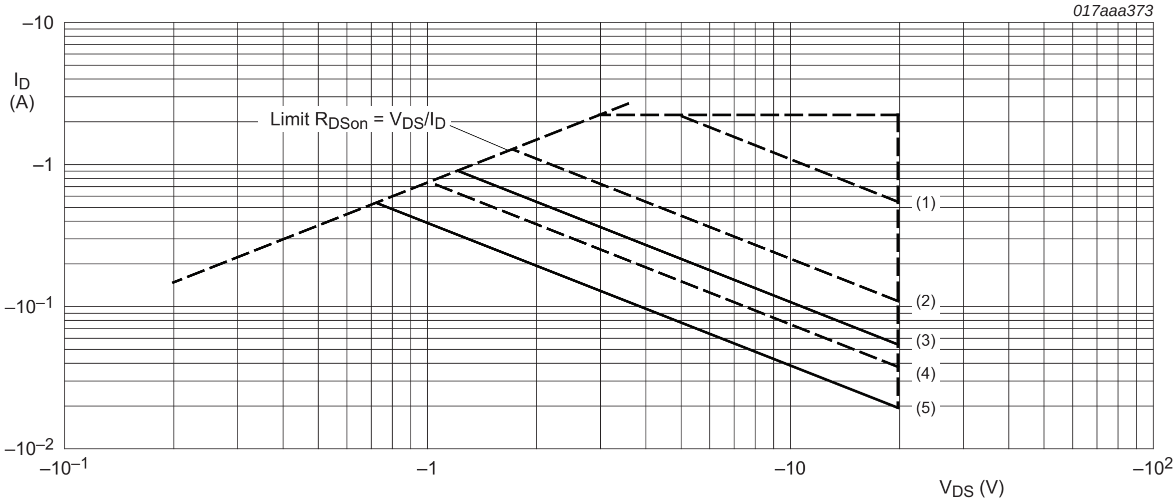
(2) t_p = 10 ms

(3) DC; T_{sp} = 25 °C

(4) t_p = 100 ms

(5) DC; T_{amb} = 25 °C; drain mounting pad 1 cm^2

Fig 3. Safe operating area TR1 (N-channel); junction to ambient; continuous and peak drain currents as a function of drain-source voltage



I_{DM} = single pulse

(1) t_p = 1 ms

(2) t_p = 10 ms

(3) DC; T_{sp} = 25 °C

(4) t_p = 100 ms

(5) DC; T_{amb} = 25 °C; drain mounting pad 1 cm^2

Fig 4. Safe operating area TR2 (P-channel); junction to ambient; continuous and peak drain currents as a function of drain-source voltage

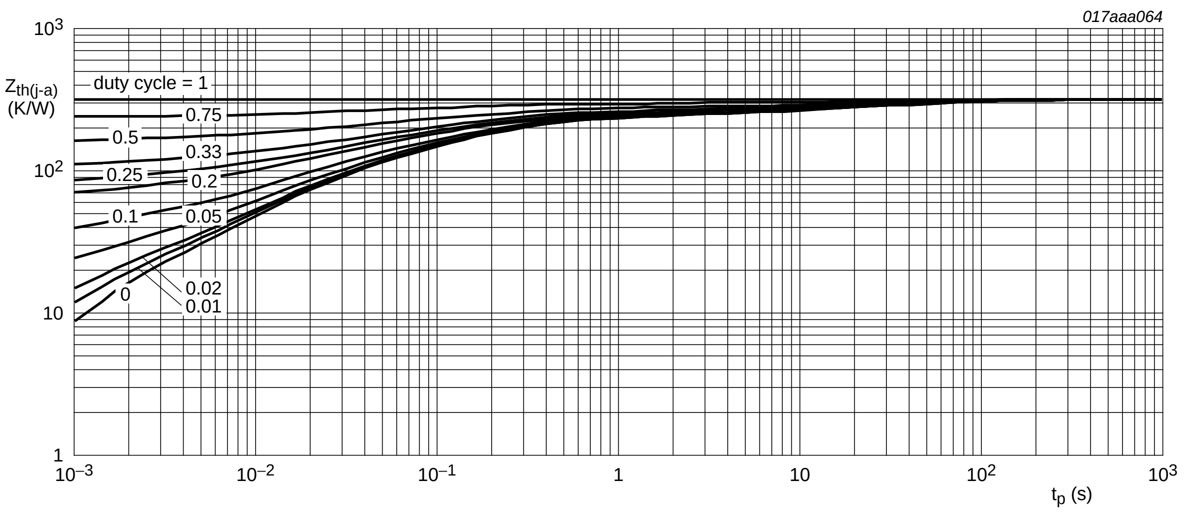
6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
TR1 (N-channel)							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	330	380	K/W
			[2]	-	280	320	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	-	115	K/W
TR2 (P-channel)							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	330	380	K/W
			[2]	-	280	320	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	-	115	K/W
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	250	K/W

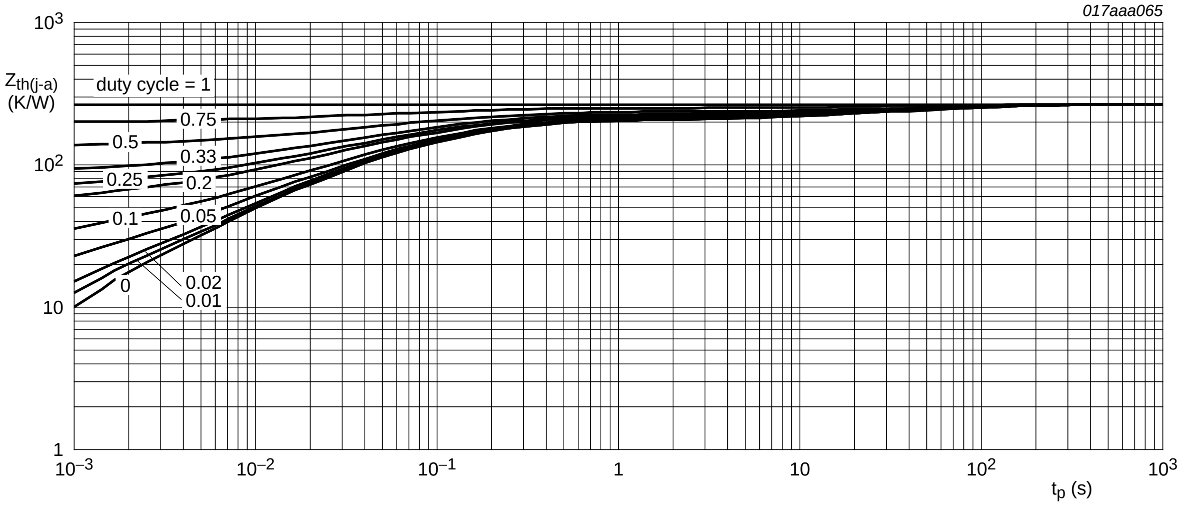
[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper; tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm^2.



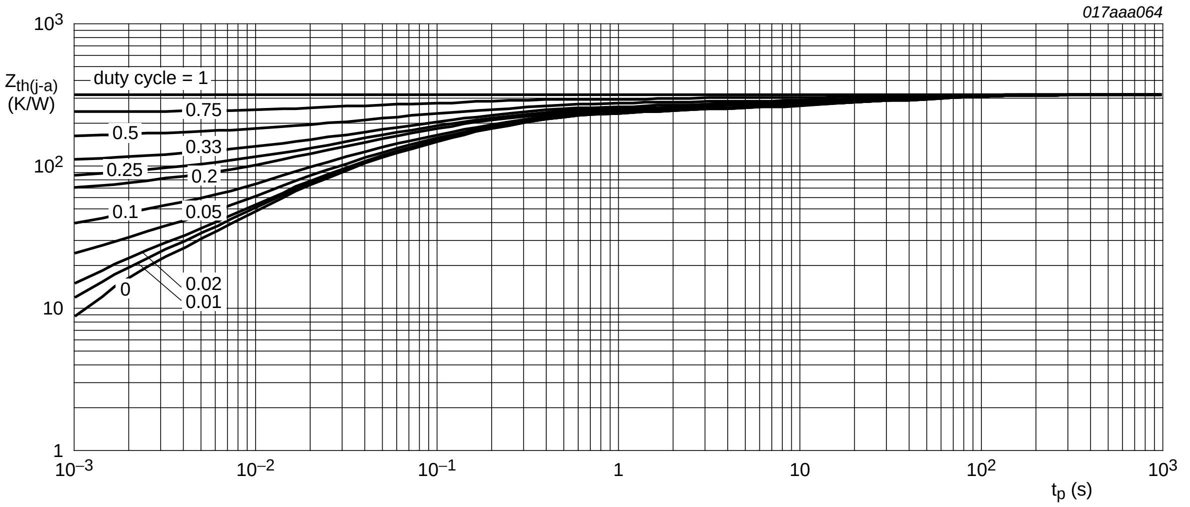
FR4 PCB, standard footprint

Fig 5. TR1: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



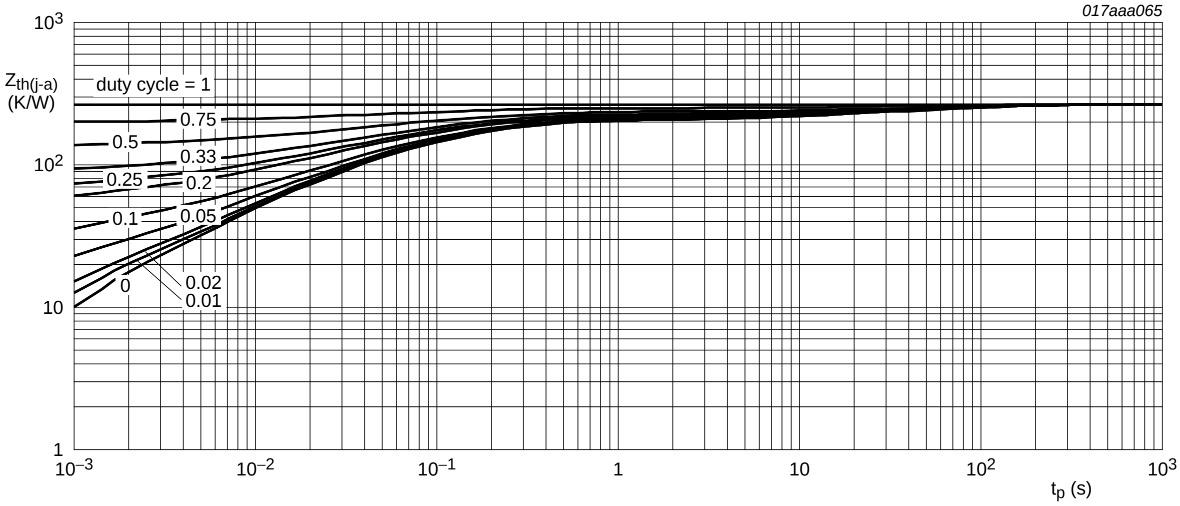
FR4 PCB, mounting pad for drain 1 cm^2

Fig 6. TR1: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, standard footprint

Fig 7. TR2: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, mounting pad for drain 1 cm^2

Fig 8. TR2: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

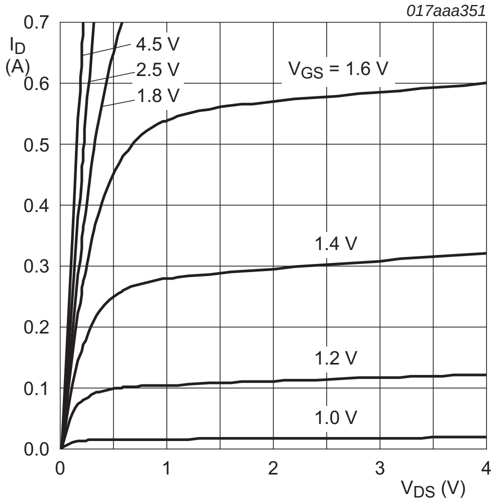
7. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TR1 (N-channel), Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C	20	-	-	V
V_{GSth}	gate-source threshold voltage	I_D = 250 µA; V_{DS} = V_{GS}; T_j = 25 °C	0.5	0.75	0.95	V
I_{DSS}	drain leakage current	V_{DS} = 20 V; V_{GS} = 0 V; T_j = 25 °C	-	-	1	µA
		V_{DS} = 20 V; V_{GS} = 0 V; T_j = 150 °C	-	-	10	µA
I_{GSS}	gate leakage current	V_{GS} = 8 V; V_{DS} = 0 V; T_j = 25 °C	-	-	2	µA
		V_{GS} = -8 V; V_{DS} = 0 V; T_j = 25 °C	-	-	2	µA
		V_{GS} = 4.5 V; V_{DS} = 0 V; T_j = 25 °C	-	-	500	nA
		V_{GS} = -4.5 V; V_{DS} = 0 V; T_j = 25 °C	-	-	500	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 500 mA; T_j = 25 °C	-	290	380	mΩ
		V_{GS} = 4.5 V; I_D = 500 mA; T_j = 150 °C	-	460	610	mΩ
		V_{GS} = 2.5 V; I_D = 200 mA; T_j = 25 °C	-	420	620	mΩ
		V_{GS} = 1.8 V; I_D = 10 mA; T_j = 25 °C	-	0.6	1.1	Ω
g_{fs}	transfer conductance	V_{DS} = 10 V; I_D = 200 mA; T_j = 25 °C	-	1.6	-	S
TR1 (N-channel), Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	V_{DS} = 10 V; I_D = 500 mA; V_{GS} = 4.5 V; T_j = 25 °C	-	0.45	0.68	nC
Q_{GS}	gate-source charge		-	0.15	-	nC
Q_{GD}	gate-drain charge		-	0.15	-	nC

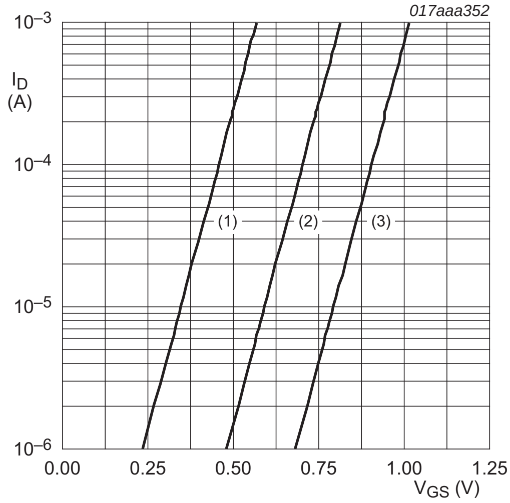
Table 7. Characteristics *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{iss}	input capacitance	V_{DS} = 10 V; f = 1 MHz; V_{GS} = 0 V; T_j = 25 °C	-	55	83	pF
C_{oss}	output capacitance		-	15	-	pF
C_{rss}	reverse transfer capacitance		-	7	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 10 V; R_L = 250 Ω; V_{GS} = 4.5 V; $R_{G(ext)}$ = 6 Ω; T_j = 25 °C	-	6	12	ns
t_r	rise time		-	4	-	ns
$t_{d(off)}$	turn-off delay time		-	86	172	ns
t_f	fall time		-	31	-	ns
TR1 (N-channel), Source-drain diode characteristics						
V_{SD}	source-drain voltage	I_S = 300 mA; V_{GS} = 0 V; T_j = 25 °C	0.48	0.77	1.2	V
TR2 (P-channel), Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = -250 µA; V_{GS} = 0 V; T_j = 25 °C	-20	-	-	V
V_{GSth}	gate-source threshold voltage	I_D = -250 µA; V_{DS} = V_{GS}; T_j = 25 °C	-0.5	-0.8	-1.3	V
I_{DSS}	drain leakage current	V_{DS} = -20 V; V_{GS} = 0 V; T_j = 25 °C	-	-	-1	µA
		V_{DS} = -20 V; V_{GS} = 0 V; T_j = 150 °C	-	-	-10	µA
I_{GSS}	gate leakage current	V_{GS} = 8 V; V_{DS} = 0 V; T_j = 25 °C	-	-	-2	µA
		V_{GS} = -8 V; V_{DS} = 0 V; T_j = 25 °C	-	-	-2	µA
		V_{GS} = 4.5 V; V_{DS} = 0 V; T_j = 25 °C	-	-	-0.5	µA
		V_{GS} = -4.5 V; V_{DS} = 0 V; T_j = 25 °C	-	-	-0.5	µA
R_{DSon}	drain-source on-state resistance	V_{GS} = -4.5 V; I_D = -400 mA; T_j = 25 °C	-	0.67	0.85	Ω
		V_{GS} = -4.5 V; I_D = -400 mA; T_j = 150 °C	-	1.1	1.4	Ω
		V_{GS} = -2.5 V; I_D = -200 mA; T_j = 25 °C	-	1.2	1.5	Ω
		V_{GS} = -1.8 V; I_D = -10 mA; T_j = 25 °C	-	1.8	2.8	Ω
g_{fs}	transfer conductance	V_{DS} = -10 V; I_D = -200 mA; T_j = 25 °C	-	610	-	mS
TR2 (P-channel), Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	V_{DS} = -10 V; I_D = -400 mA; V_{GS} = -4.5 V; T_j = 25 °C	-	0.76	1.14	nC
Q_{GS}	gate-source charge		-	0.28	-	nC
Q_{GD}	gate-drain charge		-	0.18	-	nC
C_{iss}	input capacitance	V_{DS} = -10 V; f = 1 MHz; V_{GS} = 0 V; T_j = 25 °C	-	58	87	pF
C_{oss}	output capacitance		-	21	-	pF
C_{rss}	reverse transfer capacitance		-	12	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = -10 V; R_L = 250 Ω; V_{GS} = -4.5 V; $R_{G(ext)}$ = 6 Ω; T_j = 25 °C	-	18	36	ns
t_r	rise time		-	30	-	ns
$t_{d(off)}$	turn-off delay time		-	80	160	ns
t_f	fall time		-	72	-	ns
TR2 (P-channel), Source-drain diode characteristics						
V_{SD}	source-drain voltage	I_S = -300 mA; V_{GS} = 0 V; T_j = 25 °C	-0.48	-0.84	-1.2	V



T_j = 25 °C

Fig 9. TR1; Output characteristics: drain current as a function of drain-source voltage; typical values



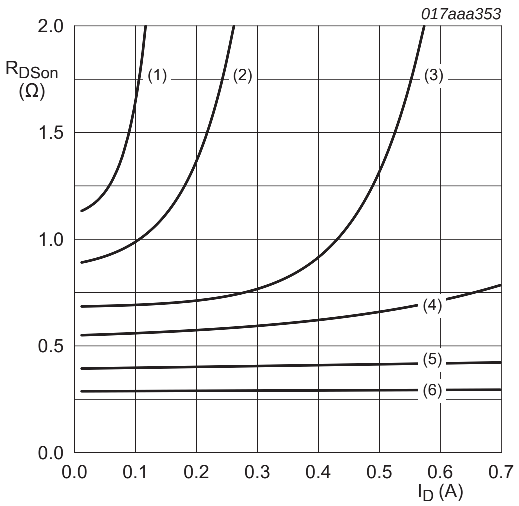
T_j = 25 °C; V_{DS} = 5 V

(1) minimum values

(2) typical values

(3) maximum values

Fig 10. TR1; Sub-threshold drain current as a function of gate-source voltage



T_j = 25 °C

(1) V_{GS} = 1.3 V

(2) V_{GS} = 1.4 V

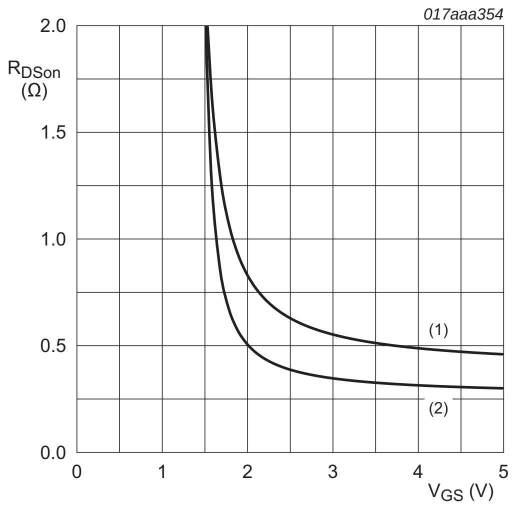
(3) V_{GS} = 1.6 V

(4) V_{GS} = 1.8 V

(5) V_{GS} = 2.5 V

(6) V_{GS} = 4.5 V

Fig 11. TR1; Drain-source on-state resistance as a function of drain current; typical values

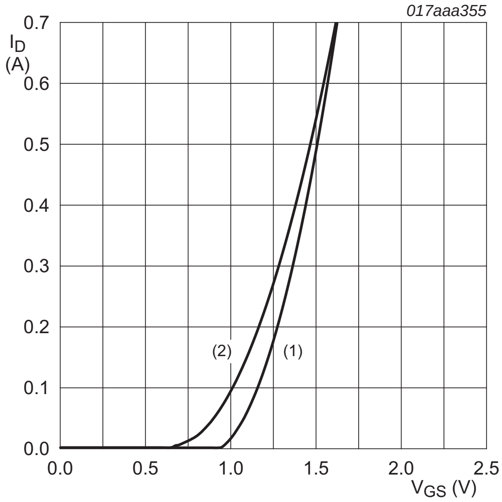


I_D = 400 mA

(1) T_j = 150 °C

(2) T_j = 25 °C

Fig 12. TR1; Drain-source on-state resistance as a function of gate-source voltage; typical values

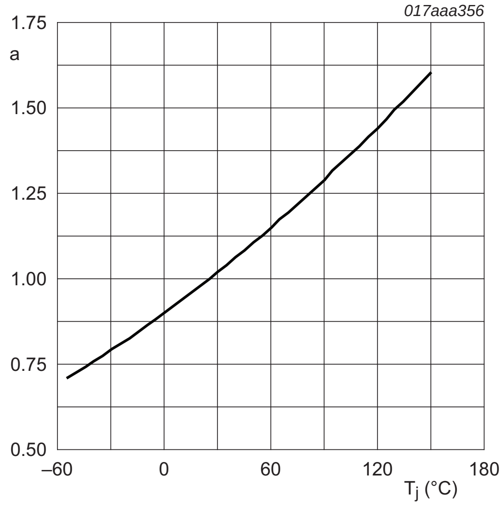


$V_{DS} > I_D \times R_{DSon}$

(1) $T_j = 25$ °C

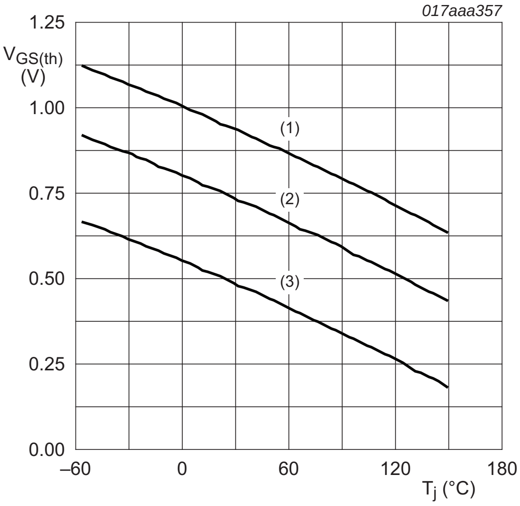
(2) $T_j = 150$ °C

Fig 13. TR1; Transfer characteristics: drain current as a function of gate-source voltage; typical values



$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 14. TR1; Normalized drain-source on-state resistance as a function of junction temperature; typical values



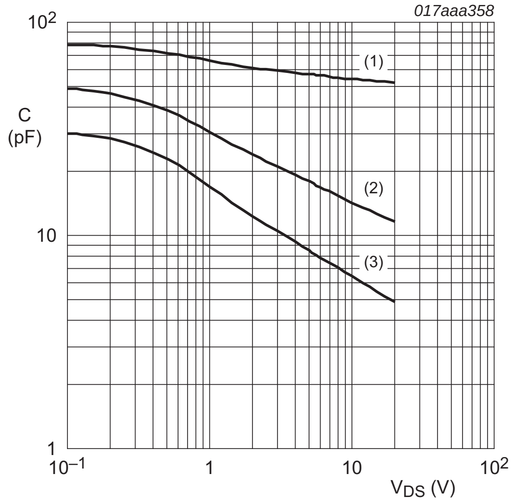
$I_D = 0.25$ mA; $V_{DS} = V_{GS}$

(1) maximum values

(2) typical values

(3) minimum values

Fig 15. TR1; Gate-source threshold voltage as a function of junction temperature



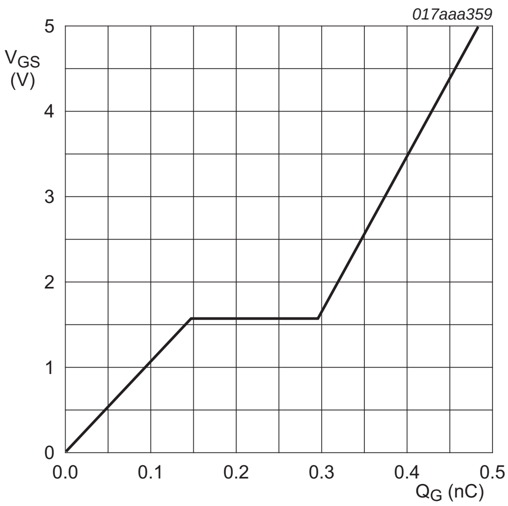
f = 1 MHz; $V_{GS} = 0$ V

(1) C_{iss}

(2) C_{oss}

(3) C_{rss}

Fig 16. TR1; Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



I_D = 0.5 A; V_{DS} = 10 V; T_{amb} = 25 °C

Fig 17. TR1; Gate-source voltage as a function of gate charge; typical values

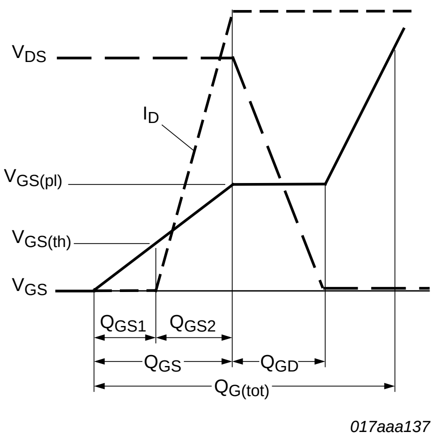
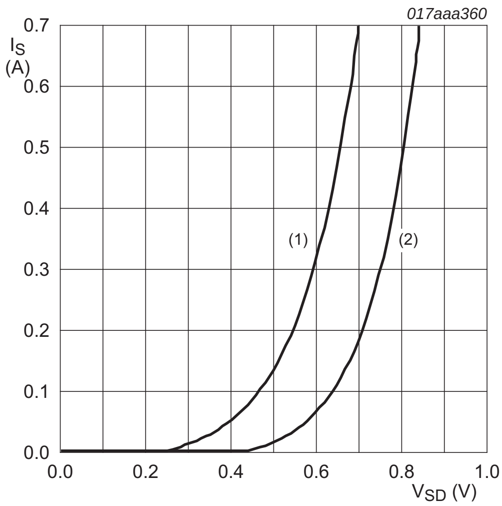


Fig 18. Gate charge waveform definitions

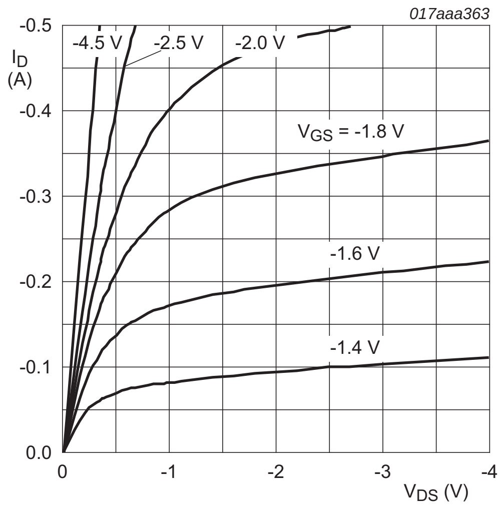


V_{GS} = 0 V

(1) T_j = 150 °C

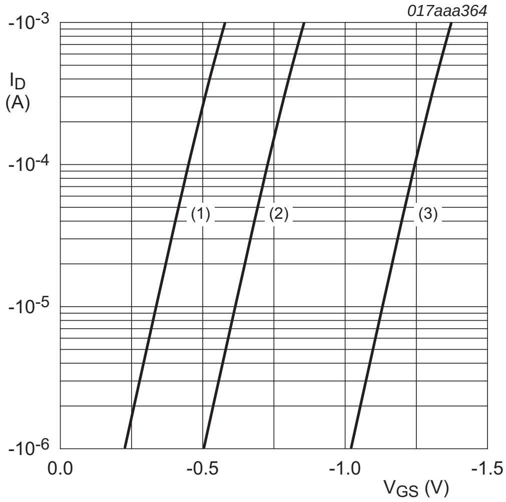
(2) T_j = 25 °C

Fig 19. TR1; Source current as a function of source-drain voltage; typical values



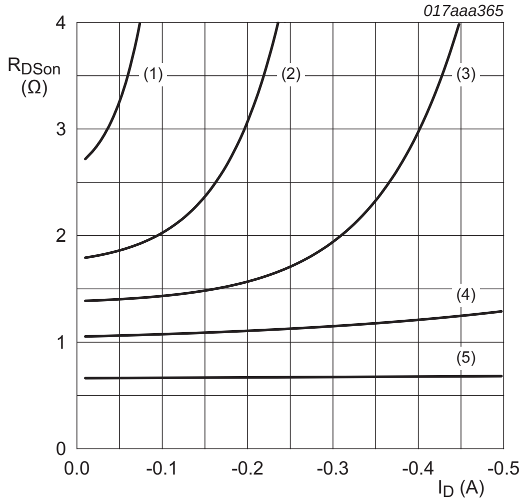
T_j = 25 °C

Fig 20. TR2; Output characteristics: drain current as a function of drain-source voltage; typical values



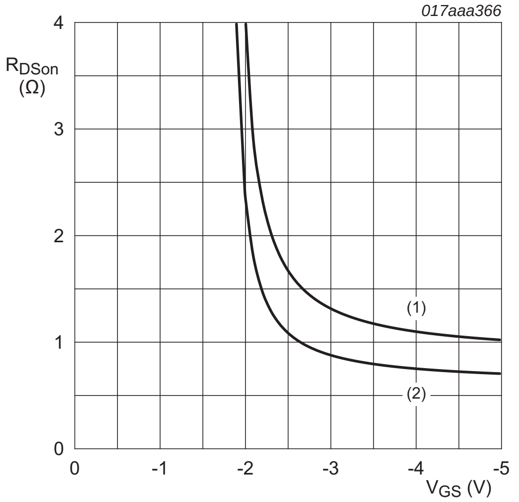
T_j = 25 °C; V_{DS} = -5 V
(1) minimum values
(2) typical values
(3) maximum values

Fig 21. TR2; Sub-threshold drain current as a function of gate-source voltage



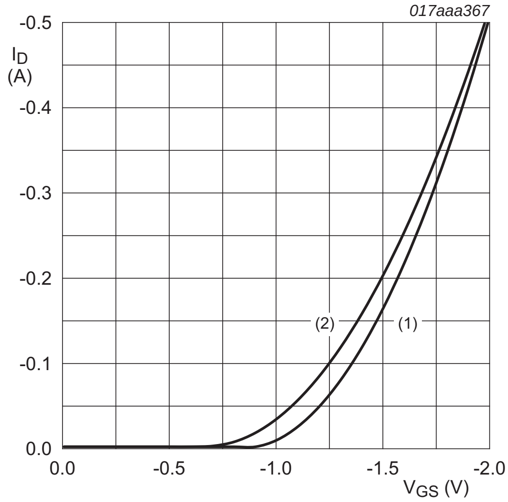
T_j = 25 °C
(1) V_{GS} = -1.5 V
(2) V_{GS} = -1.8 V
(3) V_{GS} = -2.0 V
(4) V_{GS} = -2.5 V
(5) V_{GS} = -4.5 V

Fig 22. TR2; Drain-source on-state resistance as a function of drain current; typical values



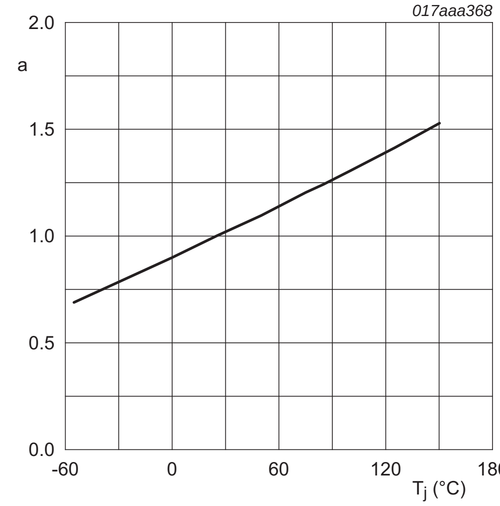
I_D = -400 mA
(1) T_j = 150 °C
(2) T_j = 25 °C

Fig 23. TR2; Drain-source on-state resistance as a function of gate-source voltage; typical values



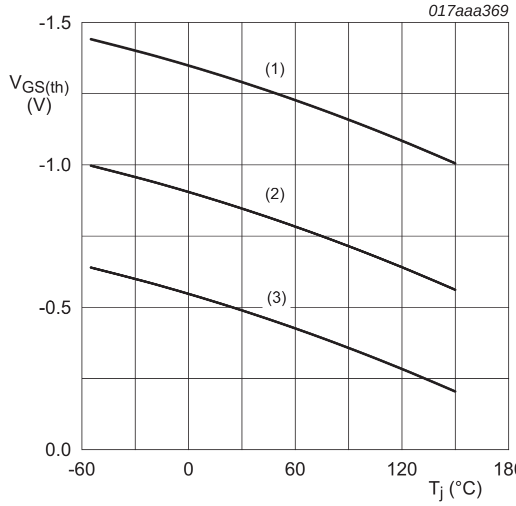
$V_{DS} > I_D \times R_{DSon}$
(1) T_j = 25 °C
(2) T_j = 150 °C

Fig 24. TR2; Transfer characteristics: drain current as a function of gate-source voltage; typical values



$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 25. TR2; Normalized drain-source on-state resistance as a function of ambient temperature; typical values



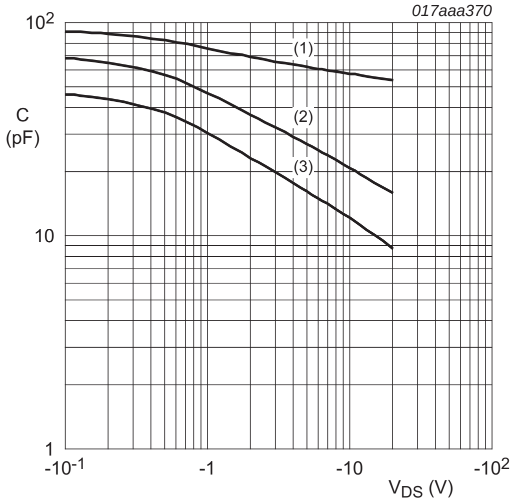
I_D = -0.25 mA; V_{DS} = V_{GS}

(1) maximum values

(2) typical values

(3) minimum values

Fig 26. TR2; Gate-source threshold voltage as a function of junction temperature



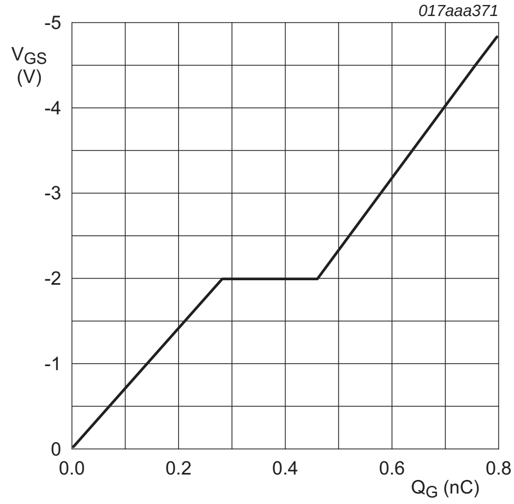
f = 1 MHz; V_{GS} = 0 V

(1) C_{iss}

(2) C_{oss}

(3) C_{rss}

Fig 27. TR2; Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



I_D = -0.4 A; V_{DD} = -10 V; T_{amb} = 25 °C

Fig 28. TR2; Gate-source voltage as a function of gate charge; typical values

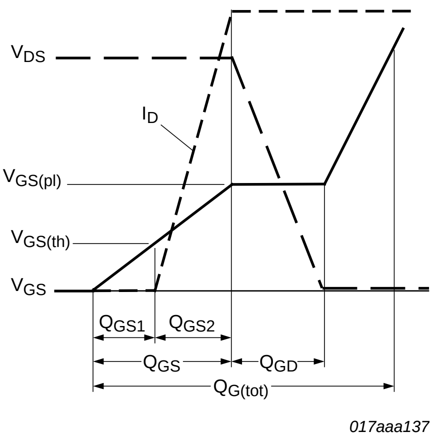
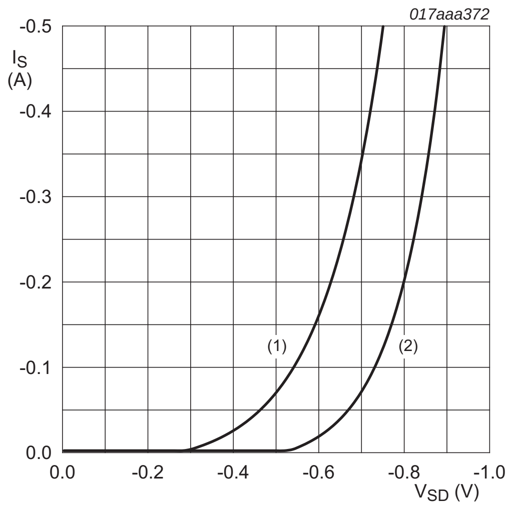


Fig 29. Gate charge waveform definitions



V_{GS} = 0 V

(1) T_{amb} = 150 °C

(2) T_{amb} = 25 °C

Fig 30. TR2; Source current as a function of source-drain voltage; typical values

8. Test information

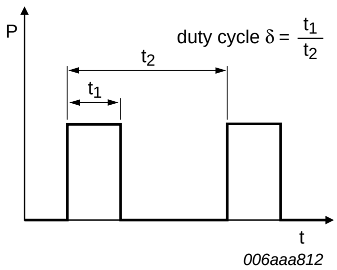


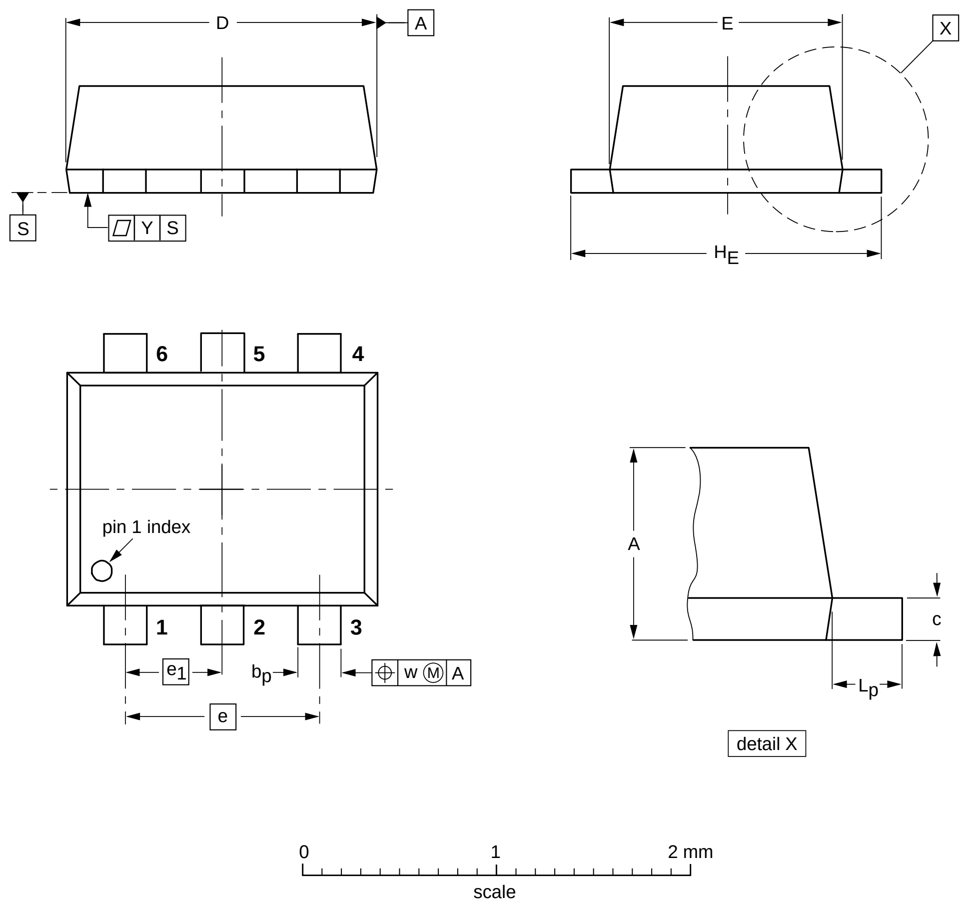
Fig 31. Duty cycle definition

8.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

9. Package outline

Plastic surface-mounted package; 6 leads **SOT666**



DIMENSIONS (mm are the original dimensions)

UNIT	A	b_p	c	D	E	e	e_1	H_E	L_p	w	y
mm	0.6 0.5	0.27 0.17	0.18 0.08	1.7 1.5	1.3 1.1	1.0	0.5	1.7 1.5	0.3 0.1	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT666						~~04-11-08~~ 06-03-16

Fig 32. Package outline SOT666

10. Soldering

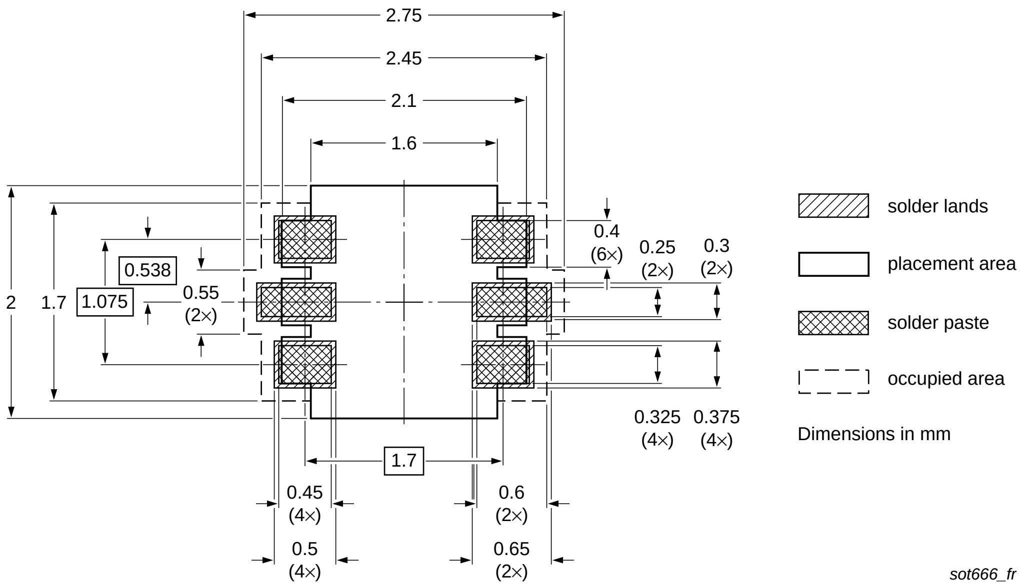


Fig 33. Reflow soldering footprint for SOT666

11. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PMDT290UCE v.1	20111006	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status [1] [2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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14. Contents

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Date of release: 06 October 2011