

PMDXB590UPE

20 V, dual P-channel Trench MOSFET

30 May 2023

Product data sheet

1. General description

Dual P-channel enhancement mode Field-Effect Transistor (FET) in a leadless ultra small DFN1010B-6 (SOT1216) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Low threshold voltage
- Very fast switching
- Trench MOSFET technology
- ElectroStatic Discharge (ESD) protection typically > 2 kV HBM

3. Applications

- Relay driver
- High-speed line driver
- High-side load switch
- Switching circuits

4. Quick reference data

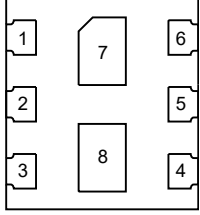
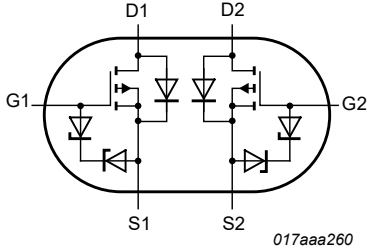
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$	-	-	-20	V
V_{GS}	gate-source voltage		-8	-	8	V
I_D	drain current	$V_{GS} = -4.5\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	-0.57	A
		$V_{GS} = -4.5\text{ V}; T_{sp} = 25\text{ °C}$		-	-2.3	A
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = -4.5\text{ V}; I_D = -1.2\text{ A}; T_j = 25\text{ °C}$	-	590	770	mΩ

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 1 cm².

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source TR1	 <p>Transparent top view DFN1010B-6 (SOT1216)</p>	 <p>017aaa260</p>
2	G1	gate TR1		
3	D2	drain TR2		
4	S2	source TR2		
5	G2	gate TR2		
6	D1	drain TR1		
7	D1	drain TR1		
8	D2	drain TR2		

6. Ordering information

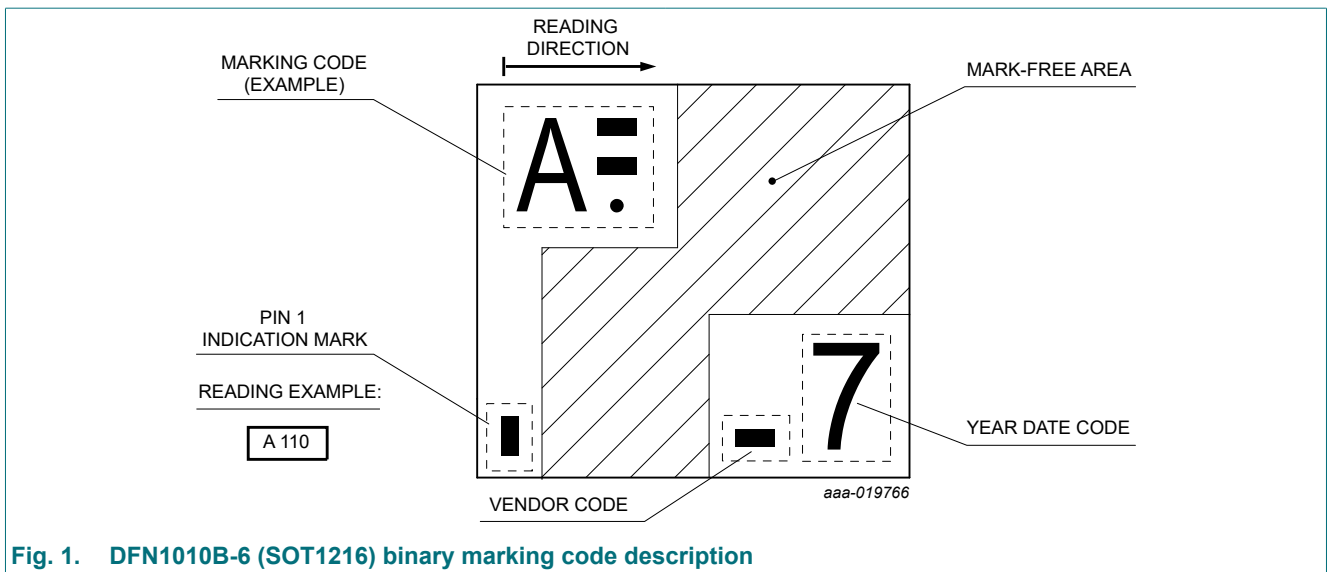
Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMDXB590UPE	DFN1010B-6	plastic, leadless thermal enhanced ultra thin small outline package; 6 terminals; 0.35 mm pitch; 1.1 mm x 1 mm x 0.37 mm body	SOT1216

7. Marking

Table 4. Marking codes

Type number	Marking code
PMDXB590UPE	D 010



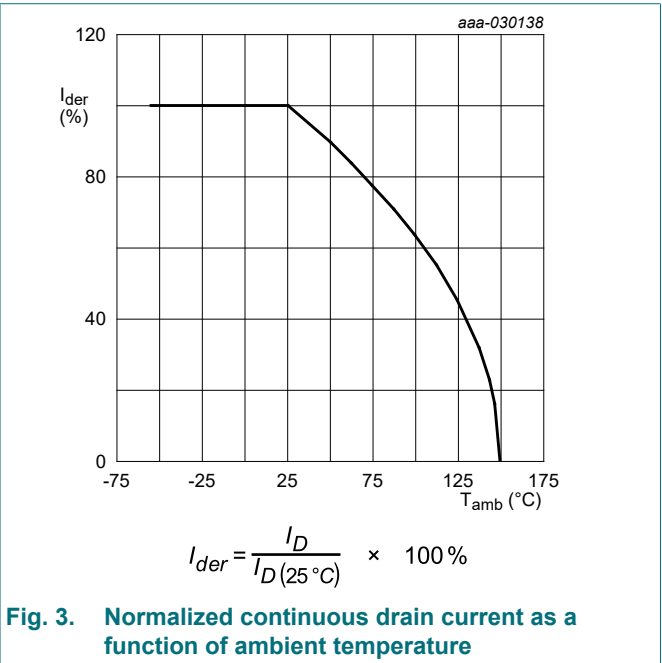
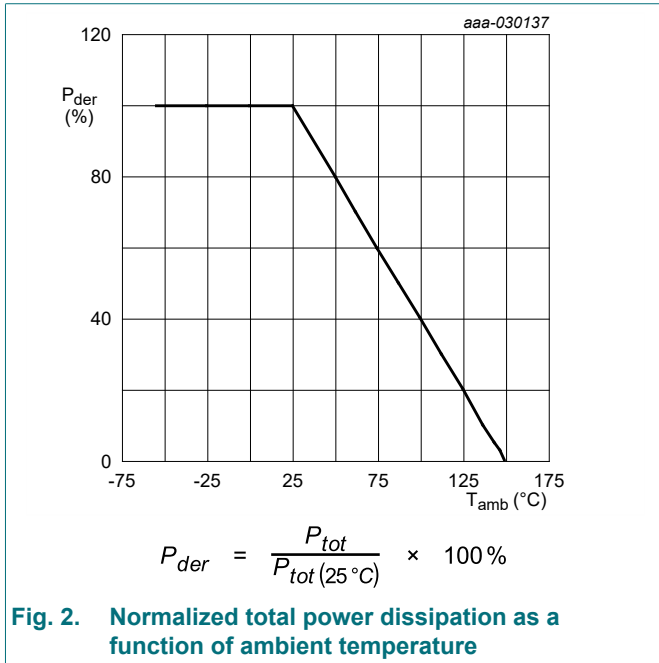
8. Limiting values

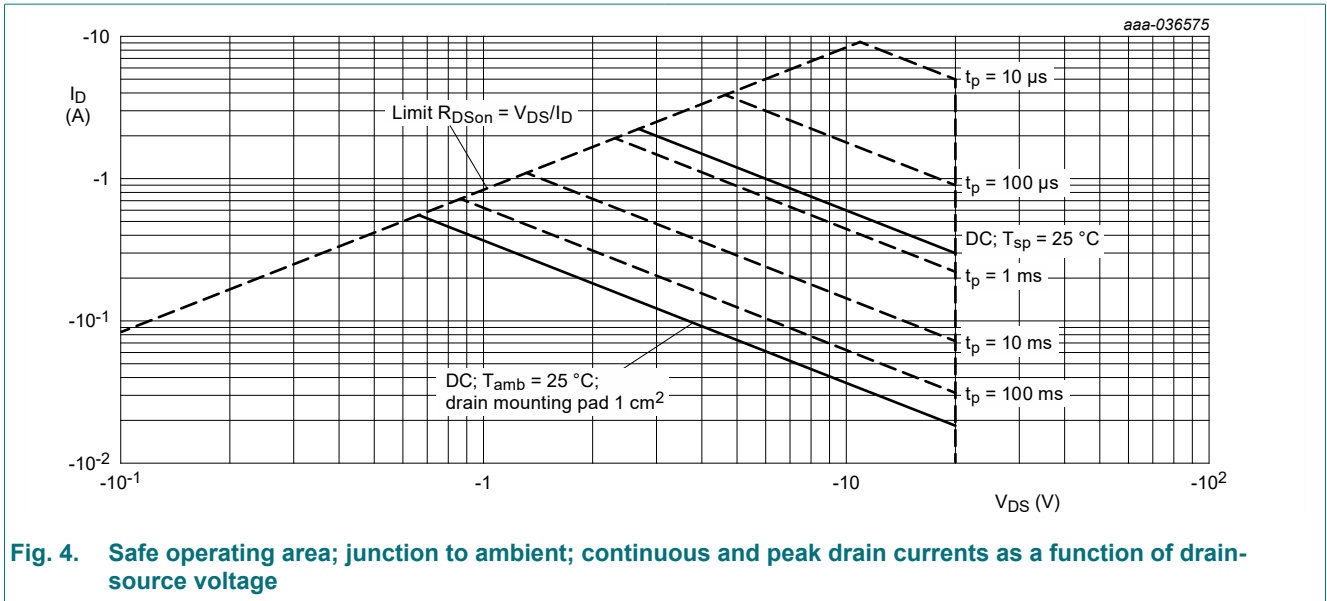
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
V _{DS}	drain-source voltage	T _j = 25 °C	-	-20	V	
V _{GS}	gate-source voltage		-8	8	V	
I _D	drain current	V _{GS} = -4.5 V; T _{amb} = 25 °C	[1]	-	-0.57	A
		V _{GS} = -4.5 V; T _{sp} = 25 °C		-	-2.3	A
		V _{GS} = -4.5 V; T _{amb} = 100 °C	[1]	-	-0.36	A
		V _{GS} = -4.5 V; T _{sp} = 100 °C		-	-1.5	A
I _{DM}	peak drain current	T _{amb} = 25 °C; single pulse; t _p ≤ 10 μs	-	-9.2	A	
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	280	mW
			[1]	-	370	mW
		T _{sp} = 25 °C		-	6	W
T _j	junction temperature		-55	150	°C	
T _{amb}	ambient temperature		-55	150	°C	
T _{stg}	storage temperature		-65	150	°C	
Source-drain diode						
I _S	source current	T _{amb} = 25 °C	[1]	-	-0.34	A

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 1 cm².
- [2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.





9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	386	444	K/W
			[2]	-	297	342	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	18	21	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm².

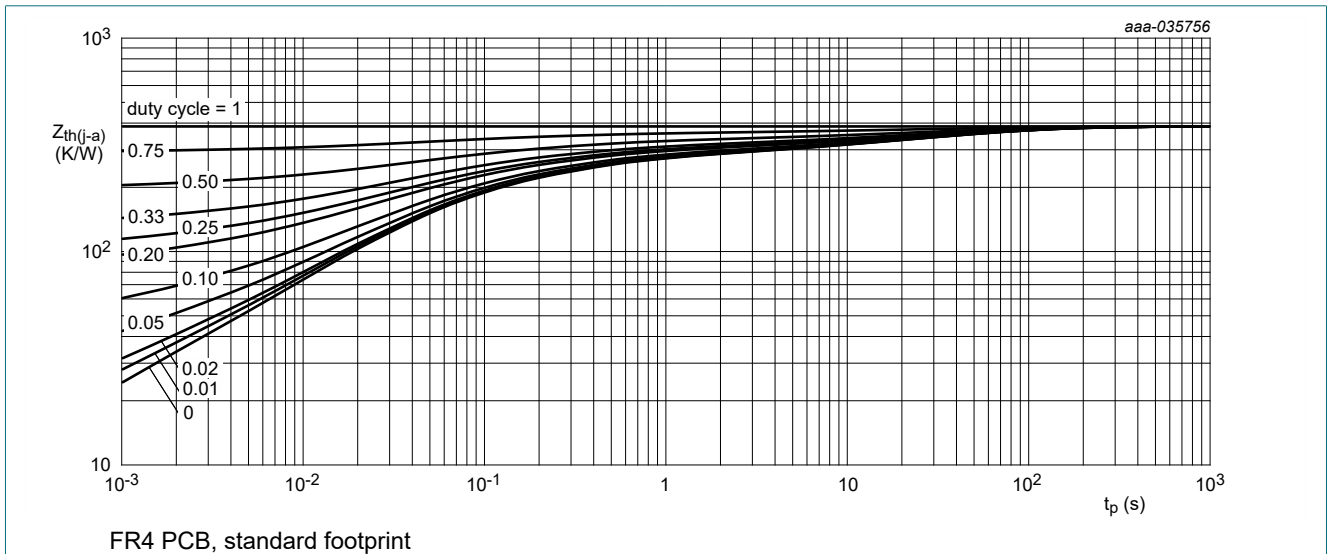


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

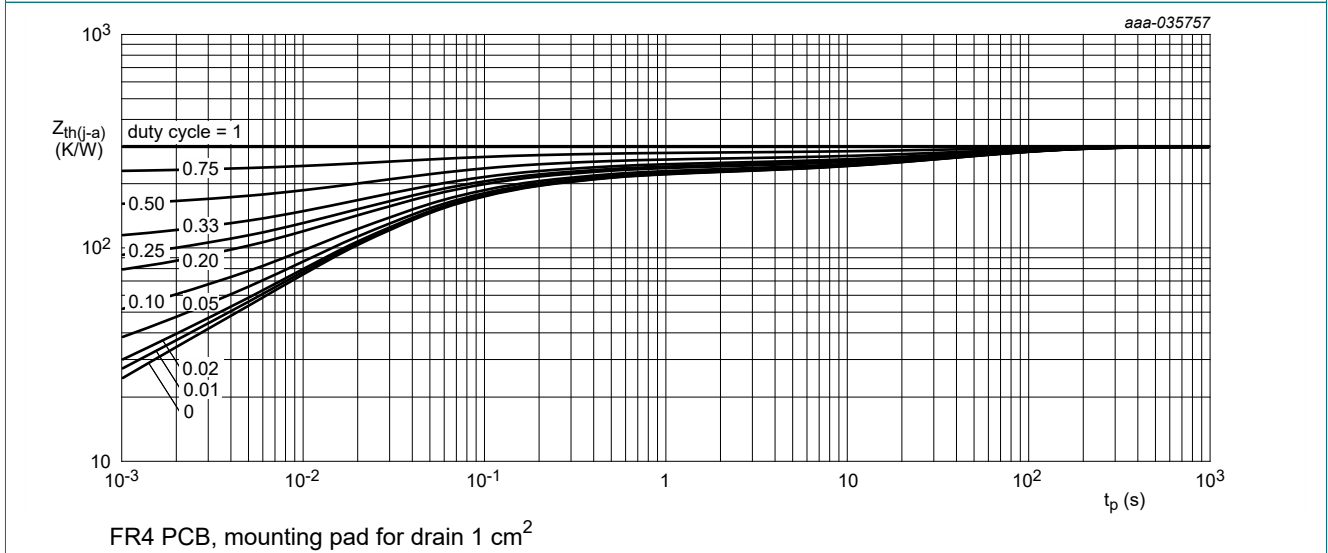


Fig. 6. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-20	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = -250 \mu\text{A}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C}$	-0.45	-0.7	-1	V
I_{DSS}	drain leakage current	$V_{DS} = -20 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	-1	μA
		$V_{DS} = -20 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ }^\circ\text{C}$	-	-	-20	μA
I_{GSS}	gate leakage current	$V_{GS} = -8 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	-10	μA
		$V_{GS} = 8 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	10	μA
		$V_{GS} = -4.5 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	-1	μA
		$V_{GS} = 4.5 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	1	μA
		$V_{GS} = -2.5 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	-500	nA
		$V_{GS} = 2.5 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	500	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = -4.5 \text{ V}; I_D = -1.2 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	590	770	m Ω
		$V_{GS} = -4.5 \text{ V}; I_D = -1.2 \text{ A}; T_j = 150 \text{ }^\circ\text{C}$	-	890	1200	m Ω
		$V_{GS} = -2.5 \text{ V}; I_D = -1 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	980	1400	m Ω
		$V_{GS} = -1.8 \text{ V}; I_D = -120 \text{ mA}; T_j = 25 \text{ }^\circ\text{C}$	-	1170	1970	m Ω
g_{fs}	forward transconductance	$V_{DS} = -5 \text{ V}; I_D = -0.6 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	1.2	-	S
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$V_{DS} = -10 \text{ V}; I_D = -0.6 \text{ A}; V_{GS} = -4.5 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.6	0.8	nC
Q_{GS}	gate-source charge		-	0.1	-	nC
Q_{GD}	gate-drain charge		-	0.1	-	nC
C_{iss}	input capacitance	$V_{DS} = -10 \text{ V}; f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	53.5	-	pF
C_{oss}	output capacitance		-	9.6	-	pF
C_{rss}	reverse transfer capacitance		-	7.8	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = -10 \text{ V}; I_D = -1.2 \text{ A}; V_{GS} = -4.5 \text{ V}; R_{G(ext)} = 6 \text{ } \Omega; T_j = 25 \text{ }^\circ\text{C}$	-	1	-	ns
t_r	rise time		-	3	-	ns
$t_{d(off)}$	turn-off delay time		-	6	-	ns
t_f	fall time		-	3.7	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = -0.34 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-0.9	-1.2	V

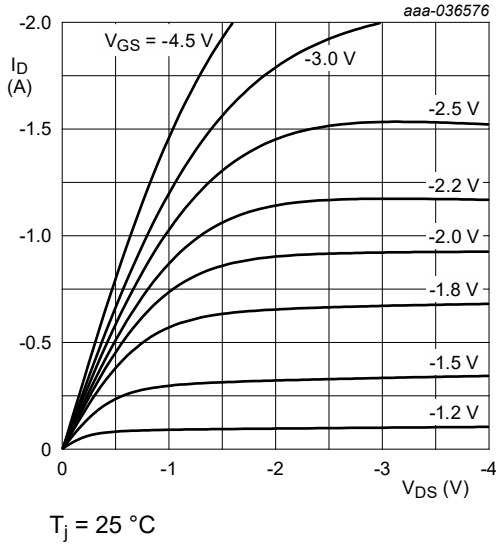


Fig. 7. Output characteristics: drain current as a function of drain-source voltage; typical values

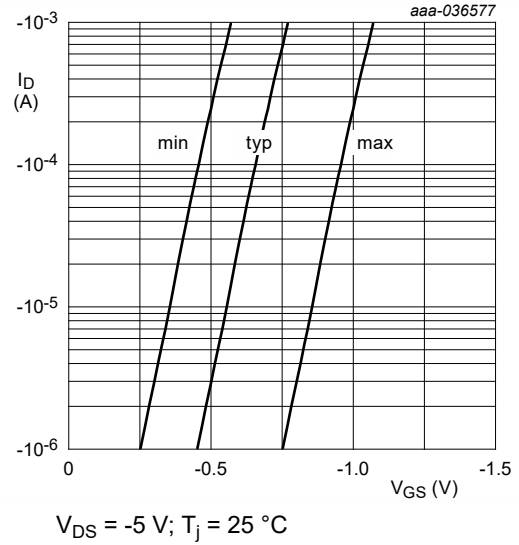


Fig. 8. Sub-threshold drain current as a function of gate-source voltage

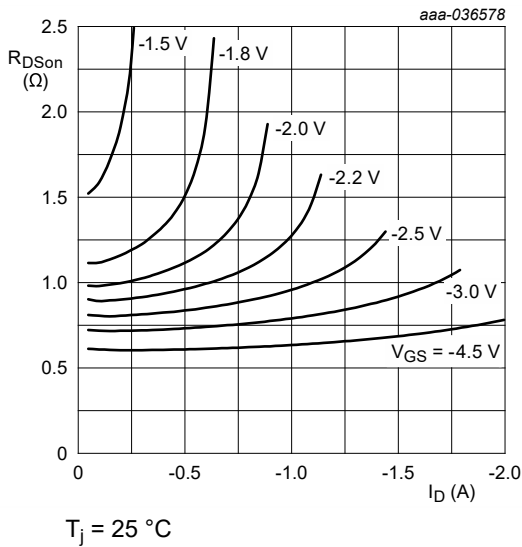


Fig. 9. Drain-source on-state resistance as a function of drain current; typical values

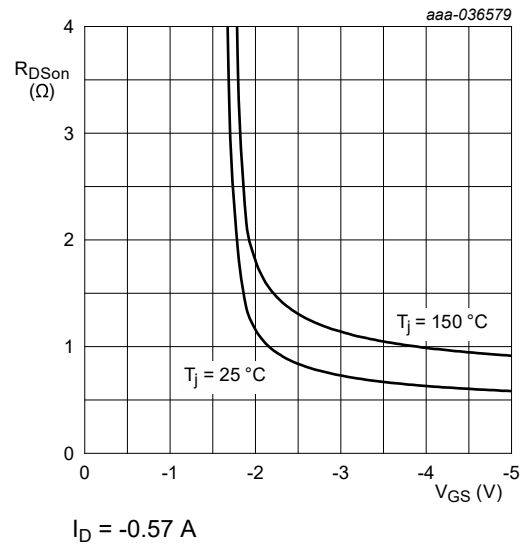


Fig. 10. Drain-source on-state resistance as a function of gate-source voltage; typical values

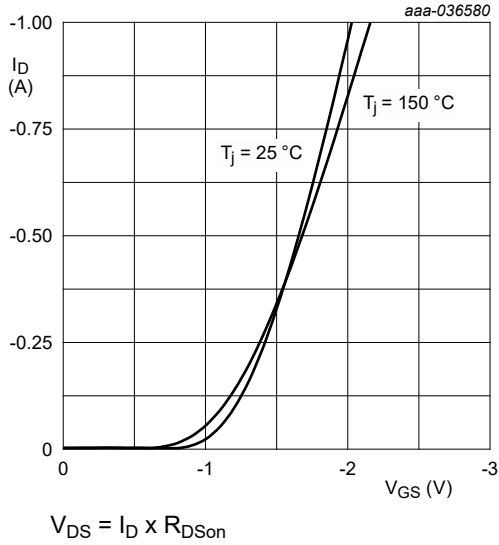


Fig. 11. Transfer characteristics: drain current as a function of gate-source voltage; typical values

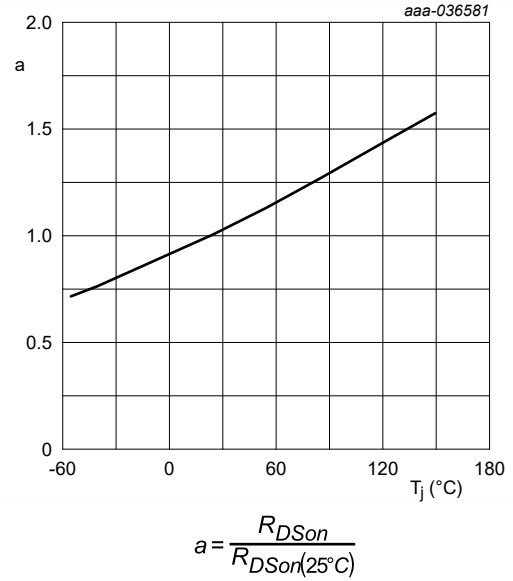


Fig. 12. Normalized drain-source on-state resistance as a function of junction temperature; typical values

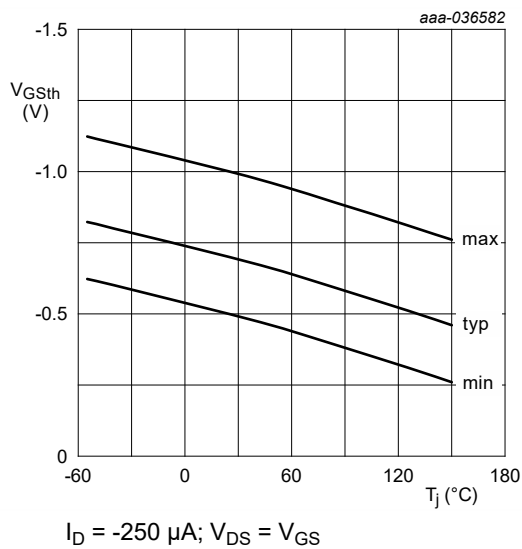


Fig. 13. Gate-source threshold voltage as a function of junction temperature

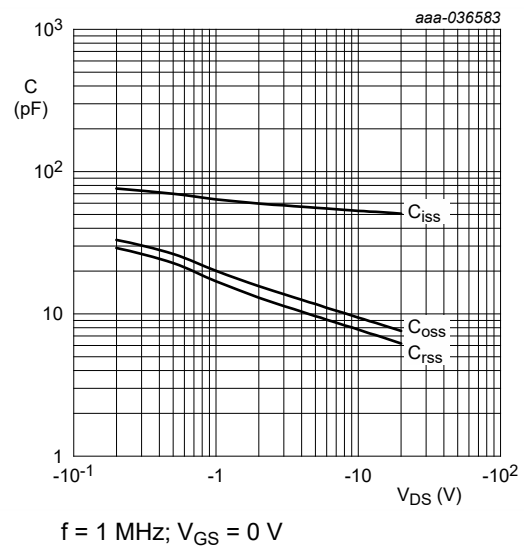
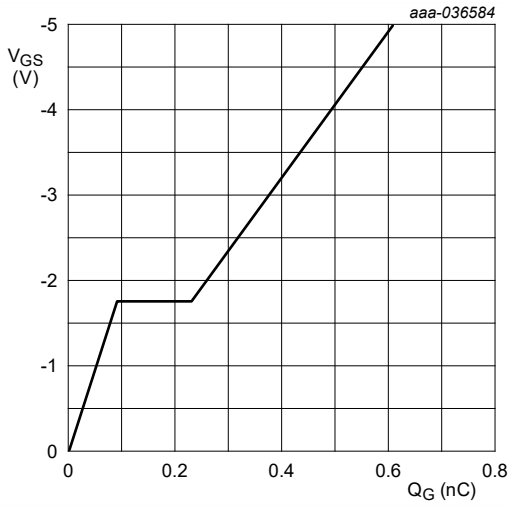


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{DS} = -10\text{ V}; I_D = -0.6\text{ A}; T_j = 25\text{ }^\circ\text{C}$

Fig. 15. Gate-source voltage as a function of gate charge; typical values

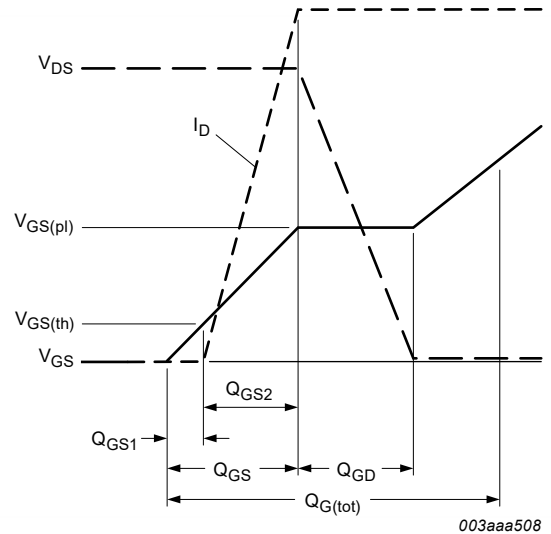
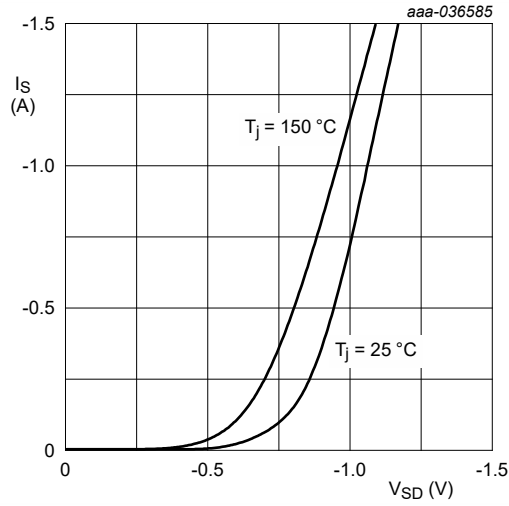


Fig. 16. Gate charge waveform definitions



$V_{GS} = 0\text{ V}$

Fig. 17. Source current as a function of source-drain voltage; typical values

11. Test information

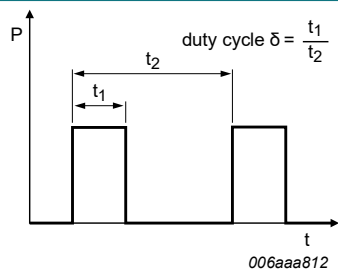
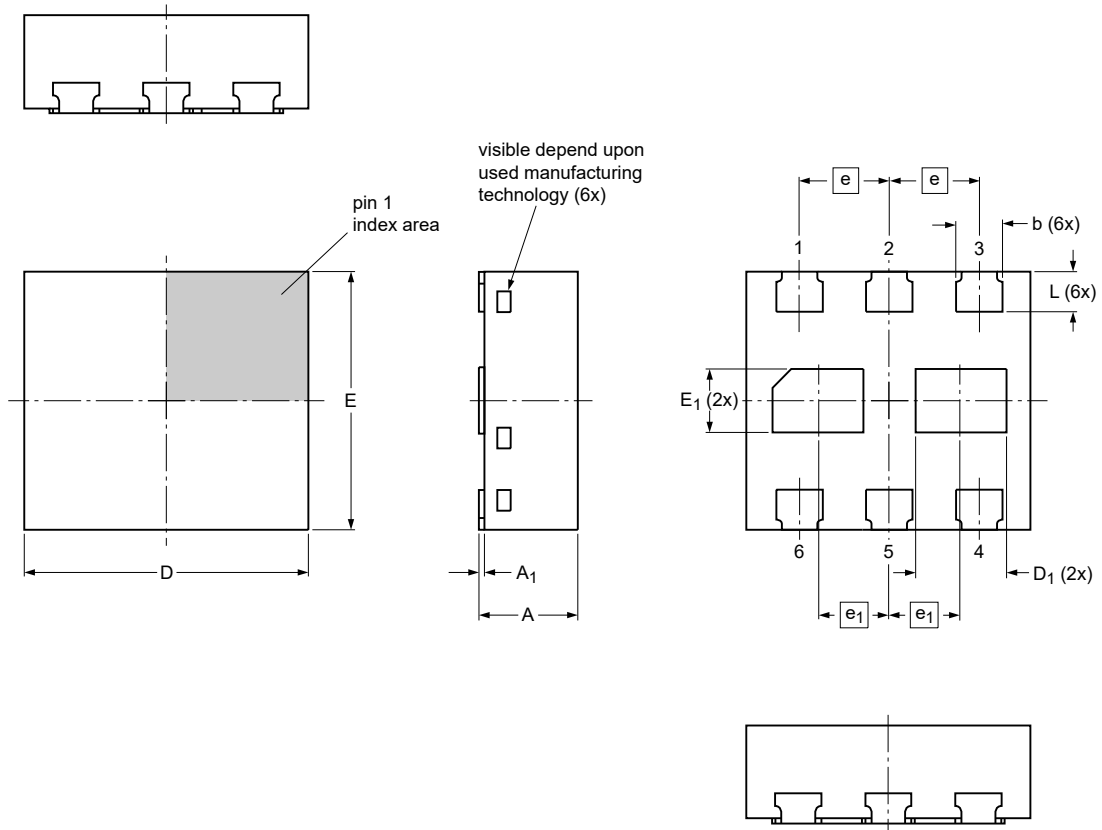


Fig. 18. Duty cycle definition

12. Package outline

DFN1010B-6: plastic thermal enhanced ultra thin small outline package; no leads;
6 terminals; body: 1.1 x 1.0 x 0.37 mm

SOT1216



Dimensions (mm are the original dimensions)

Unit	A	A ₁	b	D	D ₁	E	E ₁	e	e ₁	L
min	0.34		0.15	1.05	0.32	0.95	0.22			0.125
mm nom	0.37		0.18	1.10	0.35	1.00	0.25	0.35	0.275	0.155
max	0.40	0.04	0.23	1.15	0.40	1.05	0.30			0.205

Note

1. Dimension A is including plating thickness.

sot1216_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT1216					13-03-05 13-03-06

Fig. 19. Package outline DFN1010B-6 (SOT1216)

13. Soldering

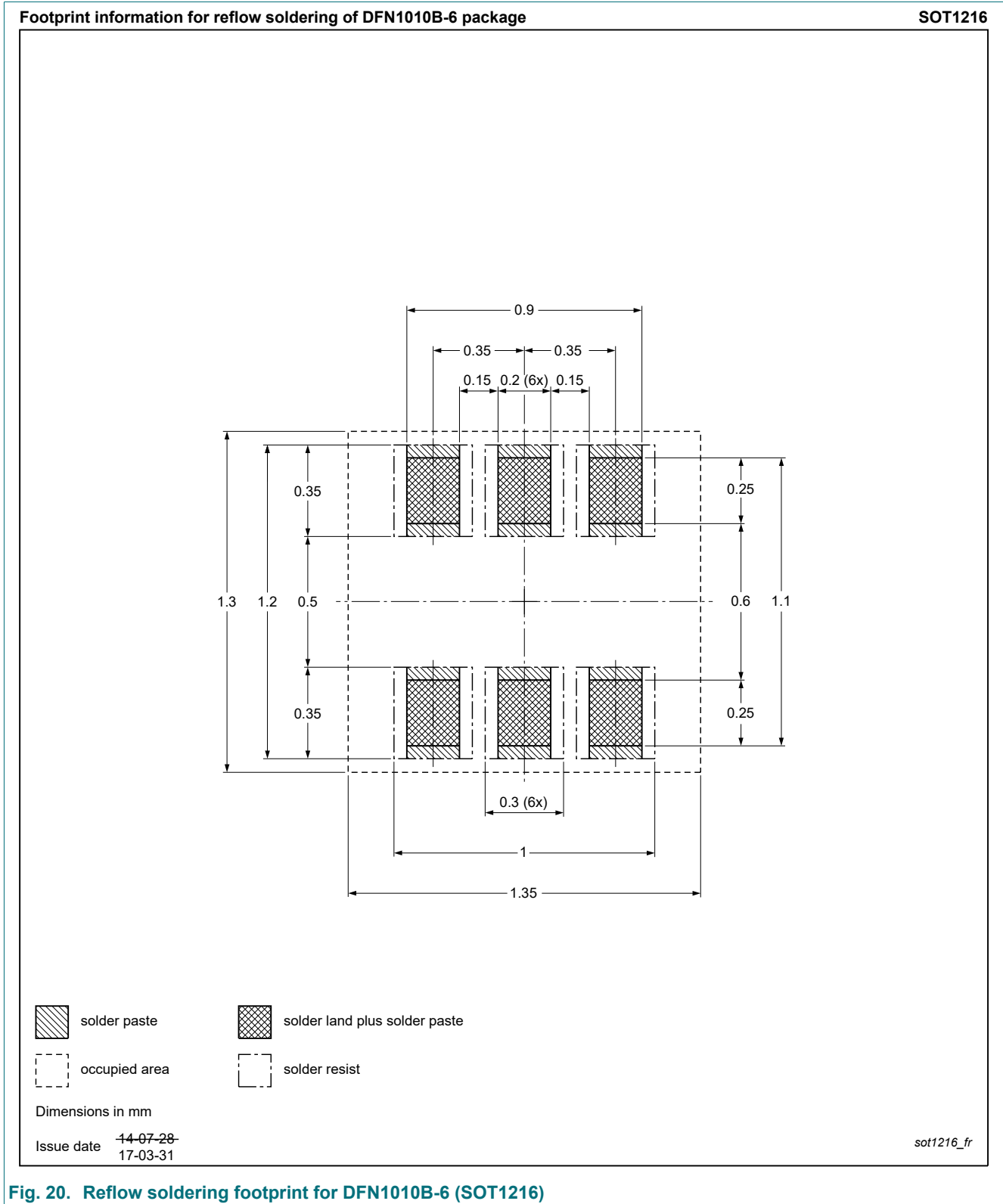


Fig. 20. Reflow soldering footprint for DFN1010B-6 (SOT1216)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMDXB590UPE v.1	20230530	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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