



# PMF370XN

## N-channel TrenchMOS extremely low level FET

5 July 2019

Product data sheet

### 1. General description

Extremely low level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

### 2. Features and benefits

- Low conduction losses due to low on-state resistance
- Low threshold voltage
- Saves PCB space due to small footprint (40 % smaller than SOT23)
- Suitable for low gate drive sources
- Surface-mounted package

### 3. Applications

- Driver circuits
- Switching in portable appliances

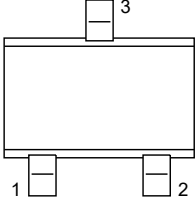
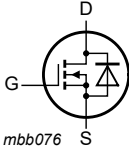
### 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	-	30	V
$I_D$	drain current	$V_{GS} = 4.5\text{ V}; T_{sp} = 25\text{ °C}$	-	-	0.87	A
$P_{tot}$	total power dissipation	$T_{sp} = 25\text{ °C}$	-	-	0.56	W
<b>Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}; I_D = 0.2\text{ A}; T_j = 25\text{ °C}$	-	370	440	mΩ

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>SC-70 (SOT323)</p>	 <p>mbb076</p>
2	S	source		
3	D	drain		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMF370XN	SC-70	plastic surface-mounted package; 3 leads	SOT323

## 7. Marking

Table 4. Marking codes

Type number	Marking code <sup>[1]</sup>
PMF370XN	F6%

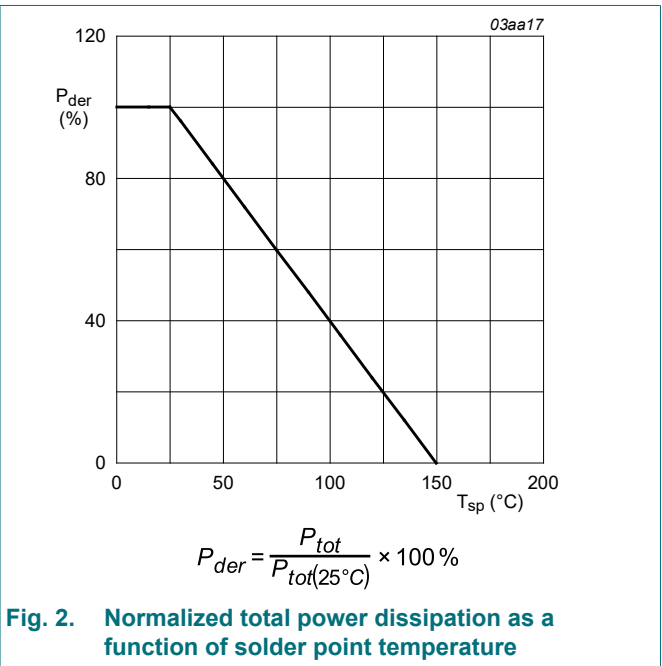
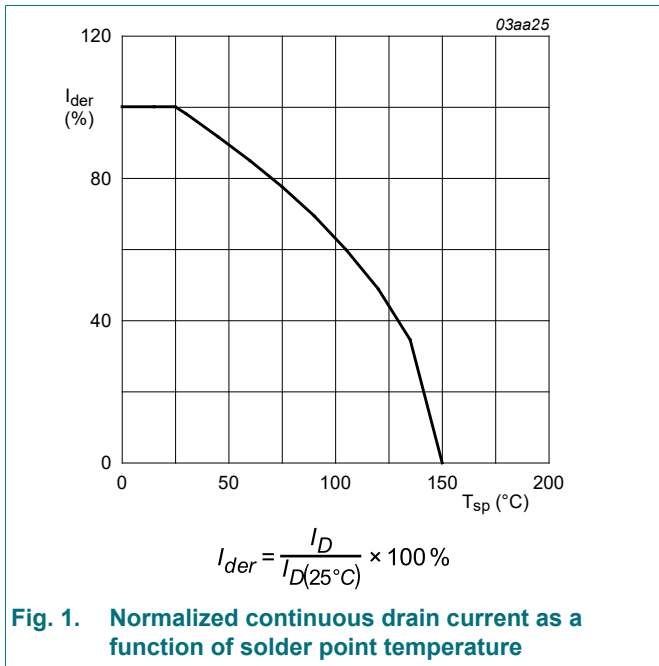
[1] % = placeholder for manufacturing site code

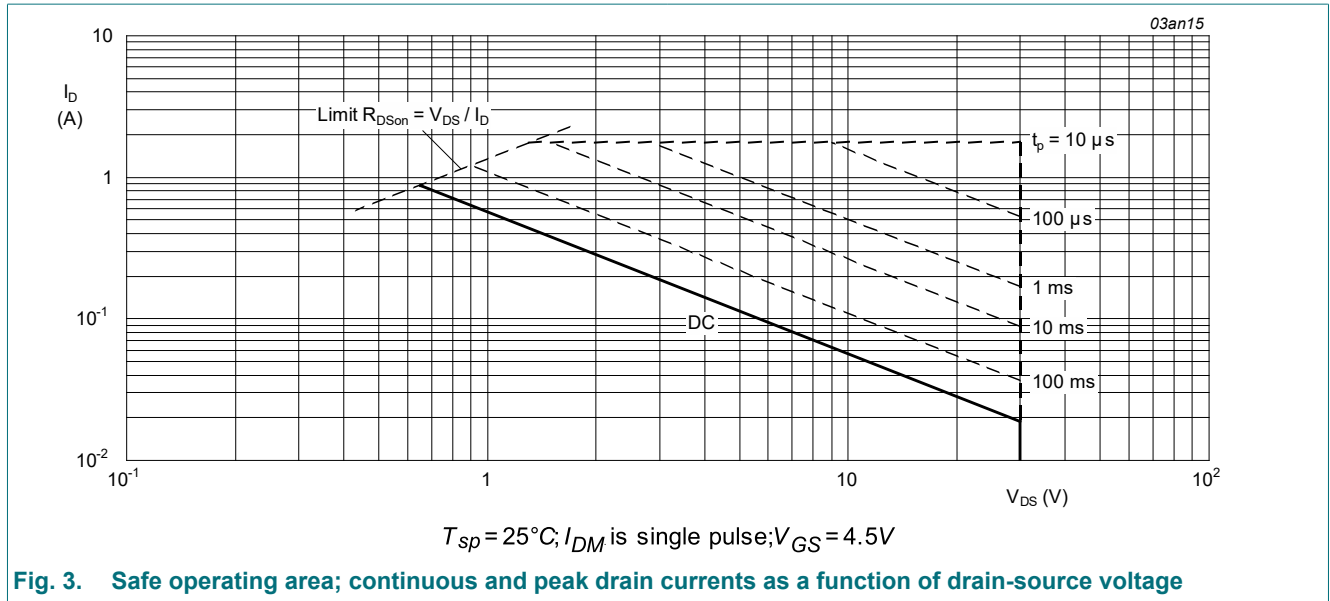
## 8. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134)

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	25 °C ≤ T <sub>j</sub> ≤ 150 °C	-	30	V
V <sub>DGR</sub>	drain-gate voltage	25 °C ≤ T <sub>j</sub> ≤ 150 °C; R <sub>GS</sub> = 20 kΩ	-	30	V
V <sub>GS</sub>	gate-source voltage		-12	12	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 4.5 V; T <sub>sp</sub> = 25 °C	-	0.87	A
		V <sub>GS</sub> = 4.5 V; T <sub>sp</sub> = 100 °C	-	0.55	A
I <sub>DM</sub>	peak drain current	T <sub>sp</sub> = 25 °C; pulsed; t <sub>p</sub> ≤ 10 μs	-	1.74	A
P <sub>tot</sub>	total power dissipation	T <sub>sp</sub> = 25 °C	-	0.56	W
T <sub>j</sub>	junction temperature		-55	150	°C
T <sub>stg</sub>	storage temperature		-55	150	°C
I <sub>S</sub>	source current	T <sub>sp</sub> = 25 °C	-	0.47	A
I <sub>SM</sub>	peak source current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>sp</sub> = 25 °C	-	0.94	A





## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	-	220	K/W

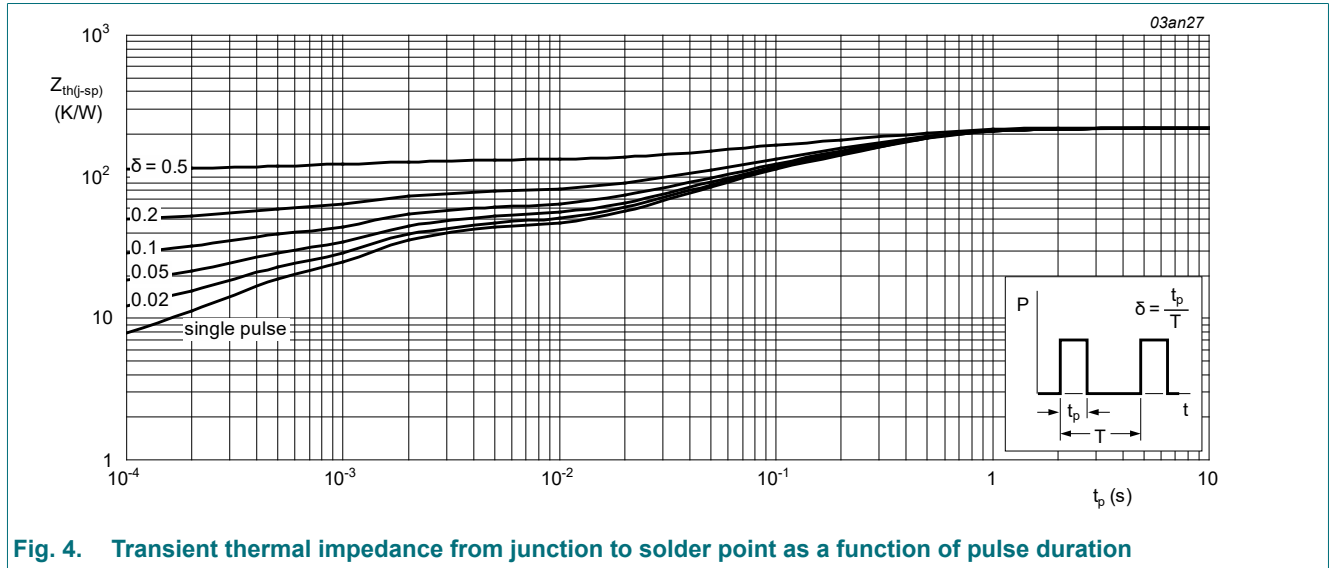


Fig. 4. Transient thermal impedance from junction to solder point as a function of pulse duration

## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	27	-	-	V
		$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	30	-	-	V
$V_{GSth}$	gate-source threshold voltage	$I_D = 250 \mu\text{A}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C}$	-	-	1.8	V
		$I_D = 250 \mu\text{A}; V_{DS} = V_{GS}; T_j = 150 \text{ }^\circ\text{C}$	0.35	-	-	V
		$I_D = 250 \mu\text{A}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C}$	0.5	1	1.5	V
$I_{DSS}$	drain leakage current	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 70 \text{ }^\circ\text{C}$	-	-	2	$\mu\text{A}$
		$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ }^\circ\text{C}$	-	-	10	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = 12 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	10	100	nA
		$V_{GS} = -12 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	10	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 2.5 \text{ V}; I_D = 0.1 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	550	650	m $\Omega$
		$V_{GS} = 4.5 \text{ V}; I_D = 0.2 \text{ A}; T_j = 150 \text{ }^\circ\text{C}$	-	629	748	m $\Omega$
		$V_{GS} = 4.5 \text{ V}; I_D = 0.2 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	370	440	m $\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$V_{DS} = 15 \text{ V}; I_D = 1 \text{ A}; V_{GS} = 4.5 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.65	-	nC
$Q_{GS}$	gate-source charge		-	0.14	-	nC
$Q_{GD}$	gate-drain charge		-	0.18	-	nC
$C_{iss}$	input capacitance	$V_{DS} = 25 \text{ V}; f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	37	-	pF
$C_{oss}$	output capacitance		-	8.5	-	pF
$C_{rss}$	reverse transfer capacitance		-	5.5	-	pF
$t_{d(on)}$	turn-on delay time		-	6.5	-	ns
$t_r$	rise time	$R_{G(ext)} = 6 \text{ } \Omega; T_j = 25 \text{ }^\circ\text{C}$	-	9.5	-	ns
$t_{d(off)}$	turn-off delay time		-	14	-	ns
$t_f$	fall time		-	5.5	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 0.3 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.81	1.2	V

N-channel TrenchMOS extremely low level FET

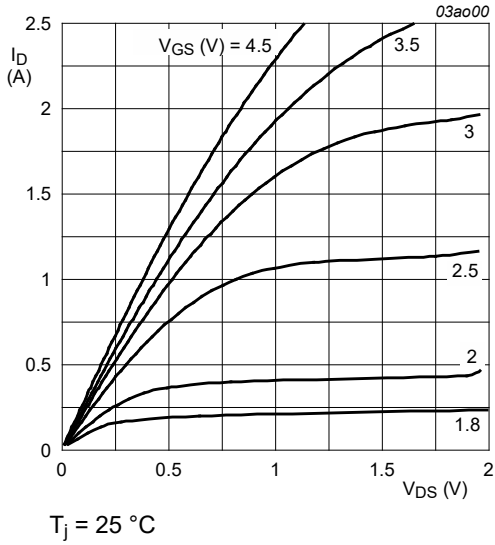


Fig. 5. Output characteristics: drain current as a function of drain-source voltage; typical values

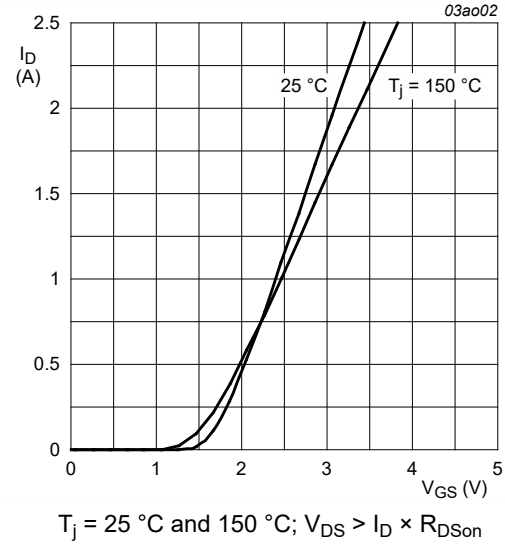


Fig. 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values

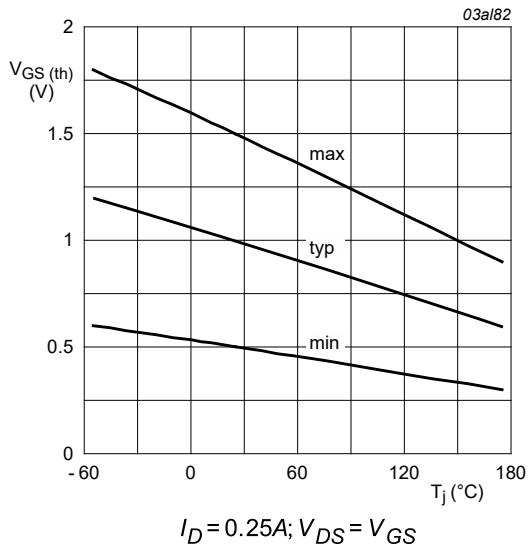


Fig. 7. Gate-source threshold voltage as a function of junction temperature

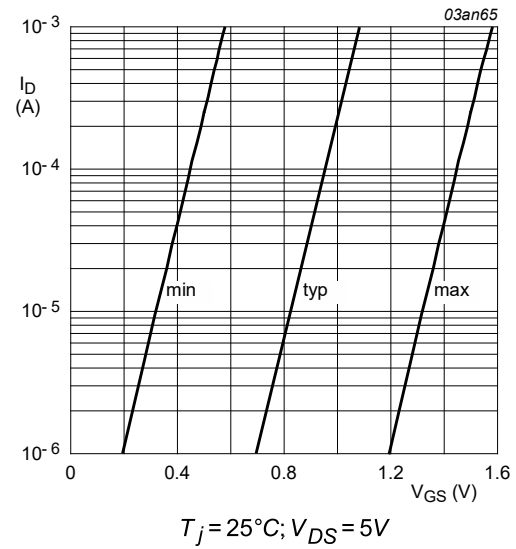


Fig. 8. Subthreshold drain current as a function of gate-source voltage

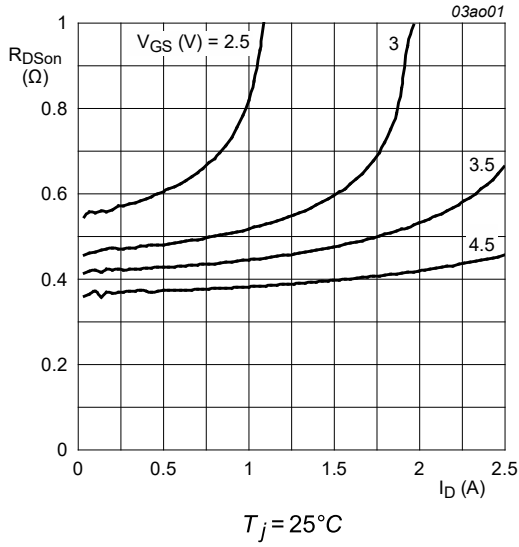


Fig. 9. Drain-source on-state resistance as a function of drain current; typical values

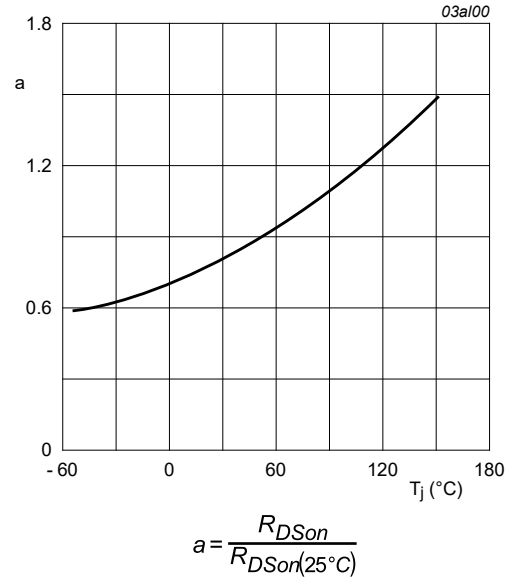


Fig. 10. Normalized drain-source on-state resistance factor as a function of junction temperature

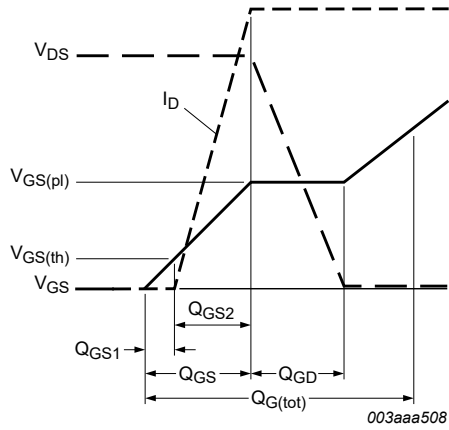


Fig. 11. Gate charge waveform definitions

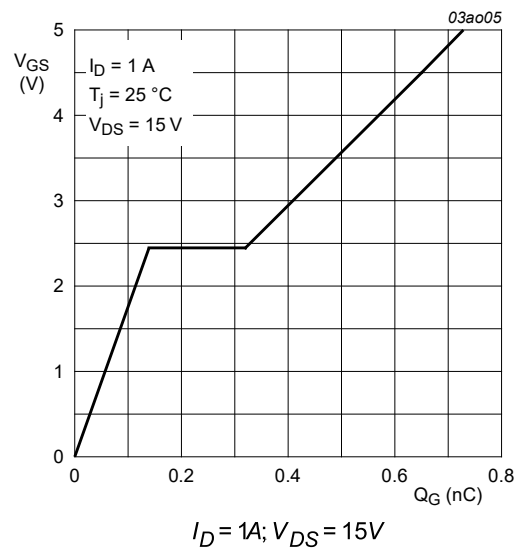
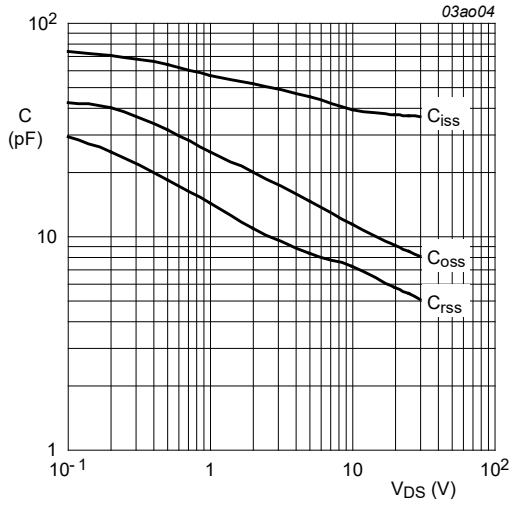


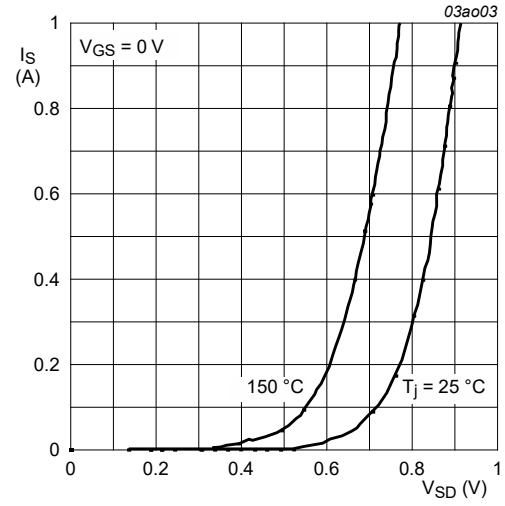
Fig. 12. Gate-source voltage as a function of gate charge; typical values





V<sub>GS</sub> = 0 V; 1 MHz

**Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



T<sub>j</sub> = 25 °C and 150 °C; V<sub>GS</sub> = 0 V

**Fig. 14. Source current as a function of source-drain voltage; typical values**

### 11. Package outline

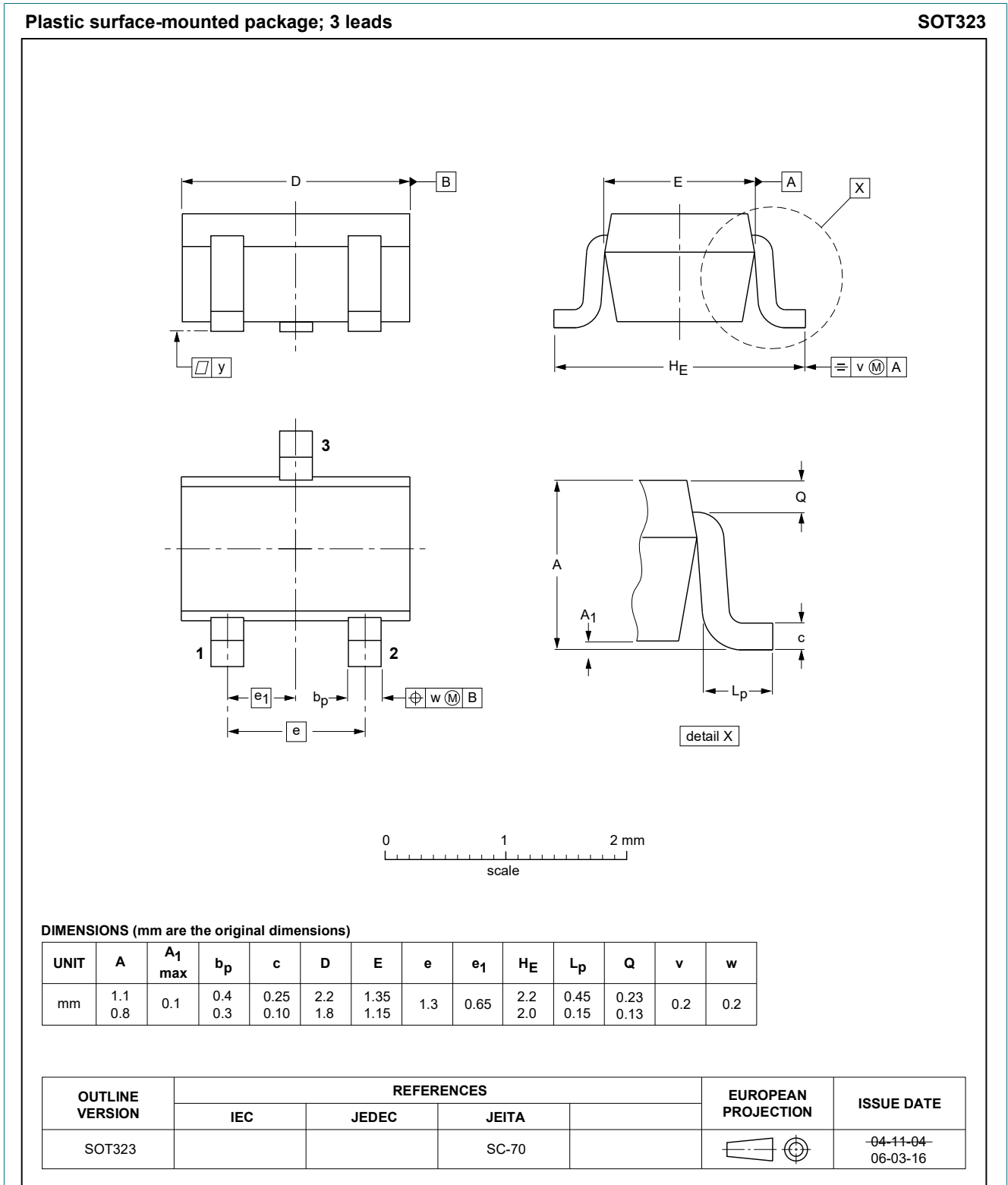


Fig. 15. Package outline SC-70 (SOT323)

## 12. Soldering

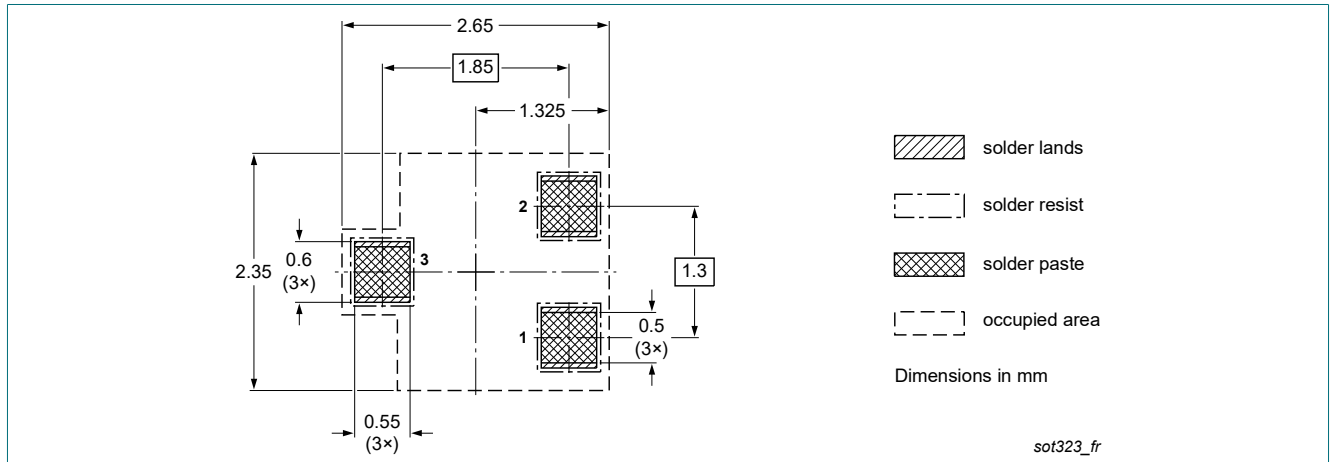


Fig. 16. Reflow soldering footprint for SC-70 (SOT323)

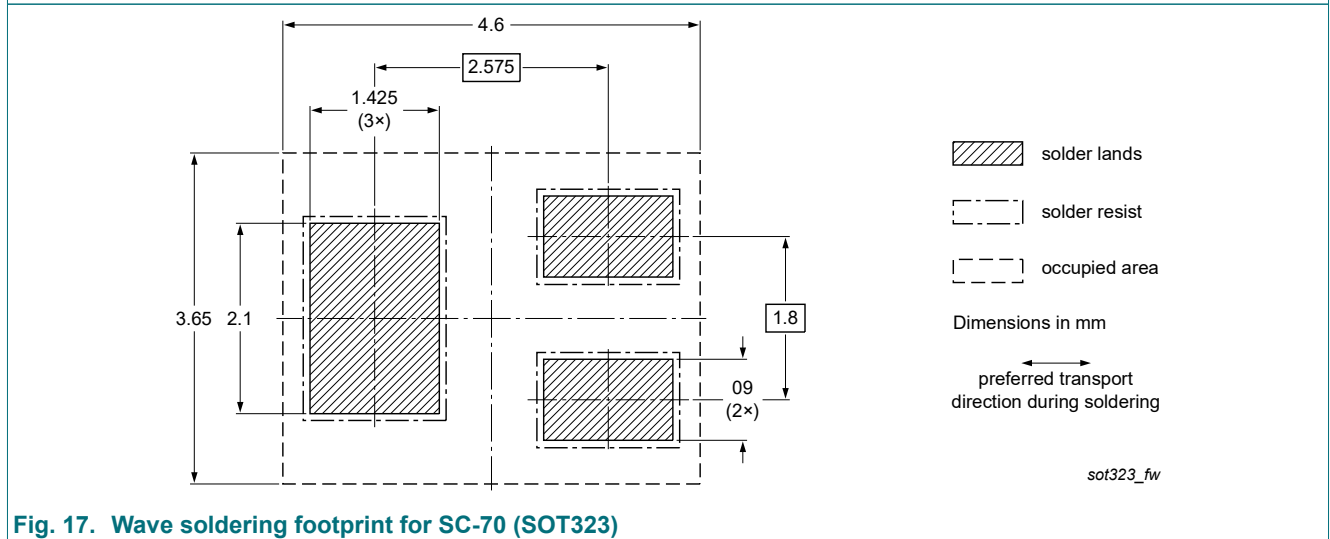


Fig. 17. Wave soldering footprint for SC-70 (SOT323)

## 13. Revision history

**Table 8. Revision history**

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMF370XN v.4	20190705	Product data sheet	-	PMF370XN v.3
Modifications:	<ul style="list-style-type: none"><li>• Measurement conditions for <math>V_{(BR)DSS}</math> revised.</li><li>• Legal texts have been adapted to the new company name where appropriate.</li><li>• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li></ul>			
PMF370XN v.3	20080620	Product data sheet	-	PMF370XN v.2
PMF370XN v.2	20051206	Product data sheet	-	PMF370XN v.1
PMF370XN v.1	20040211	Product data sheet	-	-

## 14. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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