Product data sheet

1. General description

P-channel enhancement mode Field-Effect Transistor (FET) in a leadless ultra small DFN0606-3 (SOT8001) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Low threshold voltage
- Very fast switching
- Trench MOSFET technology
- ElectroStatic Discharge (ESD) protection up to 1.8 kV HBM
- Leadless ultra small and ultra thin SMD plastic package: 0.62 × 0.62 × 0.37 mm

3. Applications

- Relay driver
- · High-speed line driver
- · High-side load switch
- · Switching circuits

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V _{DS}	drain-source voltage	T _j = 25 °C		-	-	-30	V
V _{GS}	gate-source voltage			-8	-	8	V
I _D	drain current	V _{GS} = -4.5 V; T _{amb} = 25 °C	[1]	-	-	-0.6	Α
Static characteristics							
R _{DSon}	drain-source on-state resistance	$V_{GS} = -4.5 \text{ V}; I_D = -0.5 \text{ A}; T_j = 25 \text{ °C}$		-	0.85	1	Ω

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 1 cm².



30 V, P-channel Trench MOSFET

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		D
2	S	source		
3	D	drain	Transparent top view DFN0606-3 (SOT8001)	G S S 017aaa259

6. Ordering information

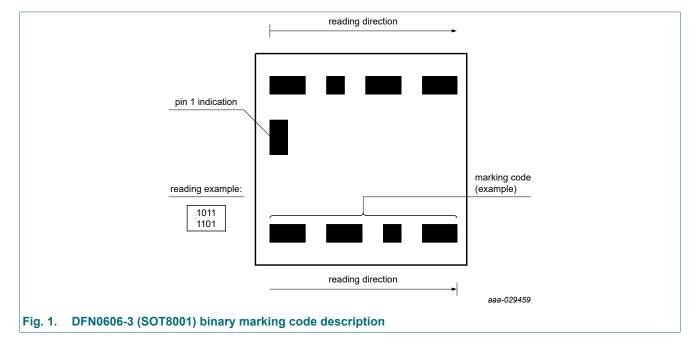
Table 3. Ordering information

Type number	Package					
	Name	Description	Version			
PMH850UPE		plastic, leadless ultra small package; 3 terminals; body 0.62 x 0.62 x 0.37 mm	SOT8001			

7. Marking

Table 4. Marking codes

Type number	Marking code
PMH850UPE	0001 1001



30 V, P-channel Trench MOSFET

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	T _j = 25 °C		-	-30	V
V _{GS}	gate-source voltage			-8	8	V
I _D	drain current	V _{GS} = -4.5 V; T _{amb} = 25 °C	[1]	-	-0.6	Α
		V _{GS} = -4.5 V; T _{amb} = 100 °C	[1]	-	-0.4	Α
I _{DM}	peak drain current	T _{amb} = 25 °C; single pulse; t _p ≤ 10 μs		-	-2	Α
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	0.36	W
			[1]	-	0.66	W
		T _{sp} = 25 °C		-	2.23	W
T _j	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
Source-drai	n diode			1		,
Is	source current	T _{amb} = 25 °C	[1]	-	-0.6	Α

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 1 cm².
- [2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

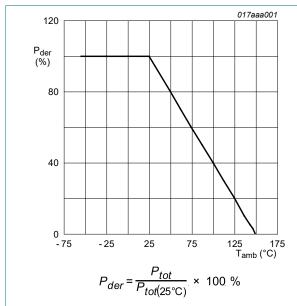


Fig. 2. Normalized total power dissipation as a function of ambient temperature

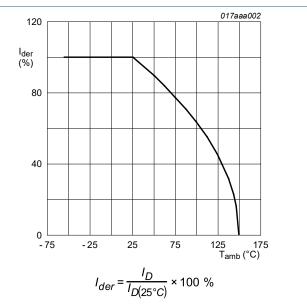


Fig. 3. Normalized continuous drain current as a function of ambient temperature

30 V, P-channel Trench MOSFET

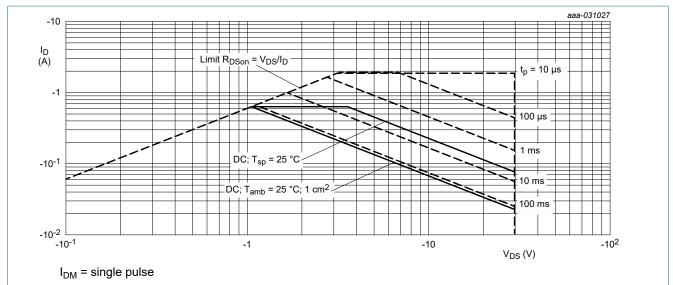


Fig. 4. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

30 V, P-channel Trench MOSFET

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
$R_{th(j-a)}$	thermal resistance from	in free air	[1]	-	287	344	K/W
junction to ambient		[2]	-	158	190	K/W	
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	47	56	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm².

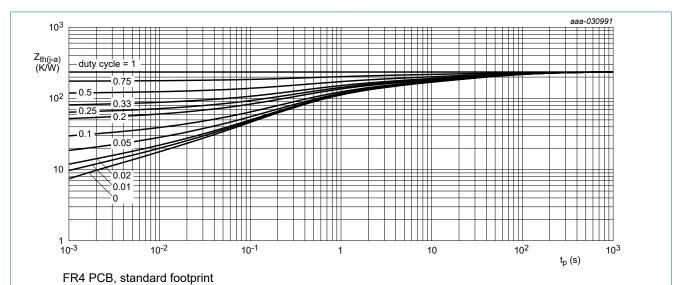
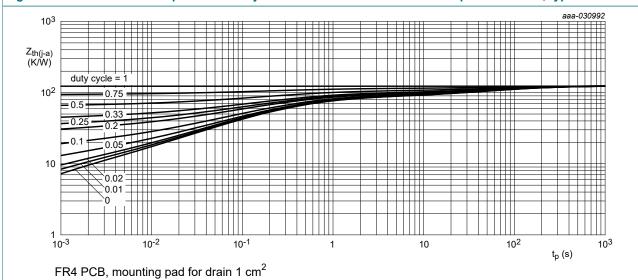


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



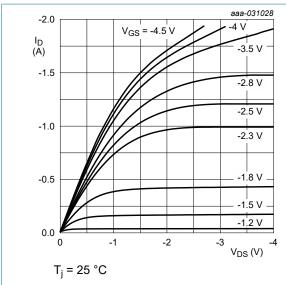
30 V, P-channel Trench MOSFET

10. Characteristics

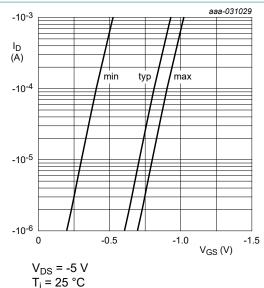
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics					
V _{(BR)DSS}	drain-source breakdown voltage	I_D = -250 μ A; V_{GS} = 0 V; T_j = 25 °C	-30	-	-	V
V_{GSth}	gate-source threshold voltage	I_D = -250 μ A; V_{DS} = V_{GS} ; T_j = 25 °C	-0.45	-0.7	-0.95	V
I _{DSS}	drain leakage current	V _{DS} = -30 V; V _{GS} = 0 V; T _j = 25 °C	-	-	-1	μA
		V _{DS} = -30 V; V _{GS} = 0 V; T _j = 150 °C	-	-	-20	μΑ
I _{GSS}	gate leakage current	$V_{GS} = -8 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	-5	μΑ
		V _{GS} = 8 V; V _{DS} = 0 V; T _j = 25 °C	-	-	5	μΑ
		$V_{GS} = -4.5 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C}$	-	-	-1	μΑ
		V _{GS} = 4.5 V; V _{DS} = 0 V; T _j = 25 °C	-	-	1	μΑ
		V _{GS} = -2.5 V; V _{DS} = 0 V; T _j = 25 °C	-	-	-100	nA
		V _{GS} = 2.5 V; V _{DS} = 0 V; T _j = 25 °C	-	-	100	nA
R _{DSon}	drain-source on-state resistance	$V_{GS} = -4.5 \text{ V}; I_D = -0.5 \text{ A}; T_j = 25 \text{ °C}$	-	0.85	1	Ω
		$V_{GS} = -4.5 \text{ V}; I_D = -0.5 \text{ A}; T_j = 150 ^{\circ}\text{C}$	-	1.43	1.7	Ω
		$V_{GS} = -2.5 \text{ V}; I_D = -0.3 \text{ A}; T_j = 25 \text{ °C}$	-	1.28	1.7	Ω
		V_{GS} = -1.8 V; I_D = -0.05 A; T_j = 25 °C	-	1.88	2.48	Ω
		V _{GS} = -1.5 V; I _D = -0.01 A; T _j = 25 °C	-	2.13	3.6	Ω
g _{fs}	forward transconductance	$V_{DS} = -10 \text{ V}; I_D = -0.5 \text{ A}; T_j = 25 \text{ °C}$	-	1	-	S
R _G	gate resistance	f = 1 MHz	-	19	-	Ω
Dynamic ch	naracteristics					
Q _{G(tot)}	total gate charge	$V_{DS} = -15 \text{ V}; I_D = -0.5 \text{ A}; V_{GS} = -4.5 \text{ V};$	-	0.6	0.9	nC
Q_{GS}	gate-source charge	T _j = 25 °C	-	0.11	-	nC
Q _{GD}	gate-drain charge	1	-	0.14	-	nC
C _{iss}	input capacitance	V _{DS} = -15 V; f = 1 MHz; V _{GS} = 0 V;	-	62.2	-	pF
C _{oss}	output capacitance	T _j = 25 °C	-	7.9	-	pF
C _{rss}	reverse transfer capacitance		-	4.8	-	pF
t _{d(on)}	turn-on delay time	$V_{DS} = -15 \text{ V}; I_D = -0.5 \text{ A}; V_{GS} = -4.5 \text{ V};$	-	6	-	ns
t _r	rise time	$R_{G(ext)} = 6 \Omega; T_j = 25 °C$	-	2	-	ns
t _{d(off)}	turn-off delay time	1 – –	-	2	-	ns
t _f	fall time	1 -	-	3	-	ns
Source-dra	in diode					
V _{SD}	source-drain voltage	I _S = -0.6 A; V _{GS} = 0 V; T _i = 25 °C	_	-0.7	-1.2	V

30 V, P-channel Trench MOSFET



Output characteristics: drain current as a Fig. 7. function of drain-source voltage; typical values



T_i = 25 °C

Sub-threshold drain current as a function of Fig. 8. gate-source voltage

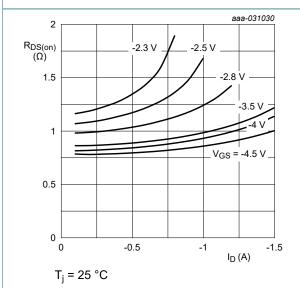


Fig. 9. Drain-source on-state resistance as a function of drain current; typical values

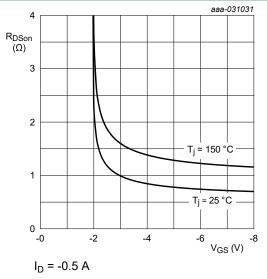


Fig. 10. Drain-source on-state resistance as a function of gate-source voltage; typical values

30 V, P-channel Trench MOSFET

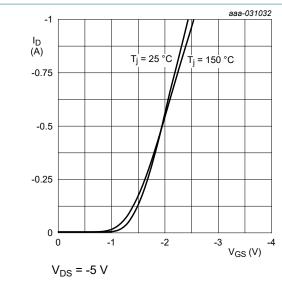


Fig. 11. Transfer characteristics: drain current as a function of gate-source voltage; typical values

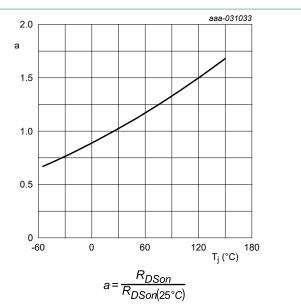


Fig. 12. Normalized drain-source on-state resistance as a function of junction temperature; typical values

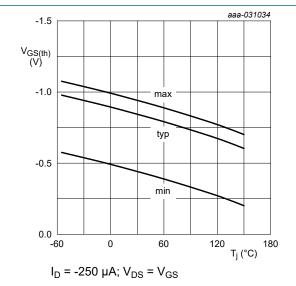


Fig. 13. Gate-source threshold voltage as a function of junction temperature

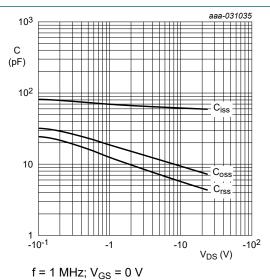


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

30 V, P-channel Trench MOSFET

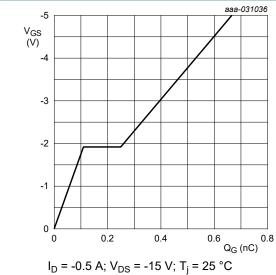


Fig. 15. Gate-source voltage as a function of gate

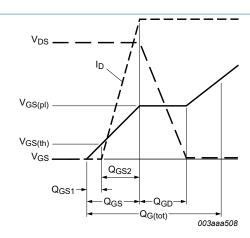


Fig. 16. Gate charge waveform definitions

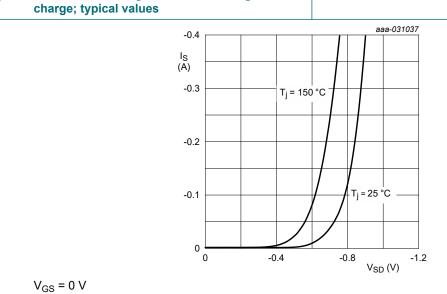
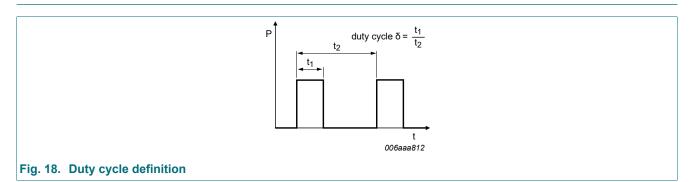


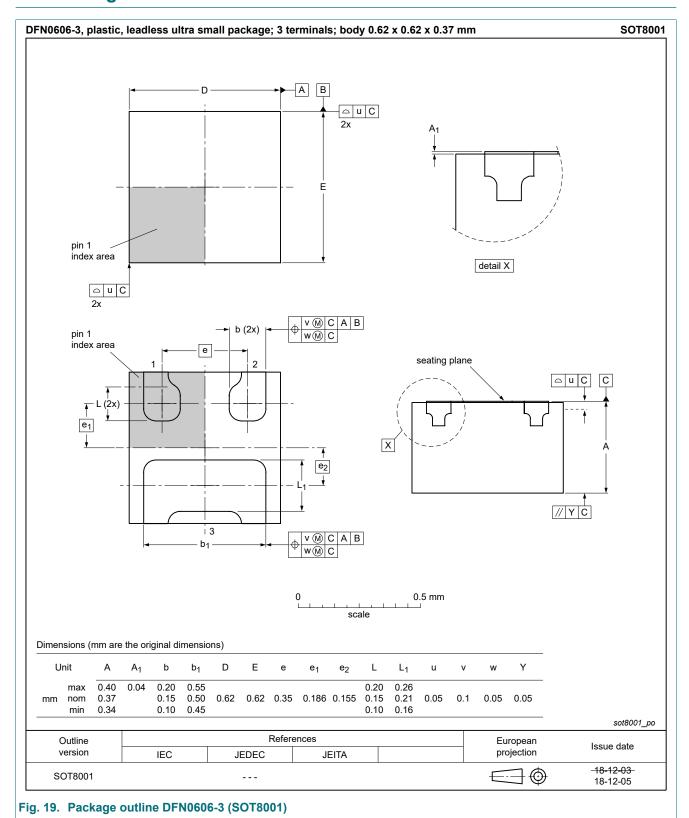
Fig. 17. Source current as a function of source-drain voltage; typical values

11. Test information



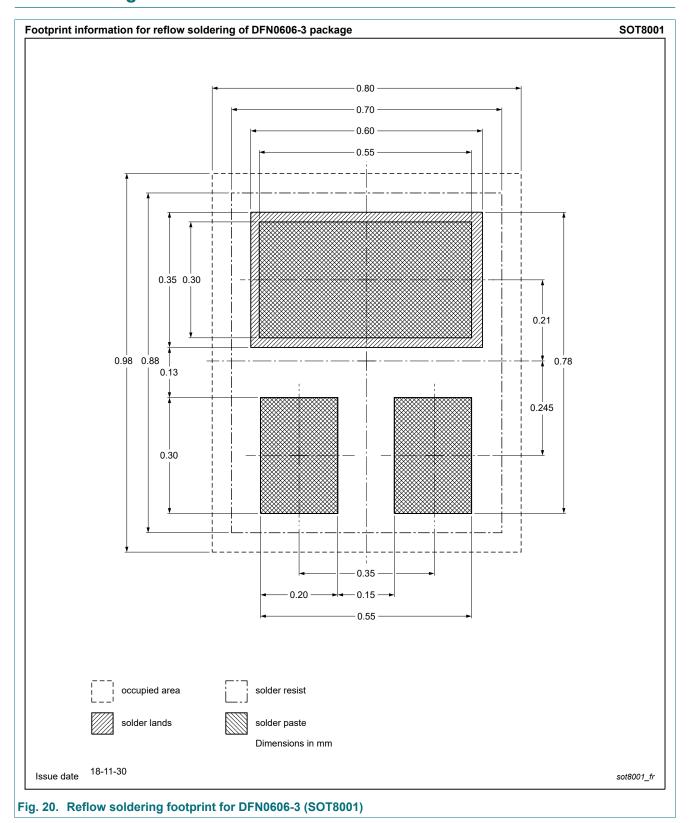
30 V, P-channel Trench MOSFET

12. Package outline



30 V, P-channel Trench MOSFET

13. Soldering



30 V, P-channel Trench MOSFET

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMH850UPE v.1	20200408	Product data sheet	-	-

30 V, P-channel Trench MOSFET

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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30 V, P-channel Trench MOSFET

Contents

General description	. 1
Features and benefits	. 1
Applications	. 1
Quick reference data	1
Pinning information	2
Ordering information	2
Marking	. 2
Limiting values	. 3
Thermal characteristics	. 5
Characteristics	. 6
Test information	. 9
Package outline	10
Soldering	11
Revision history	12
Legal information	
	Features and benefits

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