PMP4501QAS

45 V, 100 mA NPN/NPN matched double transistors

9 February 2018 **Product data sheet**

1. General description

NPN/NPN matched double transistors in an ultra small DFN1010B-6 (SOT1216) leadless Surface-Mounted Device (SMD) plastic package.

PNP/PNP complement: PMP5501QAS

2. Features and benefits

- Reduces component count
- Reduces pick and place costs
- Low package height of 0.37 mm
- Current gain matching
- Base-emitter voltage matching
- Application-optimized pinout
- AEC-Q101 qualified

3. Applications

- Current mirror
- Differential amplifier

4. Quick reference data

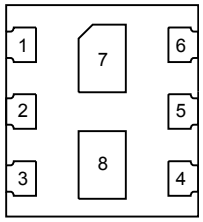
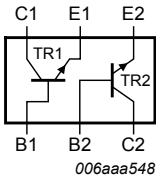
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
V_{CEO}	collector-emitter voltage	open base		-	-	45	V
I_C	collector current			-	-	100	mA
I_{CM}	peak collector current	$t_p \leq$ 1 ms; single pulse		-	-	200	mA
h_{FE}	DC current gain	V_{CE} = 5 V; I_C = 2 mA; T_{amb} = 25 °C		200	290	450	
Per device							
h_{FE1}/h_{FE2}	DC current gain matching	V_{CE} = 5 V; I_C = 2 mA; T_{amb} = 25 °C		0.95	1	1.05	
$V_{BE1}-V_{BE2}$	base-emitter voltage matching		[1]	-	-	2	mV

[1] The smaller of the two values is subtracted from the larger value.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	B1	base TR1	 Transparent top view **DFN1010B-6 (SOT1216)**	
2	B2	base TR2		
3	C2	collector TR2		
4	E2	emitter TR2		
5	E1	emitter TR1		
6	C1	collector TR1		
7	C1	collector TR1		
8	C2	collector TR2		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMP4501QAS	DFN1010B-6	DFN1010B-6: plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals	SOT1216

7. Marking

Table 4. Marking codes

Type number	Marking code
PMP4501QAS	C 100

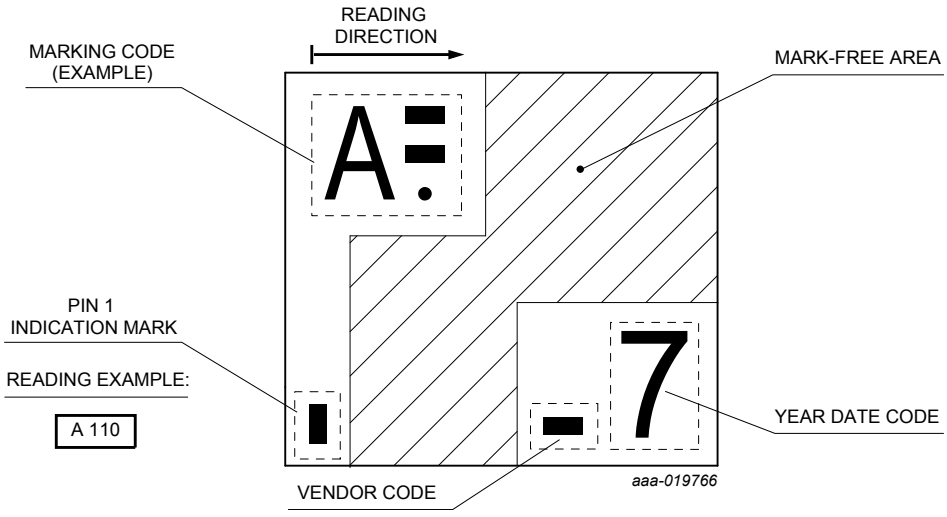


Fig. 1. DFN1010B-6 (SOT1216) binary marking code description

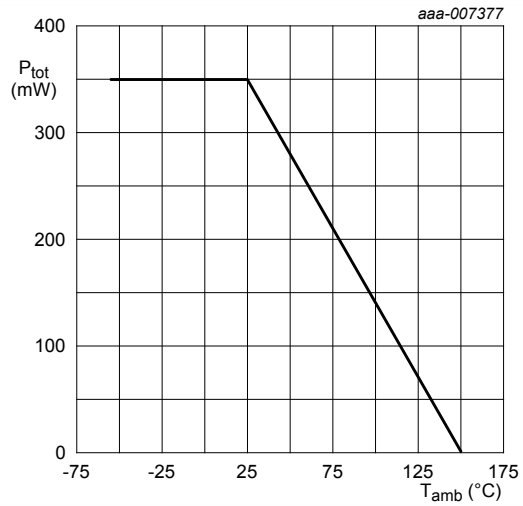
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor						
V_{CBO}	collector-base voltage	open emitter		-	50	V
V_{CEO}	collector-emitter voltage	open base		-	45	V
V_{EBO}	emitter-base voltage	open collector		-	6	V
I_C	collector current			-	100	mA
I_{CM}	peak collector current	$t_p \leq$ 1 ms; single pulse		-	200	mA
I_{BM}	peak base current			-	100	mA
P_{tot}	total power dissipation	$T_{amb} \leq$ 25 °C	[1]	-	230	mW
Per device						
P_{tot}	total power dissipation	$T_{amb} \leq$ 25 °C	[1]	-	350	mW
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.



FR4 PCB, standard footprint

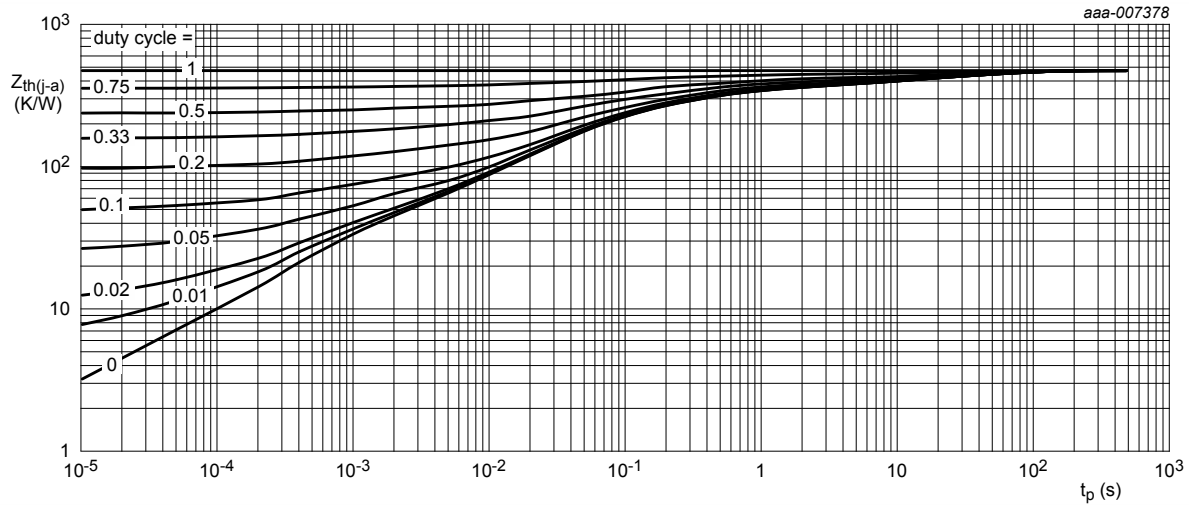
Fig. 2. Per device: Power derating curve

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	544	K/W
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	358	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.



FR4 PCB, standard footprint

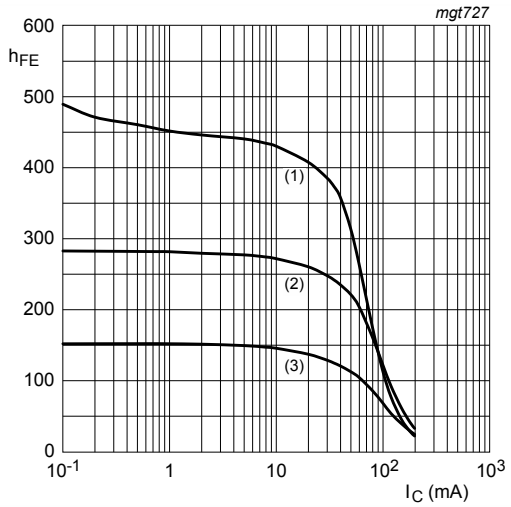
Fig. 3. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

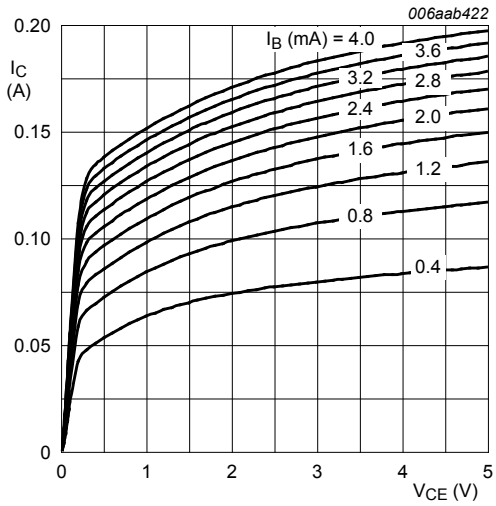
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
$V_{(BR)CBO}$	collector-base breakdown voltage	I_C = 100 µA; I_E = 0 A		50	-	-	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	I_C = 2 mA; I_B = 0 A		45	-	-	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	I_C = 0 A; I_E = 100 µA		6	-	-	V
I_{CBO}	collector-base cut-off current	V_{CB} = 30 V; I_E = 0 A; T_{amb} = 25 °C		-	-	15	nA
		V_{CB} = 30 V; I_E = 0 A; T_j = 150 °C		-	-	5	µA
I_{EBO}	emitter-base cut-off current	V_{EB} = 5 V; I_C = 0 A; T_{amb} = 25 °C		-	-	100	nA
h_{FE}	DC current gain	V_{CE} = 5 V; I_C = 10 µA; T_{amb} = 25 °C		-	250	-	
		V_{CE} = 5 V; I_C = 2 mA; T_{amb} = 25 °C		200	290	450	
V_{CEsat}	collector-emitter saturation voltage	I_C = 10 mA; I_B = 0.5 mA; T_{amb} = 25 °C		-	-	200	mV
		I_C = 100 mA; I_B = 5 mA; T_{amb} = 25 °C	[1]	-	-	400	mV
V_{BEsat}	base-emitter saturation voltage	I_C = 10 mA; I_B = 0.5 mA; T_{amb} = 25 °C	[2]	-	760	-	mV
		I_C = 100 mA; I_B = 5 mA; T_{amb} = 25 °C	[2]	-	900	-	mV
V_{BE}	base-emitter voltage	V_{CE} = 5 V; I_C = 2 mA; T_{amb} = 25 °C	[3]	600	660	725	mV
		V_{CE} = 5 V; I_C = 10 mA; T_{amb} = 25 °C	[3]	-	710	820	mV
C_c	collector capacitance	V_{CB} = 10 V; I_E = 0 A; i_e = 0 A; f = 1 MHz; T_{amb} = 25 °C		-	-	4	pF
C_e	emitter capacitance	V_{EB} = 0.5 V; I_C = 0 A; i_c = 0 A; f = 1 MHz; T_{amb} = 25 °C		-	11	-	pF
f_T	transition frequency	V_{CE} = 5 V; I_C = 10 mA; f = 100 MHz; T_{amb} = 25 °C		100	-	-	MHz
NF	noise figure	V_{CE} = 5 V; I_C = 0.2 mA; R_S = 2 kΩ; f = 1 kHz; B = 200 Hz; T_{amb} = 25 °C		-	-	10	dB
Per device							
h_{FE1}/h_{FE2}	DC current gain matching	V_{CE} = 5 V; I_C = 2 mA; T_{amb} = 25 °C		0.95	1	1.05	
$V_{BE1}-V_{BE2}$	base-emitter voltage matching		[4]	-	-	2	mV

[1] Pulse test: $t_p \leq 300$ µs; $\delta \leq 0.02$
[2] V_{BEsat} decreases by about 1.7 mV/K with increasing temperature.
[3] V_{BE} decreases by about 2 mV/K with increasing temperature.
[4] The smaller of the two values is subtracted from the larger value.



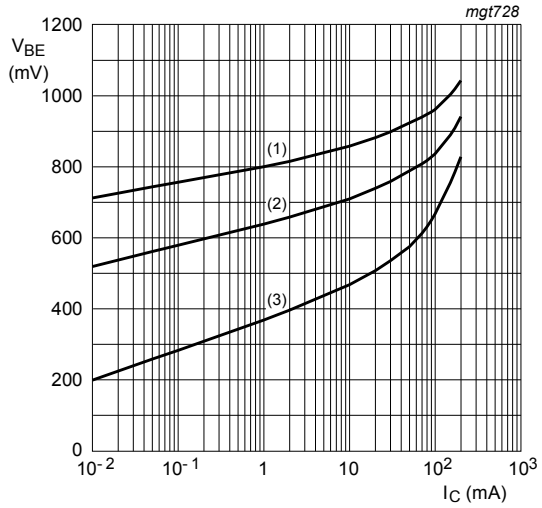
V_{CE} = 5 V
(1) T_{amb} = 150 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = −55 °C

Fig. 4. DC current gain as a function of collector current; typical values



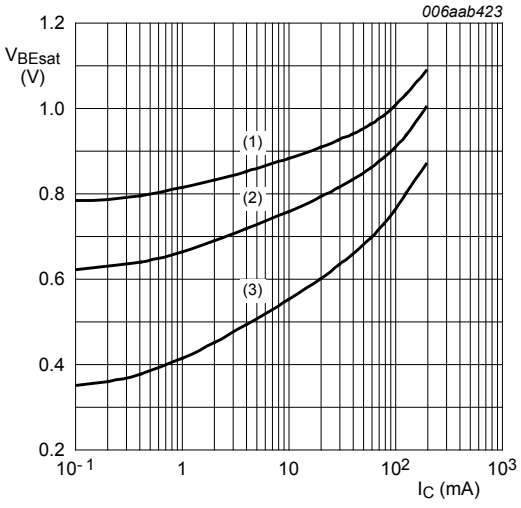
T_{amb} = 25 °C

Fig. 5. Collector current as a function of collector-emitter voltage; typical values



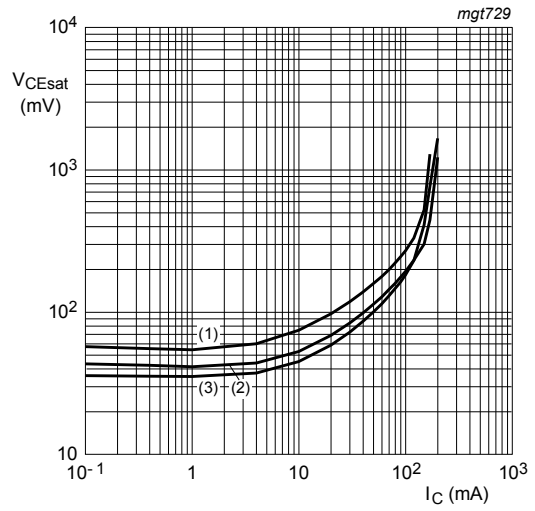
V_{CE} = 5 V
(1) T_{amb} = -55 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 150 °C

Fig. 6. Base-emitter voltage as a function of collector current; typical values



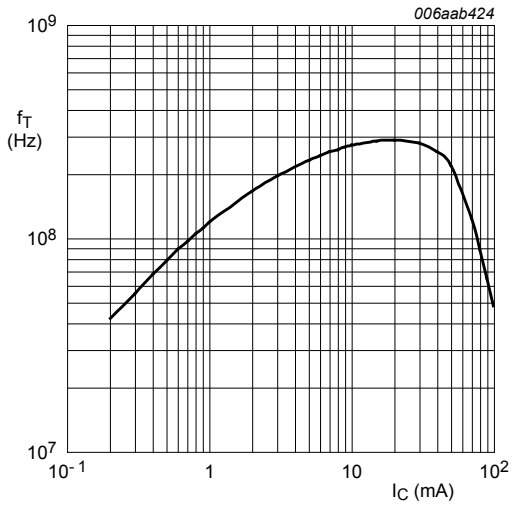
I_C/I_B = 20
(1) T_{amb} = -55 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 150 °C

Fig. 7. Base-emitter saturation voltage as a function of collector current; typical values



I_C/I_B = 20
(1) T_{amb} = 150 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = -55 °C

Fig. 8. Collector-emitter saturation voltage as a function of collector current; typical values



T_{amb} = 25 °C;
V_{CE} = 5 V;
f = 100 MHz

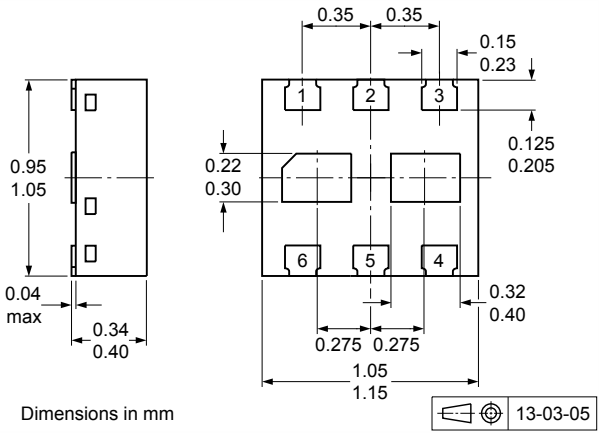
Fig. 9. Transition frequency as a function of collector current; typical values

11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline



Dimensions in mm

Fig. 10. Package outline DFN1010B-6 (SOT1216)

13. Soldering

Footprint information for reflow soldering of DFN1010B-6 package **SOT1216**

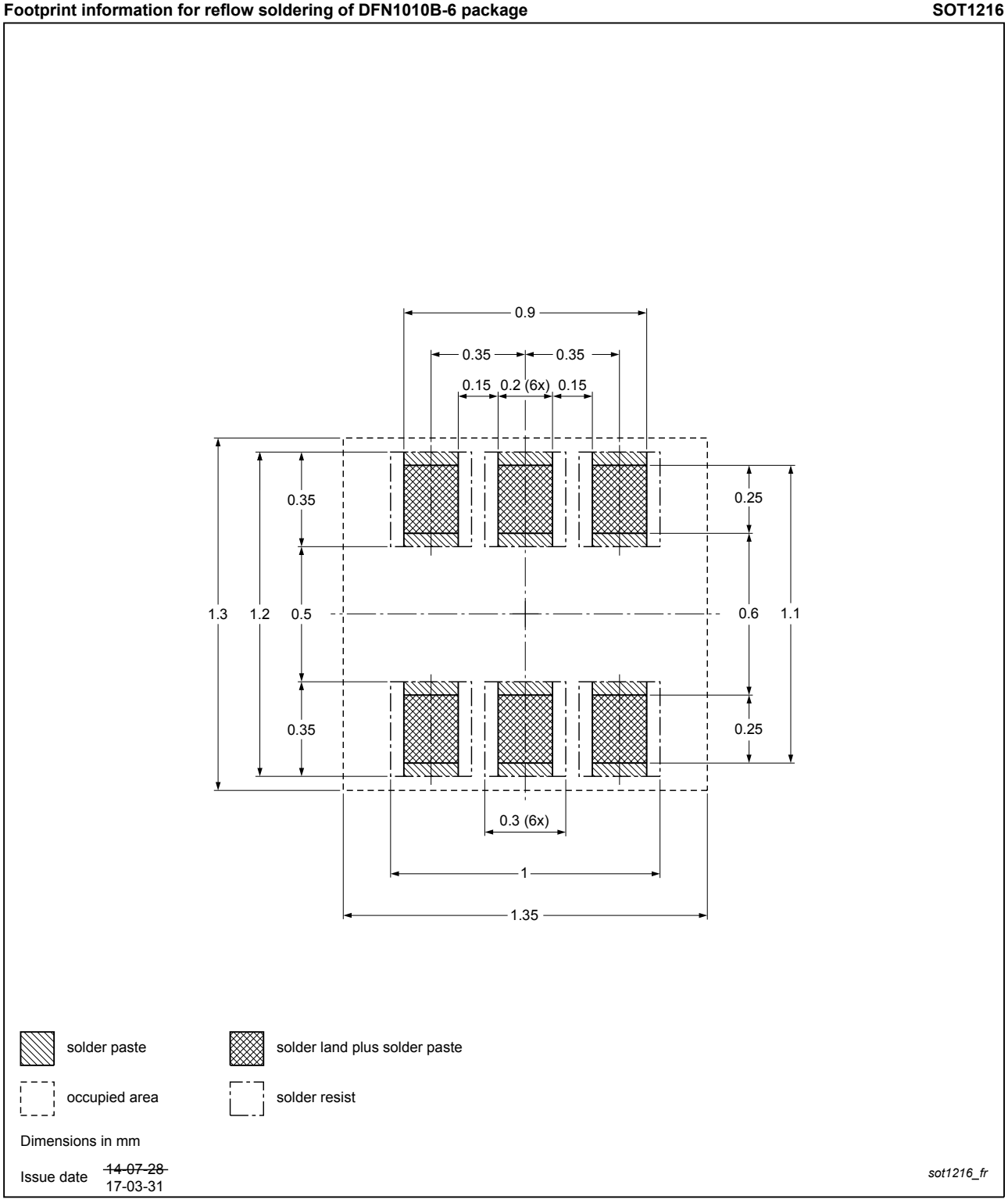


Fig. 11. Reflow soldering footprint for DFN1010B-6 (SOT1216)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMP4501QAS v.1	20180209	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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