Product data sheet

1. General description

P-channel enhancement mode Field-Effect Transistor (FET) in a leadless medium power DFN2020MD-6 (SOT1220) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- · Logic-level compatible
- Trench MOSFET technology
- Side wettable flanks for optical solder inspection
- Small and leadless ultra thin SMD plastic package: 2 x 2 x 0.65 mm
- · Exposed drain pad for excellent thermal conduction

3. Applications

- Charging switch for portable devices
- DC-to-DC converters
- · Power management in battery-driven portable devices
- · Computing power management

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit	
V _{DS}	drain-source voltage	T _j = 25 °C		-	-	-30	V	
V_{GS}	gate-source voltage			-25	-	25	V	
I _D	drain current	V _{GS} = -10 V; T _{amb} = 25 °C; t ≤ 5 s	[1]	-	-	-10.6	Α	
Static characte	Static characteristics							
R _{DSon}	drain-source on-state resistance	V_{GS} = -10 V; I_D = -7.5 A; T_j = 25 °C		-	16	20	mΩ	

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm².



30 V, P-channel Trench MOSFET

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	D	drain	1 1 1 6	D
2	D	drain		
3	G	gate	2 5	G (F)
4	S	source	3 8 4	\$
5	D	drain	Transparent top view	017aaa257
6	D	drain	DFN2020MD-6 (SOT1220)	
7	D	drain		
8	S	source		

6. Ordering information

Table 3. Ordering information

Type number	Package					
	Name	Description	Version			
PMPB16EP		plastic, leadless thermal enhanced ultra thin small outline package; 6 terminals; 0.65 mm pitch; 2 mm x 2 mm x 0.65 mm body	SOT1220			

7. Marking

Table 4. Marking codes

Type number	Marking code
PMPB16EP	5K

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8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	T _j = 25 °C		-	-30	V
V_{GS}	gate-source voltage			-25	25	V
I _D	drain current	V _{GS} = -10 V; T _{amb} = 25 °C; t ≤ 5 s	[1]	-	-10.6	Α
		V _{GS} = -10 V; T _{amb} = 25 °C	[1]	-	-7.5	Α
		V _{GS} = -10 V; T _{amb} = 100 °C	[1]	-	-4.7	А
I _{DM}	peak drain current	T_{amb} = 25 °C; single pulse; $t_p \le 10 \mu s$		-	-30	Α
P _{tot}	total power dissipation	T _{amb} = 25 °C	[1]	-	2	W
		T _{amb} = 25 °C; t ≤ 5 s	[1]	-	4	W
		T _{sp} = 25 °C		-	12.5	W
T _j	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
Source-drain	n diode					•
I _S	source current	T _{amb} = 25 °C	[1]	-	-1.9	А

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm².

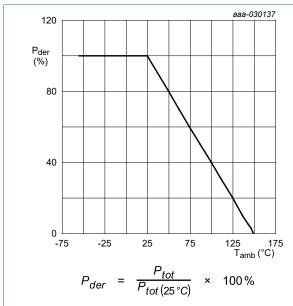


Fig. 1. Normalized total power dissipation as a function of ambient temperature

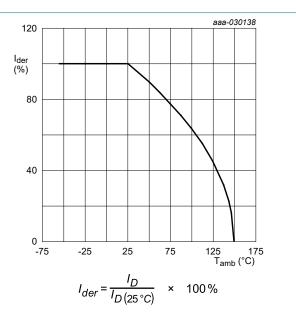


Fig. 2. Normalized continous drain current as a function of ambient temperature

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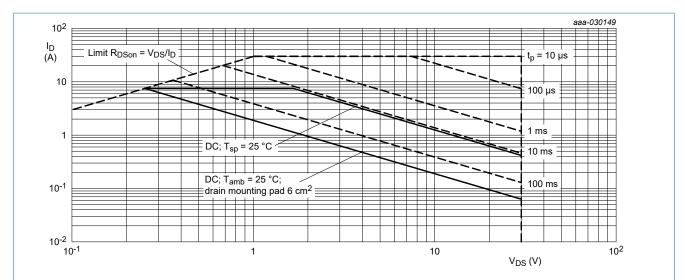


Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

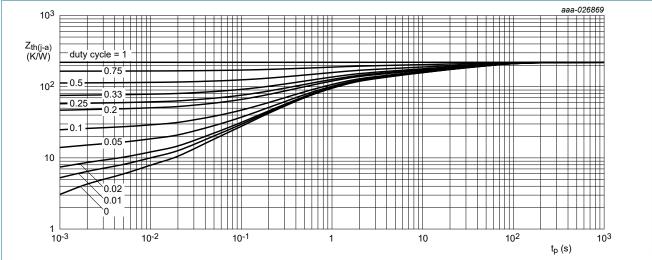
30 V, P-channel Trench MOSFET

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
$R_{th(j-a)}$	thermal resistance from	in free air	[1]	-	223	256	K/W
	junction to ambient		[2]	-	57	66	K/W
		in free air; t ≤ 5 s	[2]	-	29	33	K/W
R _{th(j-sp)}	thermal resistance from junction to solder point			-	5	10	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm².



FR4 PCB, standard footprint

Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

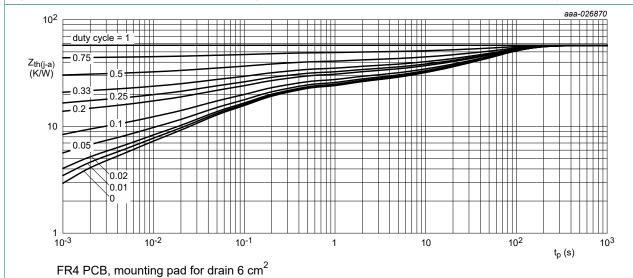


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

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10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics					
V _{(BR)DSS}	drain-source breakdown voltage	$I_D = -250 \mu A; V_{GS} = 0 V; T_j = 25 °C$	-30	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = -250 \mu A; V_{DS} = V_{GS}; T_j = 25 \text{ °C}$	-1	-1.5	-2.5	V
I _{DSS}	drain leakage current	V _{DS} = -30 V; V _{GS} = 0 V; T _j = 25 °C	-	-	-1	μΑ
I _{GSS} gate leakage current	gate leakage current	V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C	-	-	-100	nA
		V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C	-	-	100	nΑ
R _{DSon}	drain-source on-state	$V_{GS} = -10 \text{ V}; I_D = -7.5 \text{ A}; T_j = 25 \text{ °C}$	-	16	20	mΩ
	resistance	V _{GS} = -10 V; I _D = -7.5 A; T _j = 150 °C	-	27	34	mΩ
		$V_{GS} = -5 \text{ V}; I_D = -6.3 \text{ A}; T_j = 25 \text{ °C}$	-	21	28	mΩ
		$V_{GS} = -4.5 \text{ V}; I_D = -6.2 \text{ A}; T_j = 25 \text{ °C}$	-	22	29	mΩ
9 _{fs}	forward transconductance	$V_{DS} = -10 \text{ V}; I_D = -8 \text{ A}; T_j = 25 \text{ °C}$	-	33	-	S
R_{G}	gate resistance	f = 1 MHz	-	8.7	-	Ω
Dynamic ch	aracteristics					
Q _{G(tot)}	total gate charge	$V_{DS} = -15 \text{ V}; I_D = -8 \text{ A}; V_{GS} = -10 \text{ V};$	-	29	44	nC
Q _{GS}	gate-source charge	T _j = 25 °C	-	3.7	-	nC
Q_{GD}	gate-drain charge		-	6.2	-	nC
C _{iss}	input capacitance	V _{DS} = -15 V; f = 1 MHz; V _{GS} = 0 V;	-	1418	-	pF
C _{oss}	output capacitance	T _j = 25 °C	-	159	-	pF
C _{rss}	reverse transfer capacitance		-	139	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = -15 V; I _D = -7.5 A; V _{GS} = -10 V;	-	3	-	ns
t _r	rise time	$R_{G(ext)} = 6 \Omega; T_j = 25 °C$	-	7	-	ns
t _{d(off)}	turn-off delay time	1	-	60	-	ns
t _f	fall time	1	-	25	-	ns
Source-drai	in diode				<u> </u>	
V_{SD}	source-drain voltage	$I_S = -1.9 \text{ A}; V_{GS} = 0 \text{ V}; T_i = 25 ^{\circ}\text{C}$	-	-0.8	-1.2	V

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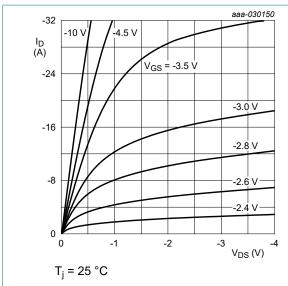


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

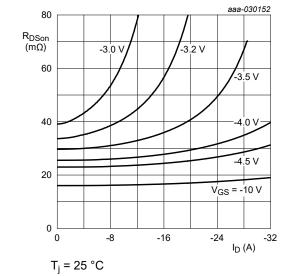


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

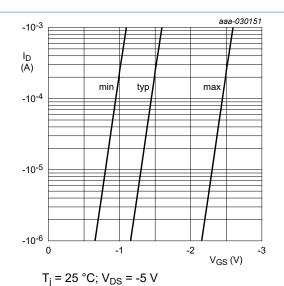


Fig. 7. Subthreshold drain current as a function of gate-source voltage

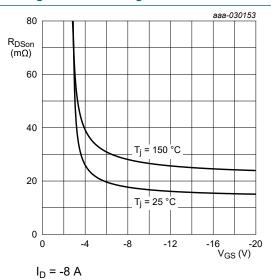


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

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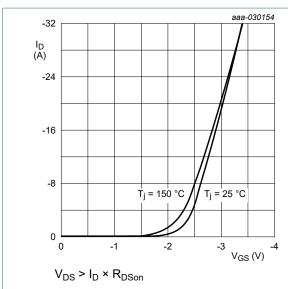


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

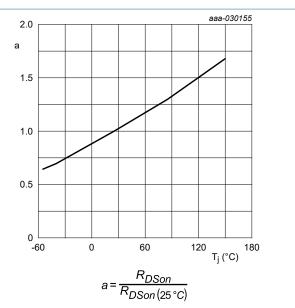


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

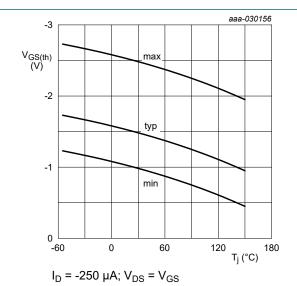
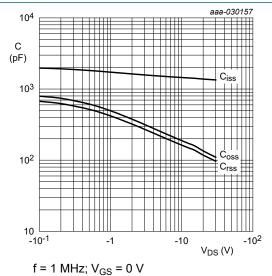


Fig. 12. Gate-source threshold voltage as a function of junction temperature



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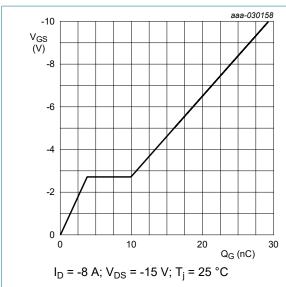


Fig. 14. Gate-source voltage as a function of gate charge; typical values

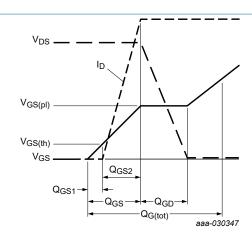


Fig. 15. Gate charge waveform definitions

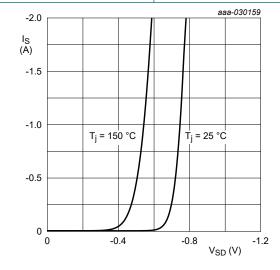
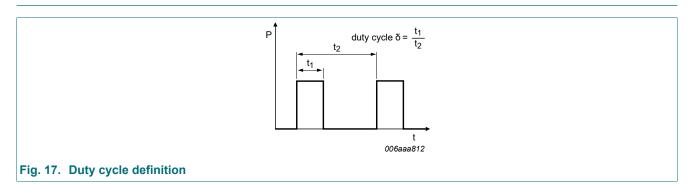


Fig. 16. Source current as a function of source-drain voltage; typical values

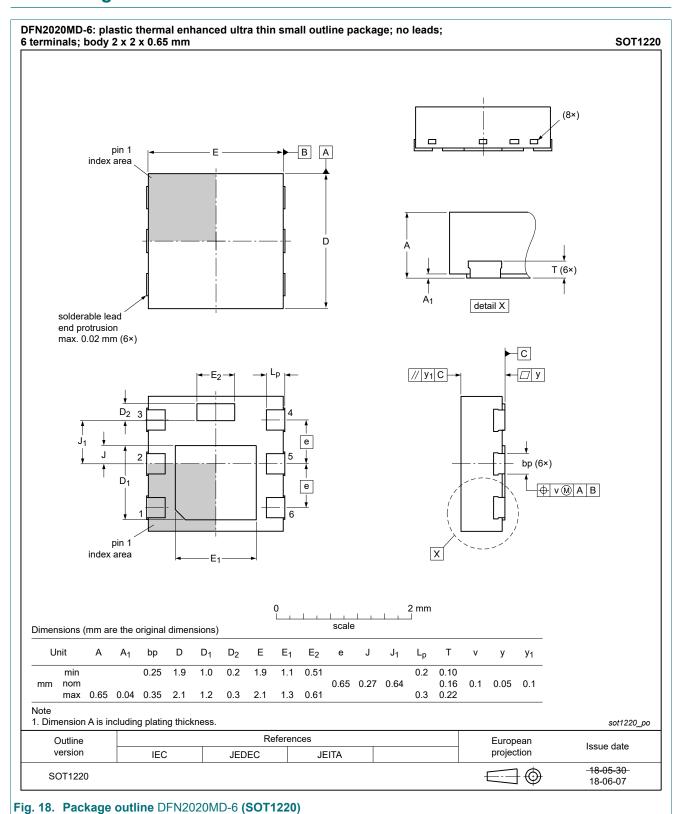
11. Test information

 $V_{GS} = 0 V$



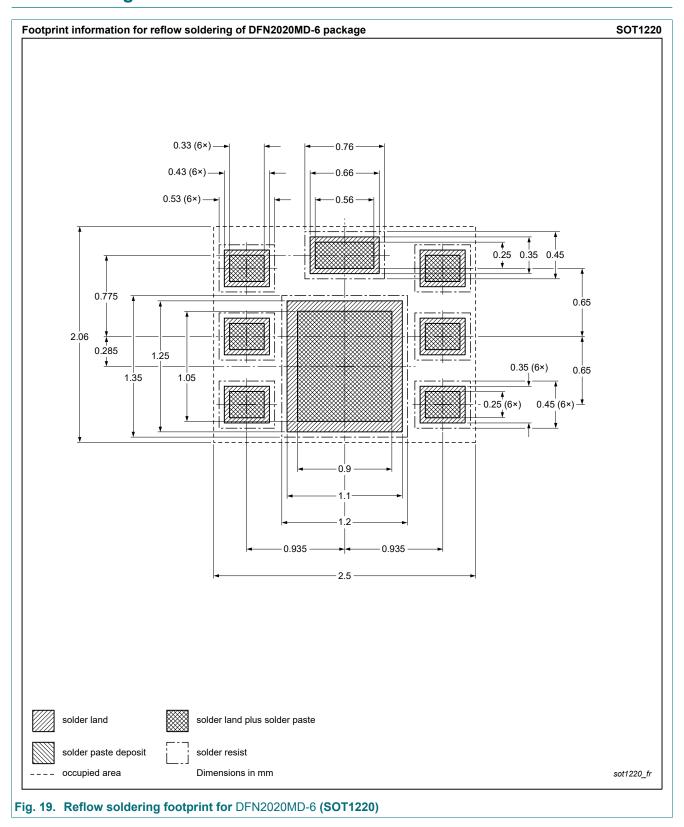
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12. Package outline



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13. Soldering



30 V, P-channel Trench MOSFET

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMPB16EP v.1	20190924	Product data sheet	-	-

30 V, P-channel Trench MOSFET

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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