



# PMPB19XP

20 V, single P-channel Trench MOSFET

20 September 2012

Product data sheet

## 1. Product profile

### 1.1 General description

P-channel enhancement mode Field-Effect Transistor (FET) in a leadless medium power DFN2020MD-6 (SOT1220) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

### 1.2 Features and benefits

- Trench MOSFET technology
- Small and leadless ultra thin SMD plastic package: 2 x 2 x 0.65 mm
- Exposed drain pad for excellent thermal conduction
- Tin-plated 100 % solderable side pads for optical solder inspection

### 1.3 Applications

- Charging switch for portable devices
- DC-to-DC converters
- Power management in battery-driven portable devices
- Hard disk and computing power management

### 1.4 Quick reference data

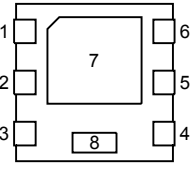
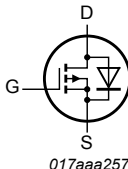
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j = 25\text{ °C}$	-	-	-20	V
$V_{GS}$	gate-source voltage		-12	-	12	V
$I_D$	drain current	$V_{GS} = -4.5\text{ V}; T_{amb} = 25\text{ °C}; t \leq 5\text{ s}$	[1]	-	-10.3	A
<b>Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = -4.5\text{ V}; I_D = -7.2\text{ A}; T_j = 25\text{ °C}$	-	19	22.5	m $\Omega$

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm<sup>2</sup>.

## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	D	drain	 <p>Transparent top view <b>DFN2020MD-6 (SOT1220)</b></p>	 <p>017aaa257</p>
2	D	drain		
3	G	gate		
4	S	source		
5	D	drain		
6	D	drain		
7	D	drain		
8	S	source		

## 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMPB19XP	DFN2020MD-6	plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals	SOT1220

## 4. Marking

Table 4. Marking codes

Type number	Marking code
PMPB19XP	1R

## 5. Limiting values

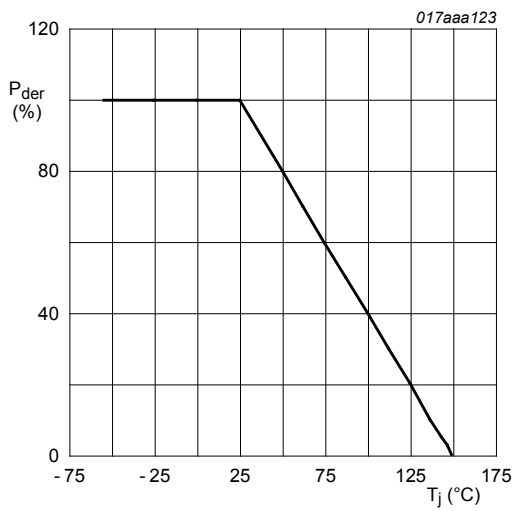
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j = 25\text{ °C}$		-	-20	V
$V_{GS}$	gate-source voltage			-12	12	V
$I_D$	drain current	$V_{GS} = -4.5\text{ V}; T_{amb} = 25\text{ °C}; t \leq 5\text{ s}$	[1]	-	-10.3	A
		$V_{GS} = -4.5\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	-7.2	A
		$V_{GS} = -4.5\text{ V}; T_{amb} = 100\text{ °C}$	[1]	-	-4.5	A
$I_{DM}$	peak drain current	$T_{amb} = 25\text{ °C};$ single pulse; $t_p \leq 10\text{ }\mu\text{s}$		-	-30	A
$P_{tot}$	total power dissipation	$T_{amb} = 25\text{ °C}$	[1]	-	1.7	W

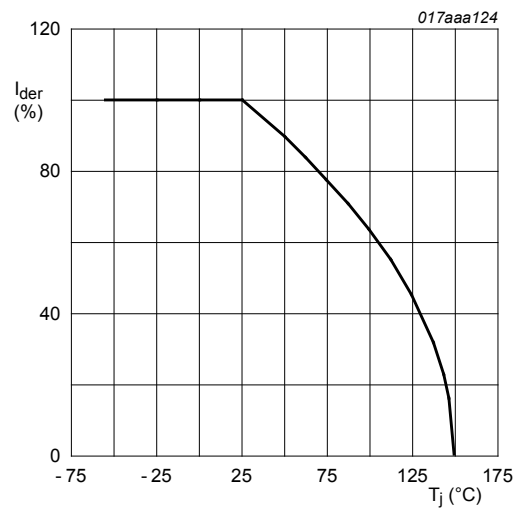
Symbol	Parameter	Conditions		Min	Max	Unit
		$T_{amb} = 25\text{ °C}; t \leq 5\text{ s}$	[1]	-	3.5	W
		$T_{sp} = 25\text{ °C}$		-	12.5	W
$T_j$	junction temperature			-55	150	°C
$T_{amb}$	ambient temperature			-55	150	°C
$T_{stg}$	storage temperature			-65	150	°C
<b>Source-drain diode</b>						
$I_S$	source current	$T_{amb} = 25\text{ °C}$	[1]	-	-1.9	A

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm<sup>2</sup>.



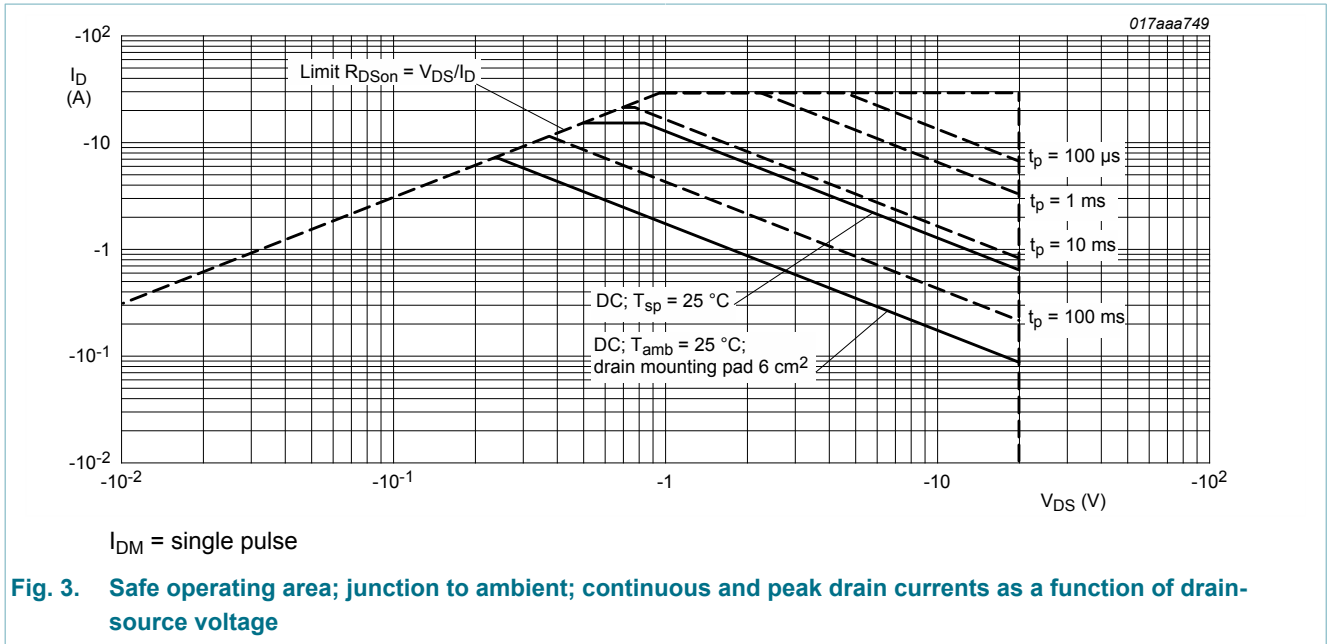
**Fig. 1. Normalized total power dissipation as a function of junction temperature**

$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$



**Fig. 2. Normalized continuous drain current as a function of junction temperature**

$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100\%$$



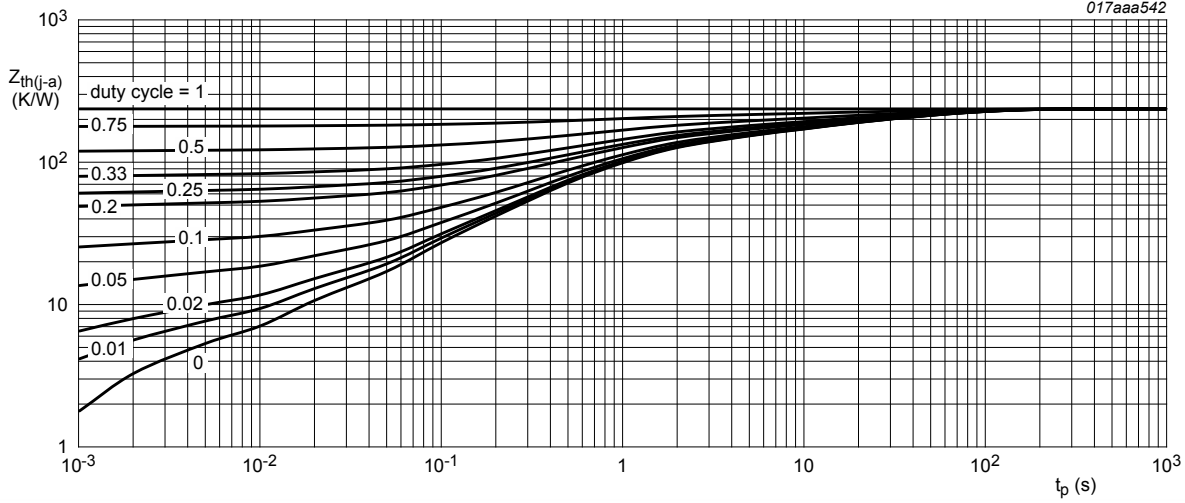
## 6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	235	270	K/W
			[2]	-	67	74	K/W
		in free air; $t \leq 5\text{ s}$	[2]	-	33	36	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	5	10	K/W

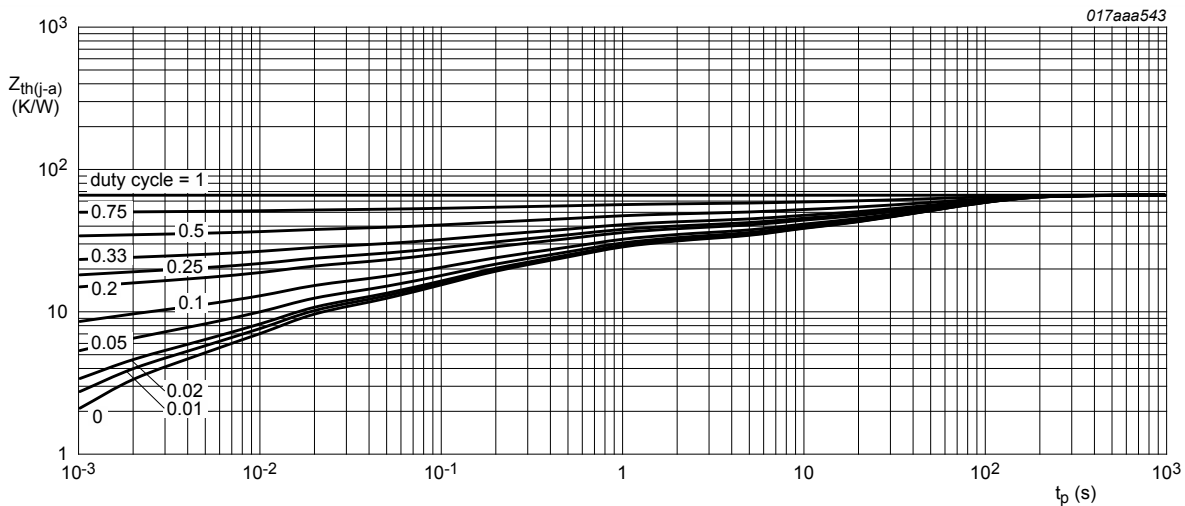
[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain  $6\text{ cm}^2$ .



FR4 PCB, standard footprint

Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, mounting pad for drain 6 cm<sup>2</sup>

Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

## 7. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-20	-	-	V
$V_{GSth}$	gate-source threshold voltage	$I_D = -250 \mu A; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$	-0.47	-0.68	-0.9	V
$I_{DSS}$	drain leakage current	$V_{DS} = -20 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	-1	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = -12 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	-100	nA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		$V_{GS} = 12\text{ V}; V_{DS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C}$	-	-	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = -4.5\text{ V}; I_D = -7.2\text{ A}; T_j = 25\text{ }^\circ\text{C}$	-	19	22.5	m $\Omega$
		$V_{GS} = -4.5\text{ V}; I_D = -7.2\text{ A}; T_j = 150\text{ }^\circ\text{C}$	-	27	33	m $\Omega$
		$V_{GS} = -2.5\text{ V}; I_D = -6.6\text{ A}; T_j = 25\text{ }^\circ\text{C}$	-	21	27	m $\Omega$
		$V_{GS} = -1.8\text{ V}; I_D = -3.9\text{ A}; T_j = 25\text{ }^\circ\text{C}$	-	27	38	m $\Omega$
$g_{fs}$	forward transconductance	$V_{DS} = -10\text{ V}; I_D = -7.2\text{ A}; T_j = 25\text{ }^\circ\text{C}$	-	50	-	S
$R_G$	gate resistance	$f = 1\text{ MHz}$	-	3.9	-	$\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$V_{DS} = -10\text{ V}; I_D = -7.2\text{ A}; V_{GS} = -4.5\text{ V}; T_j = 25\text{ }^\circ\text{C}$	-	28.8	43.2	nC
$Q_{GS}$	gate-source charge		-	4	-	nC
$Q_{GD}$	gate-drain charge		-	5.8	-	nC
$C_{iss}$	input capacitance	$V_{DS} = -10\text{ V}; f = 1\text{ MHz}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C}$	-	2890	-	pF
$C_{oss}$	output capacitance		-	250	-	pF
$C_{rss}$	reverse transfer capacitance		-	225	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = -10\text{ V}; I_D = -7.2\text{ A}; V_{GS} = -4.5\text{ V}; R_{G(ext)} = 6\text{ }^\circ\Omega; T_j = 25\text{ }^\circ\text{C}$	-	16	-	ns
$t_r$	rise time		-	54	-	ns
$t_{d(off)}$	turn-off delay time		-	43	-	ns
$t_f$	fall time		-	36	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = -1.9\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C}$	-	-0.6	-1.2	V

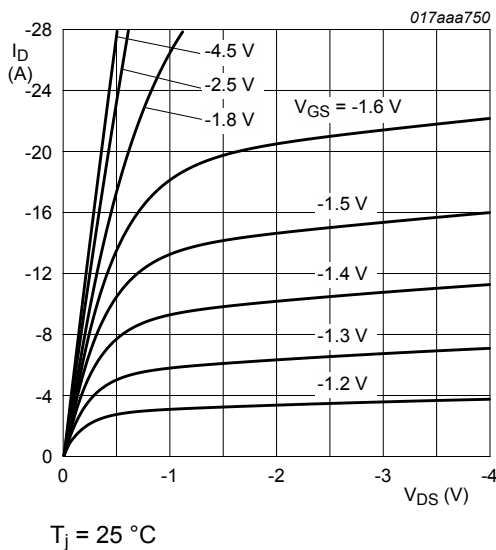


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

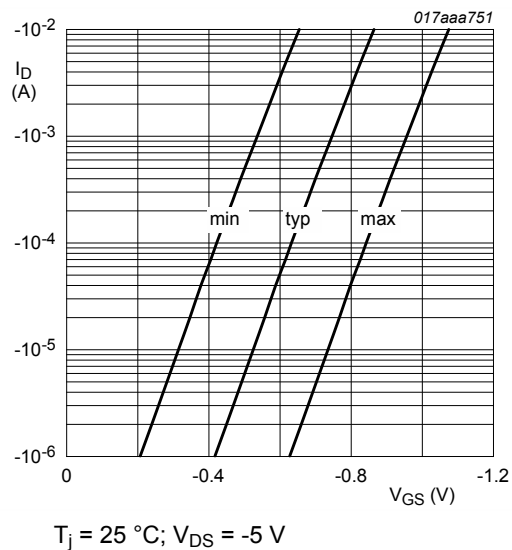
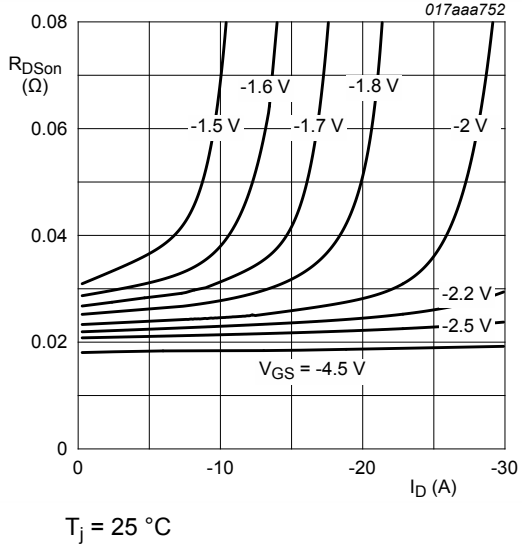
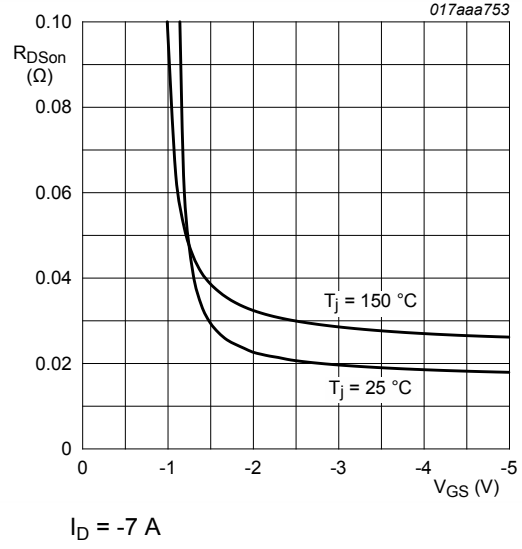


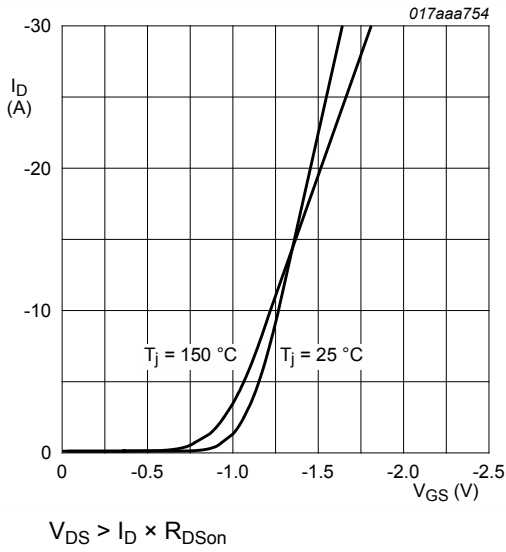
Fig. 7. Sub-threshold drain current as a function of gate-source voltage



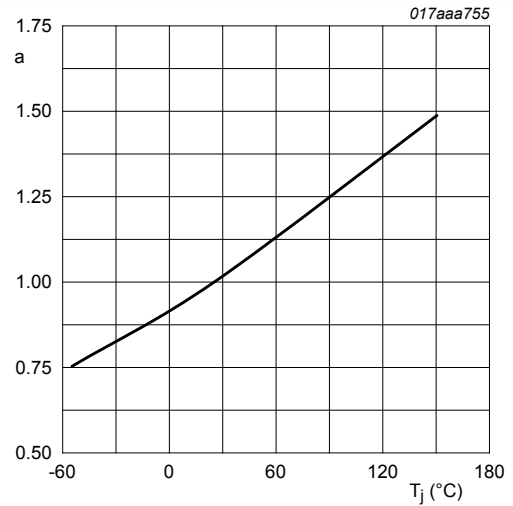
**Fig. 8. Drain-source on-state resistance as a function of drain current; typical values**



**Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values**

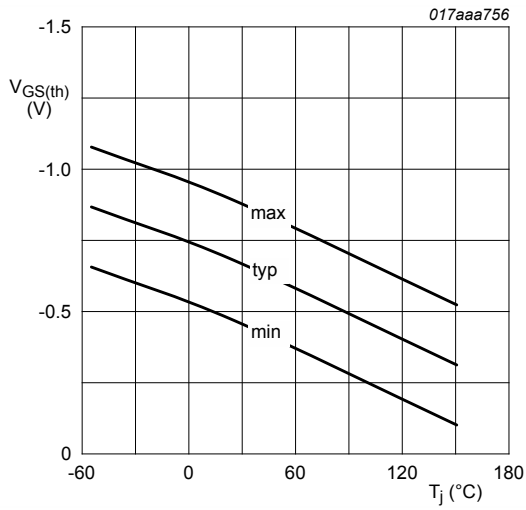


**Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values**



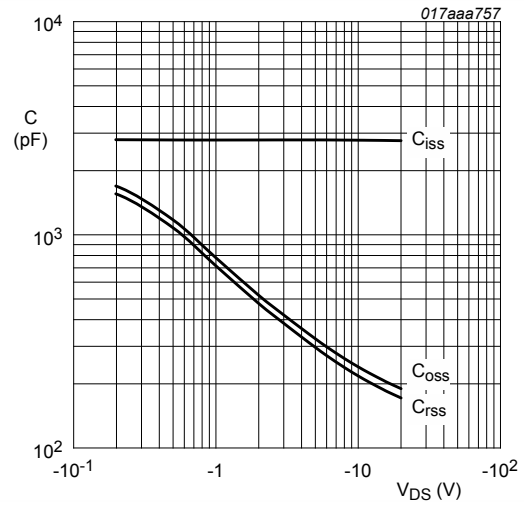
**Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values**

$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$



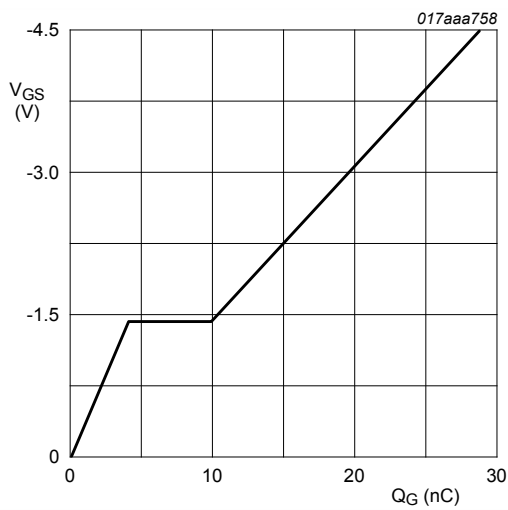
$I_D = -0.25 \text{ mA}; V_{DS} = V_{GS}$

**Fig. 12. Gate-source threshold voltage as a function of junction temperature**



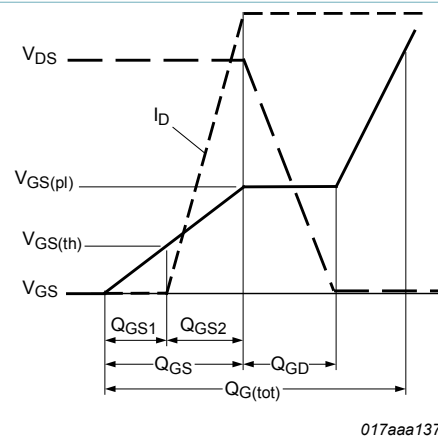
$f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}$

**Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



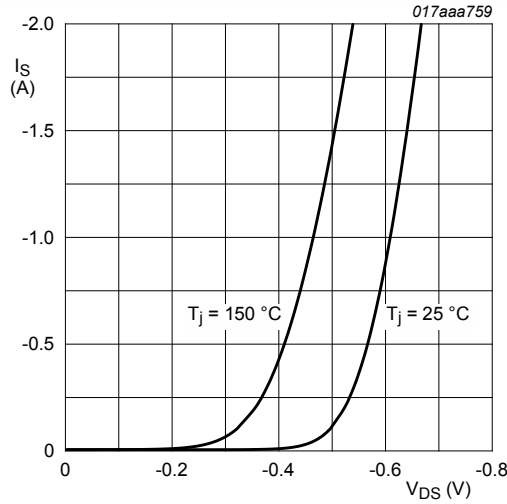
$I_D = -7.2 \text{ A}; V_{DS} = -10 \text{ V}; T_{amb} = 25 \text{ °C}$

**Fig. 14. Gate-source voltage as a function of gate charge; typical values**



**Fig. 15. Gate charge waveform definitions**





$V_{GS} = 0\text{ V}$

Fig. 16. Source current as a function of source-drain voltage; typical values

## 8. Test information

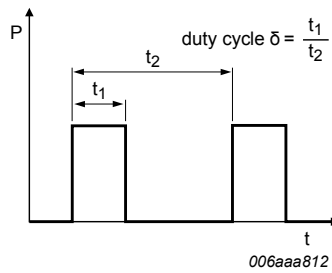


Fig. 17. Duty cycle definition

## 9. Package outline

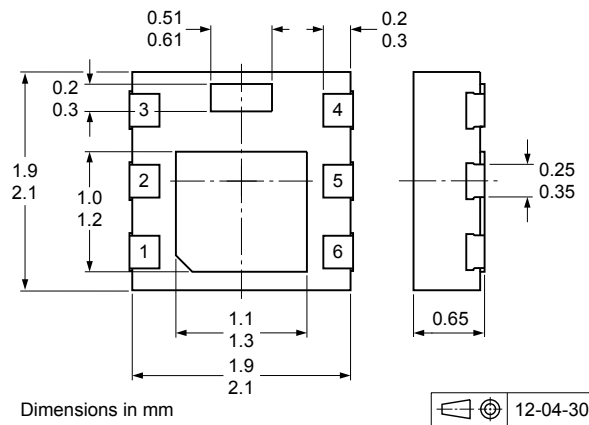


Fig. 18. Package outline DFN2020MD-6 (SOT1220)

### 10. Soldering

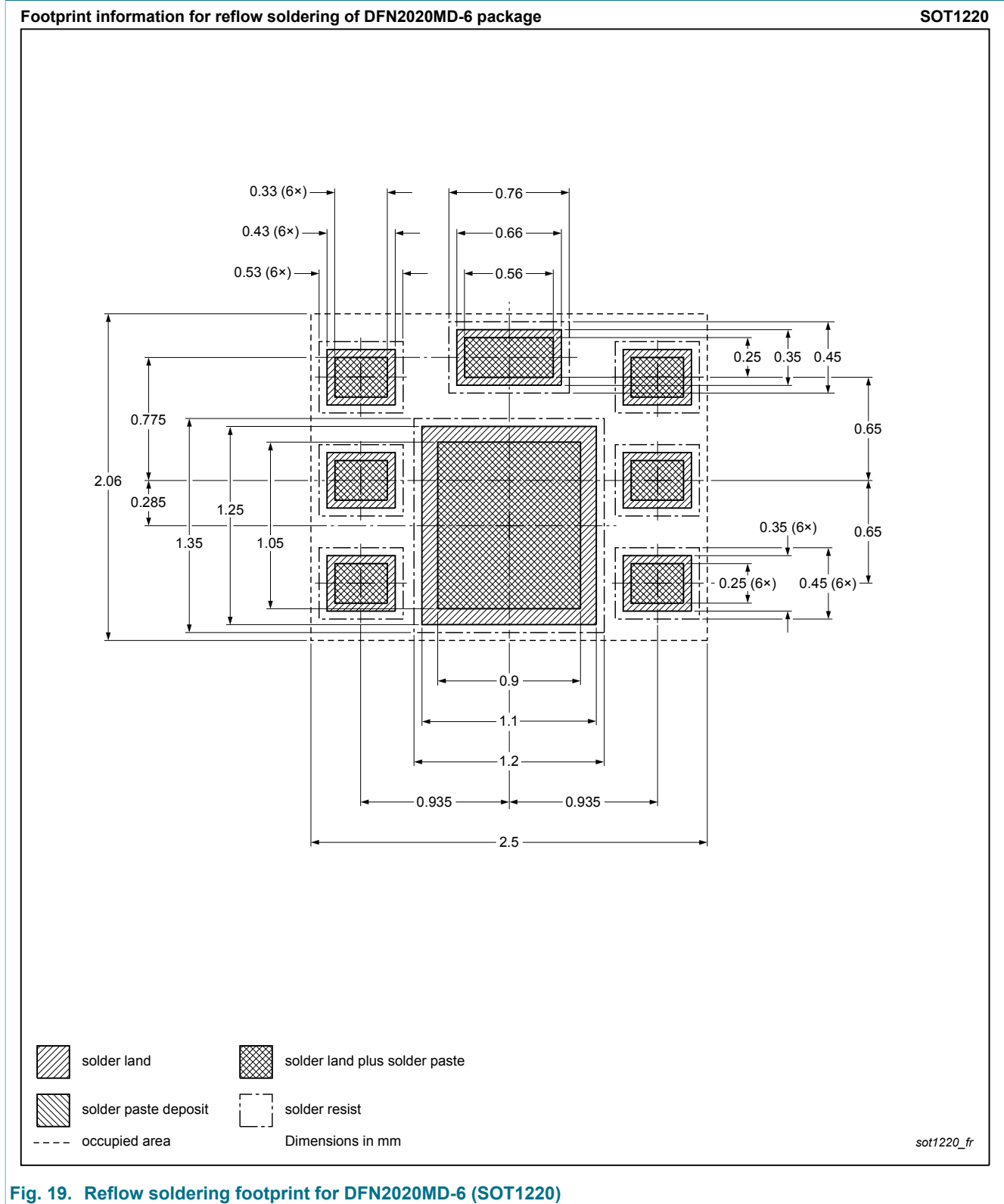


Fig. 19. Reflow soldering footprint for DFN2020MD-6 (SOT1220)

## 11. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMPB19XP v.1	20120920	Product data sheet	-	-

## 12. Legal information

### 12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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