Product data sheet

1. General description

N-channel enhancement mode Field-Effect Transistor (FET) in a medium power SOT223 (SC-73) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Logic level compatible
- Very fast switching
- Trench MOSFET technology
- ElectroStatic Discharge (ESD) protection > 2 kV HBM
- AEC-Q101 qualified

3. Applications

- Relay driver
- High-speed line driver
- Low-side loadswitch
- Switching circuits

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V_{DS}	drain-source voltage	T _j = 25 °C		-	-	100	V
V_{GS}	gate-source voltage			-20	-	20	V
I _D	drain current	V _{GS} = 10 V; T _{amb} = 25 °C	[1]	-	-	1.1	Α
Static characte	Static characteristics						
R _{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 1.1 \text{ A}; T_j = 25 ^{\circ}\text{C}$		-	527	715	mΩ

^[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm².



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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	4	D I
2	D	drain		
3	S	source		$G \left(\begin{array}{c} \downarrow \\ \downarrow \downarrow \end{array} \right)$
4	D	drain	⊟1 ⊟2 ⊟3 SC-73 (SOT223)	S 017aaa255

6. Ordering information

Table 3. Ordering information

Type number	Package				
	Name	Description	Version		
PMT560ENEA	SC-73	plastic surface-mounted package with increased heatsink; 4 leads	SOT223		

7. Marking

Table 4. Marking codes

Type number	Marking code
PMT560ENEA	56ENEA

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8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit		
V_{DS}	drain-source voltage	T _j = 25 °C		-	100	V		
V_{GS}	gate-source voltage			-20	20	V		
I _D	drain current	V _{GS} = 10 V; T _{amb} = 25 °C	[1]	-	1.1	Α		
		V _{GS} = 10 V; T _{amb} = 100 °C	[1]	-	0.7	Α		
I _{DM}	peak drain current	T_{amb} = 25 °C; single pulse; $t_p \le 10 \mu s$		-	4.4	Α		
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	$T_{j(init)}$ = 25 °C; I_D = 0.1 A; DUT in avalanche (unclamped)		-	5.3	mJ		
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	750	mW		
			[1]	-	1.9	W		
		T _{sp} = 25 °C		-	6.25	W		
T _j	junction temperature			-55	150	°C		
T _{amb}	ambient temperature			-55	150	°C		
T _{stg}	storage temperature			-65	150	°C		
Source-drain	n diode							
I _S	source current	T _{amb} = 25 °C	[1]	-	1.1	Α		
ESD maximu	ESD maximum rating							
V _{ESD}	electrostatic discharge voltage	НВМ	[3]	-	2000	V		

^[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm².

^[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

^[3] Measured between all pins.

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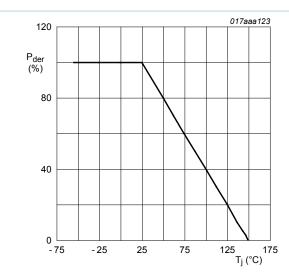


Fig. 1. Normalized total power dissipation as a function of junction temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100 \%$$

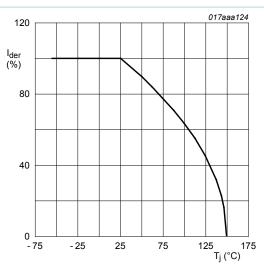


Fig. 2. Normalized continuous drain current as a function of junction temperature

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100 \%$$

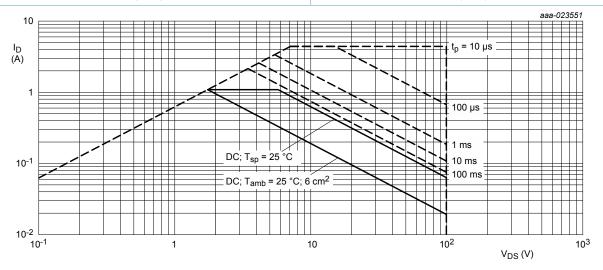


Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drainsource voltage

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9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1]	-	145	167	K/W
			[2]	-	57	66	K/W
R _{th(j-sp)}	thermal resistance from junction to solder point			-	13	20	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm².

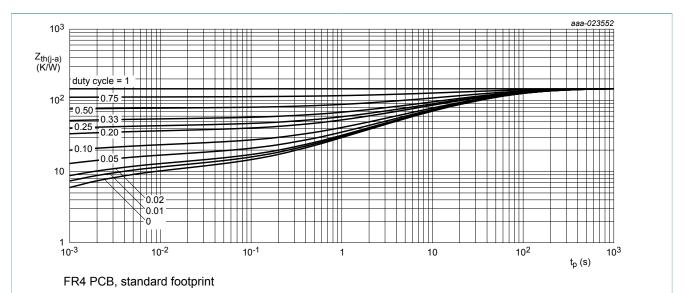


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

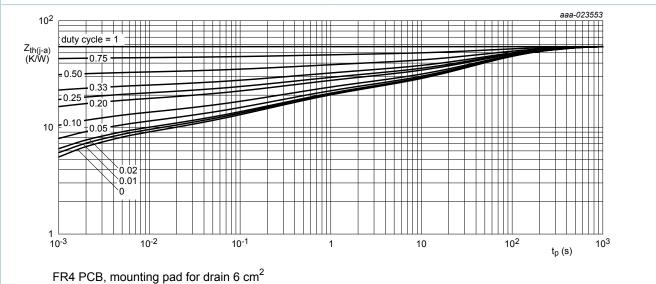


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

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PMT560ENEA

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10. Characteristics

Table 7 Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics		l l			
V _{(BR)DSS}	drain-source breakdown voltage	$I_D = 250 \ \mu\text{A}; \ V_{GS} = 0 \ V; \ T_j = 25 \ ^{\circ}\text{C}$	100	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = 250 \ \mu A; \ V_{DS} = V_{GS}; \ T_j = 25 \ ^{\circ}C$	1.3	1.7	2.7	V
I _{DSS}	drain leakage current	V _{DS} = 100 V; V _{GS} = 0 V; T _j = 25 °C	-	-	1	μA
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C	-	-	15	μA
		V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C	-	-	-15	μA
		V _{GS} = 10 V; V _{DS} = 0 V; T _j = 25 °C	-	-	1	μA
		V _{GS} = -10 V; V _{DS} = 0 V; T _j = 25 °C	-	-	-1	μA
R _{DSon}	drain-source on-state	V _{GS} = 10 V; I _D = 1.1 A; T _j = 25 °C	-	527	715	mΩ
	resistance	V _{GS} = 10 V; I _D = 1.1 A; T _j = 150 °C	-	1.19	1.62	Ω
		V_{GS} = 4.5 V; I_D = 1 A; T_j = 25 °C	-	555	805	mΩ
9fs	forward transconductance	V_{DS} = 10 V; I_{D} = 1.1 A; T_{j} = 25 °C	-	3.5	-	S
R _G	gate resistance	f = 1 MHz	-	7.6	-	Ω
Dynamic ch	naracteristics				'	,
Q _{G(tot)}	total gate charge	V _{DS} = 50 V; I _D = 1.1 A; V _{GS} = 10 V;	-	2.9	4.4	nC
Q_{GS}	gate-source charge	T _j = 25 °C	-	0.3	-	nC
Q_{GD}	gate-drain charge		-	0.7	-	nC
C _{iss}	input capacitance	V _{DS} = 50 V; f = 1 MHz; V _{GS} = 0 V;	-	112	-	pF
C _{oss}	output capacitance	T _j = 25 °C	-	9	-	pF
C _{rss}	reverse transfer capacitance		-	7	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = 50 V; I _D = 1.1 A; V _{GS} = 10 V;	-	6	-	ns
t _r	rise time	$R_{G(ext)} = 6 \Omega; T_j = 25 °C$	-	8	-	ns
t _{d(off)}	turn-off delay time		-	10	-	ns
t _f	fall time		-	5	-	ns
Source-dra	in diode		'			-
V_{SD}	source-drain voltage	$I_S = 1.1 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C}$	-	0.9	1.2	V

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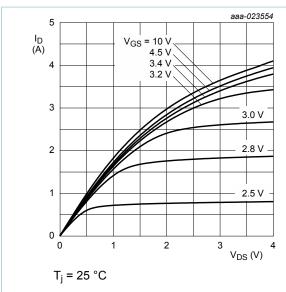


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

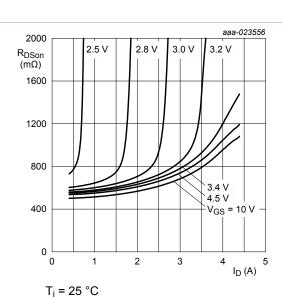


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

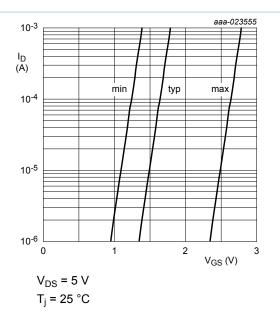


Fig. 7. Subthreshold drain current as a function of gate-source voltage

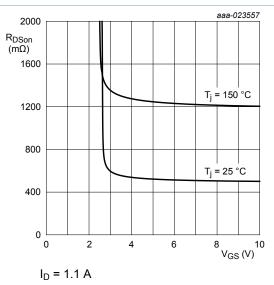


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

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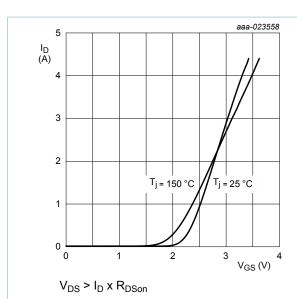


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

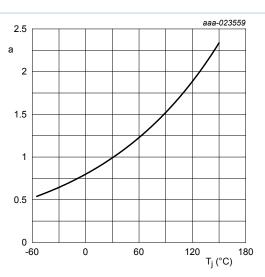


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

$$a = \frac{R_{DSon}}{R_{DSon(25\,^{\circ}C)}}$$

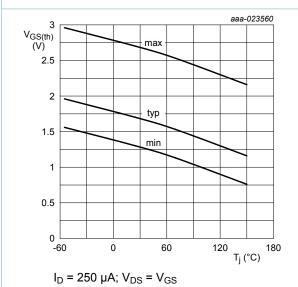
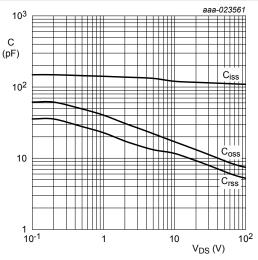


Fig. 12. Gate-source threshold voltage as a function of junction temperature



 $f = 1 MHz; V_{GS} = 0 V$

Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

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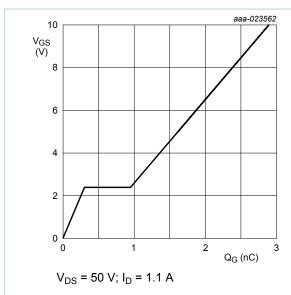


Fig. 14. Gate-source voltage as a function of gate charge; typical values

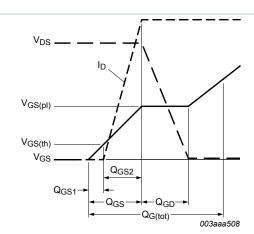


Fig. 15. Gate charge waveform definitions

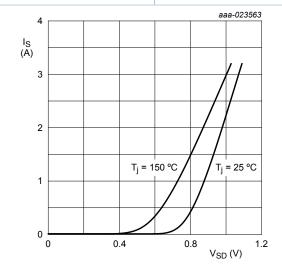
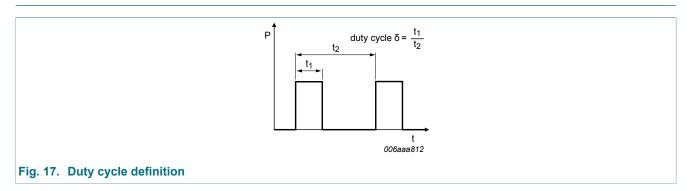


Fig. 16. Source current as a function of source-drain voltage; typical values

 $V_{GS} = 0 V$

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11. Test information

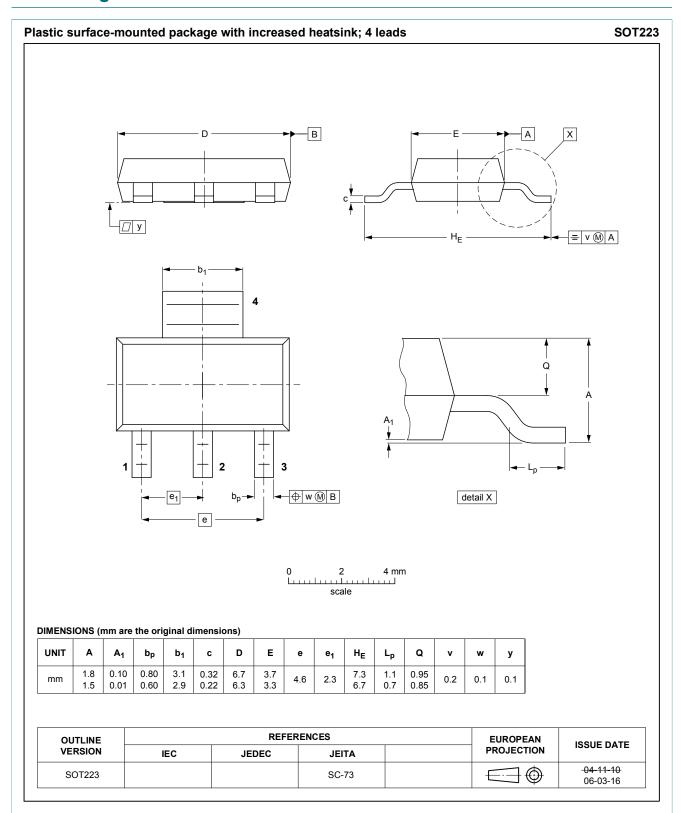


11.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

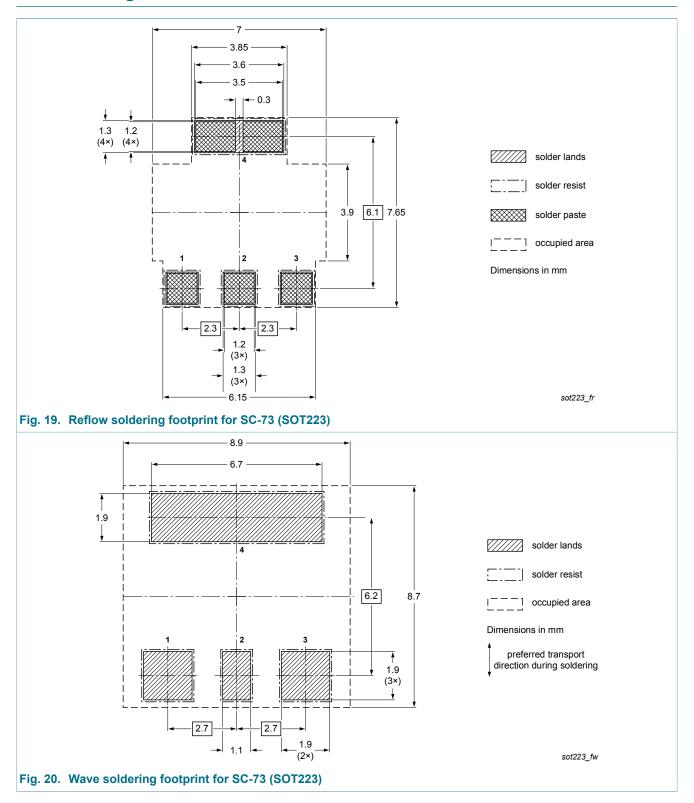
100 V N-channel Trench MOSFET

12. Package outline



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13. Soldering



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14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMT560ENEA v.1	20160714	Product data sheet	-	-

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15. Legal information

15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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