PMV213SN

N-channel TrenchMOS standard level FET

23 November 2020 **Product data sheet**

1. General description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS technology.

2. Features and benefits

- Low on-state resistance in a small surface mount package

3. Applications

- DC-to-DC primary side switching

4. Quick reference data

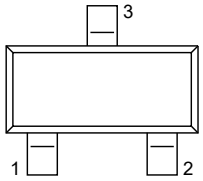
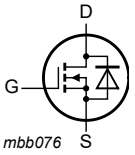
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	25 °C < T_j < 150 °C		-	-	100	V
V_{GS}	gate-source voltage	T_j = 25 °C		-30	-	30	V
I_D	drain current	V_{GS} = 10 V; T_{sp} = 25 °C		-	-	1.9	A
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 0.5 A; T_j = 25 °C		-	213	250	mΩ
P_{tot}	total power dissipation	T_{sp} = 25 °C		-	-	2	W

nexperia

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 SOT23	
2	S	source		
3	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMV213SN	SOT23	plastic, surface-mounted package; 3 terminals; 1.9 mm pitch; 2.9 mm x 1.3 mm x 1 mm body	SOT23

7. Marking

Table 4. Marking codes

Type number	Marking code[1]
PMV213SN	%2N

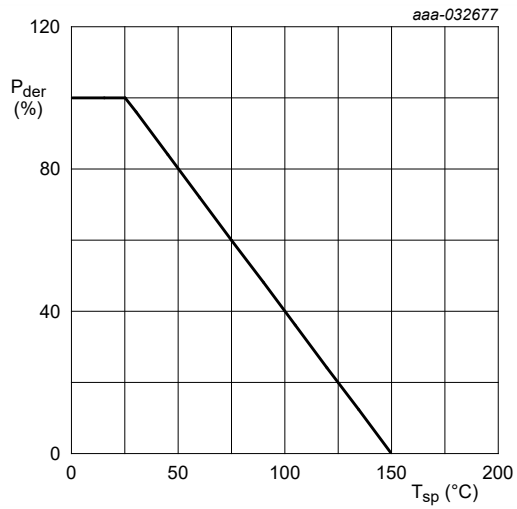
[1] % = placeholder for manufacturing site code

8. Limiting values

Table 5. Limiting values

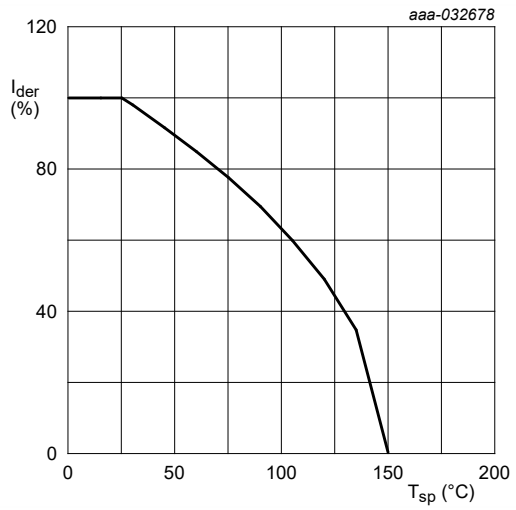
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	25 °C < T_j < 150 °C		-	100	V
V_{DGR}	drain-gate voltage	R_{GS} = 20 kΩ; 25 °C < T_j < 150 °C		-	100	V
V_{GS}	gate-source voltage	T_j = 25 °C		-30	30	V
I_D	drain current	V_{GS} = 10 V; T_{sp} = 25 °C		-	1.9	A
		V_{GS} = 10 V; T_{sp} = 100 °C		-	1.2	A
I_{DM}	peak drain current	T_{sp} = 25 °C; single pulse; t_p ≤ 10 µs		-	7.6	A
P_{tot}	total power dissipation	T_{sp} = 25 °C		-	2	W
T_j	junction temperature			-55	150	°C
T_{stg}	storage temperature			-55	150	°C
Source-drain diode						
I_S	source current	T_{sp} = 25 °C		-	1.7	A
I_{SM}	peak source current	single pulse; t_p ≤ 10 µs; T_{sp} = 25 °C		-	6.9	A



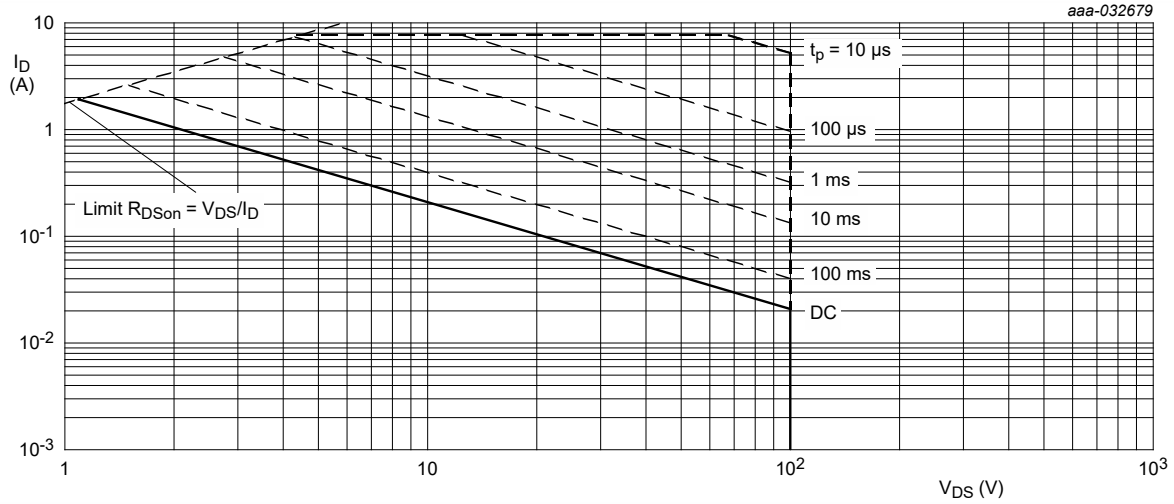
$$P_{der} = \frac{P_{tot}}{P_{tot\,(25\,°C)}} \times 100\,\%$$

Fig. 1. Normalized total power dissipation as a function of solder point temperature



$$I_{der} = \frac{I_D}{I_{D\,(25\,°C)}} \times 100\,\%$$

Fig. 2. Normalized continuous drain current as a function of solder point temperature



T_{sp} = 25 °C; I_{DM} is single pulse; V_{GS} = 10 V

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j\text{-}sp)}$	thermal resistance from junction to solder point			-	-	60	K/W

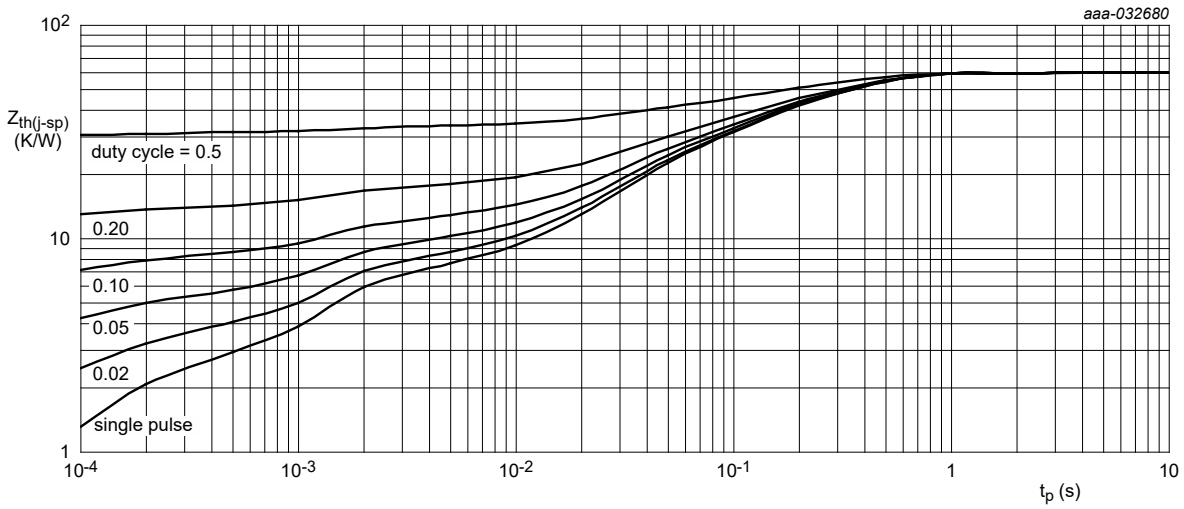
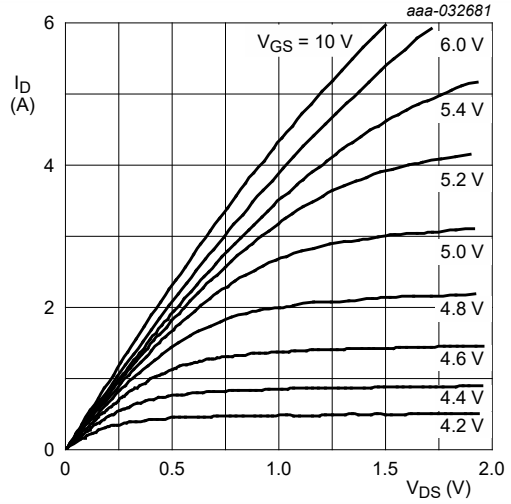


Fig. 4. Transient thermal impedance from junction to solder point as a function of pulse duration

10. Characteristics

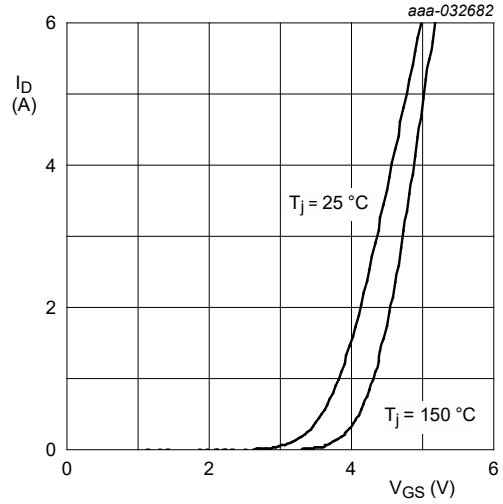
Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		100	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C		90	-	-	V
V_{GSth}	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C		2	3	4	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 150 °C		1.2	-	-	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C		-	-	4.4	V
I_{DSS}	drain leakage current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C		-	-	1	µA
		V_{DS} = 100 V; V_{GS} = 0 V; T_j = 150 °C		-	-	100	µA
I_{GSS}	gate leakage current	V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C		-	10	100	nA
		V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C		-	-10	-100	µA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 0.5 A; T_j = 25 °C		-	213	250	mΩ
		V_{GS} = 10 V; I_D = 0.5 A; T_j = 150 °C		-	490	575	mΩ
$Q_{G(tot)}$	total gate charge	V_{DS} = 80 V; I_D = 1.2 A; V_{GS} = 10 V; T_j = 25 °C		-	7	-	nC
Q_{GS}	gate-source charge			-	1.4	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge			-	2.5	-	nC
C_{iss}	input capacitance	V_{DS} = 20 V; f = 1 MHz; V_{GS} = 0 V; T_j = 25 °C		-	330	-	pF
C_{oss}	output capacitance			-	36	-	pF
C_{rss}	reverse transfer capacitance			-	22	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 50 V; R_L = 33 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 6 Ω; T_j = 25 °C		-	5.5	-	ns
t_r	rise time			-	5	-	ns
$t_{d(off)}$	turn-off delay time			-	9.5	-	ns
t_f	fall time			-	3	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 1.5 A; V_{GS} = 0 V; T_j = 25 °C		-	0.83	1.2	V
t_{rr}	reverse recovery time	I_S = 1.2 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; T_j = 25 °C		-	36	-	ns
Q_r	recovered charge			-	23	-	nC



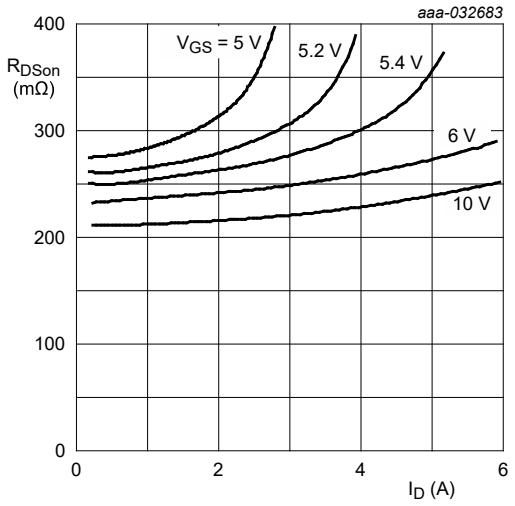
T_j = 25 °C

Fig. 5. Output characteristics: drain current as a function of drain-source voltage; typical values



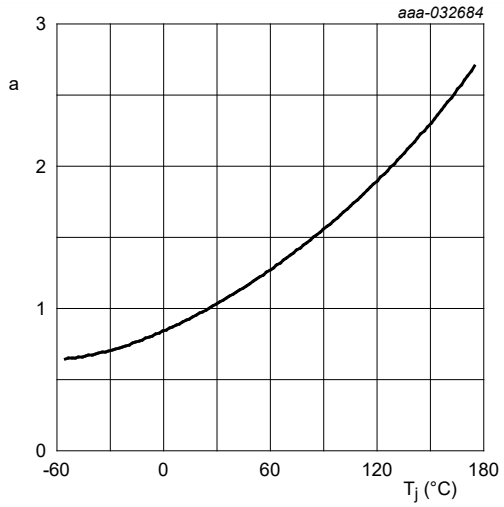
$V_{DS} > I_D \times R_{DSon}$

Fig. 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values



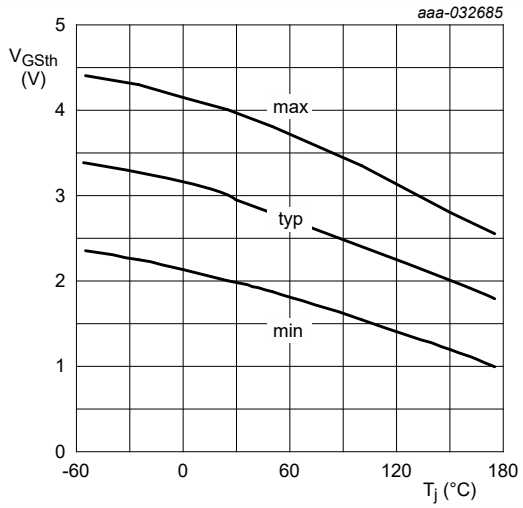
T_j = 25 °C

Fig. 7. Drain-source on-state resistance as a function of drain current; typical values



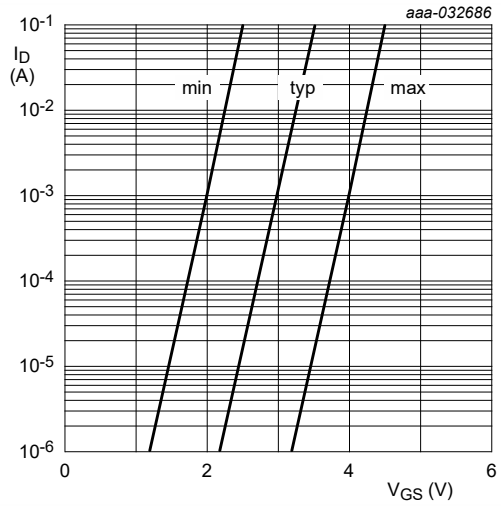
$$a = \frac{R_{DSon}}{R_{DSon(25\,°C)}}$$

Fig. 8. Normalized drain-source on-state resistance as a function of junction temperature



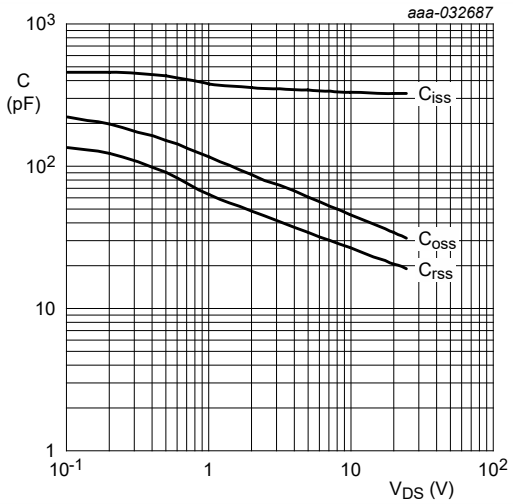
I_D = 1 mA; V_{DS} = V_{GS}

Fig. 9. Gate-source threshold voltage as a function of junction temperature



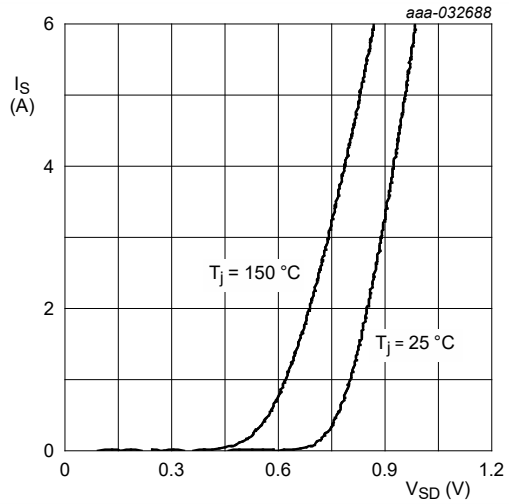
T_j = 25 °C

Fig. 10. Subthreshold drain current as a function of gate-source voltage



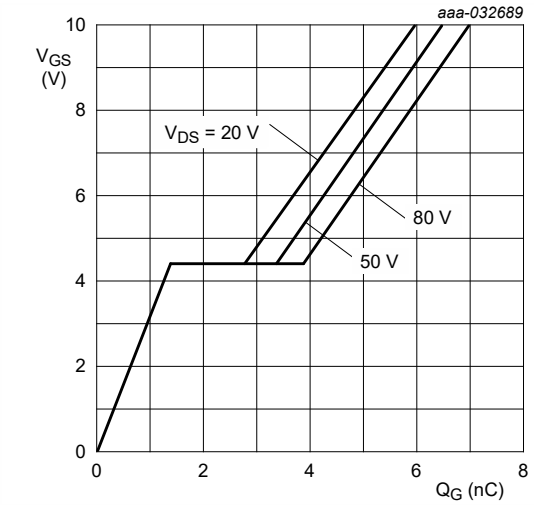
f = 1 MHz; V_{GS} = 0 V

Fig. 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



V_{GS} = 0 V

Fig. 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

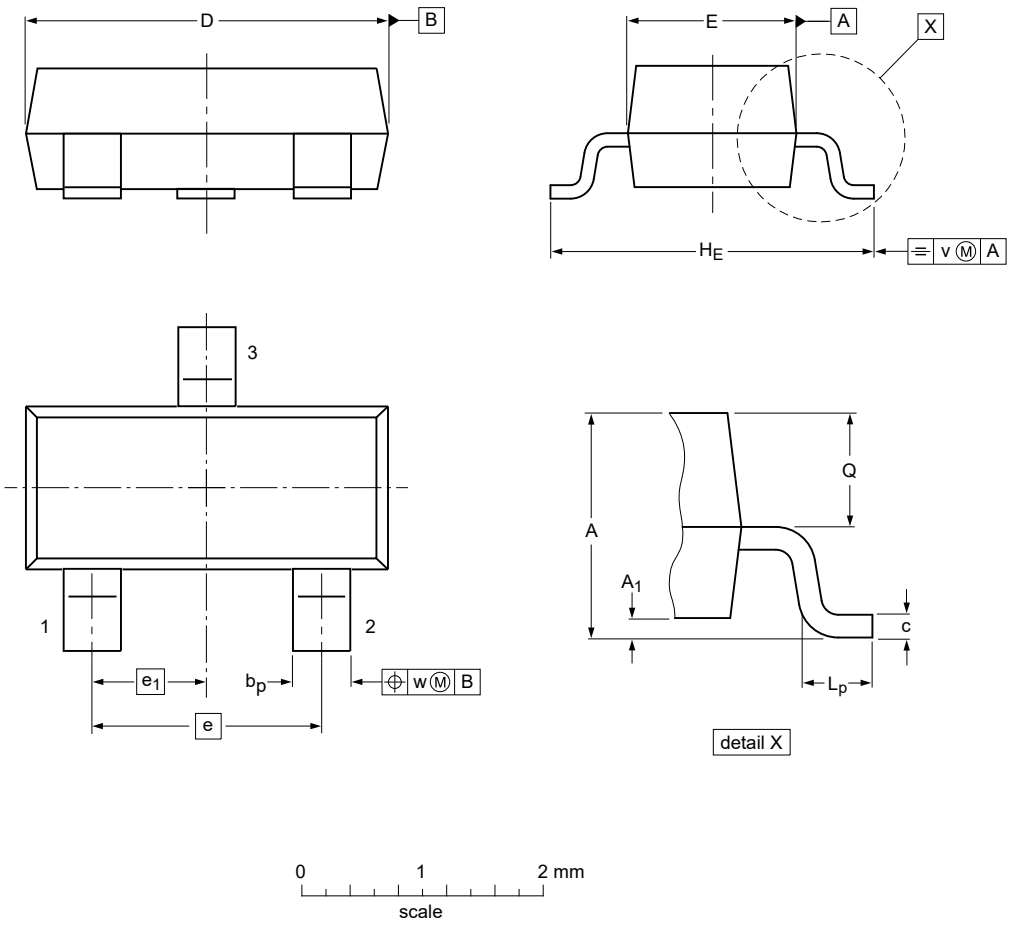


I_D = 1.2 A; T_j = 25 °C

Fig. 13. Gate-source voltage as a function of gate charge; typical values

11. Package outline

Plastic surface-mounted package; 3 leads **SOT23**



Dimensions (mm are the original dimensions)

Unit		A	A_1	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w
mm	max	1.1	0.1	0.48	0.15	3.0	1.4			2.5	0.45	0.55		
	nom							1.9	0.95				0.2	0.1
	min	0.9		0.38	0.09	2.8	1.2			2.1	0.15	0.45		

sot023_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT23		TO-236AB				~~14-06-19~~ 14-09-22

Fig. 14. Package outline SOT23

12. Soldering

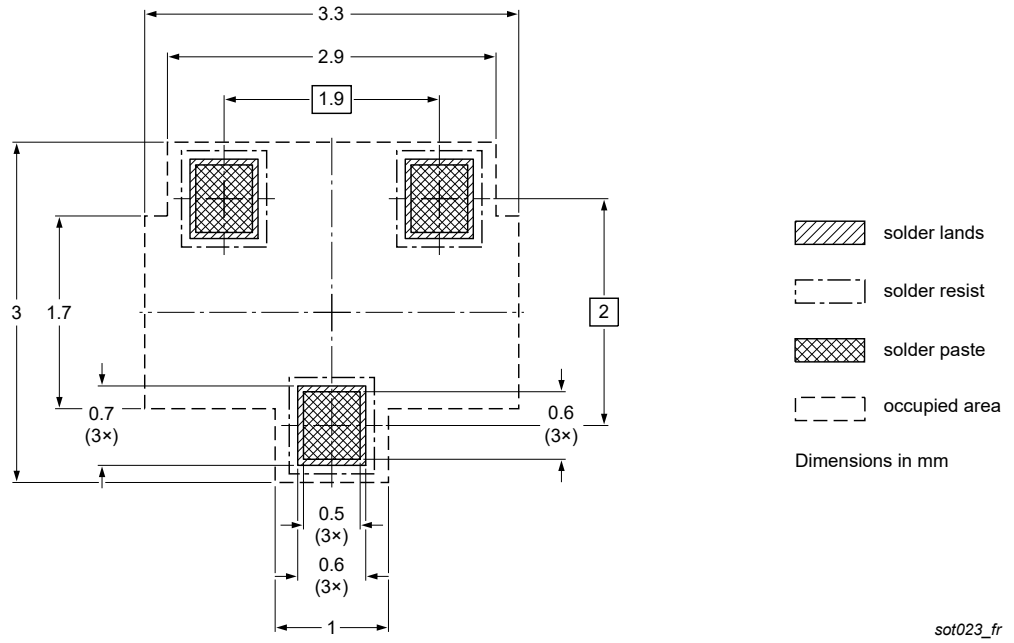


Fig. 15. Reflow soldering footprint for SOT23

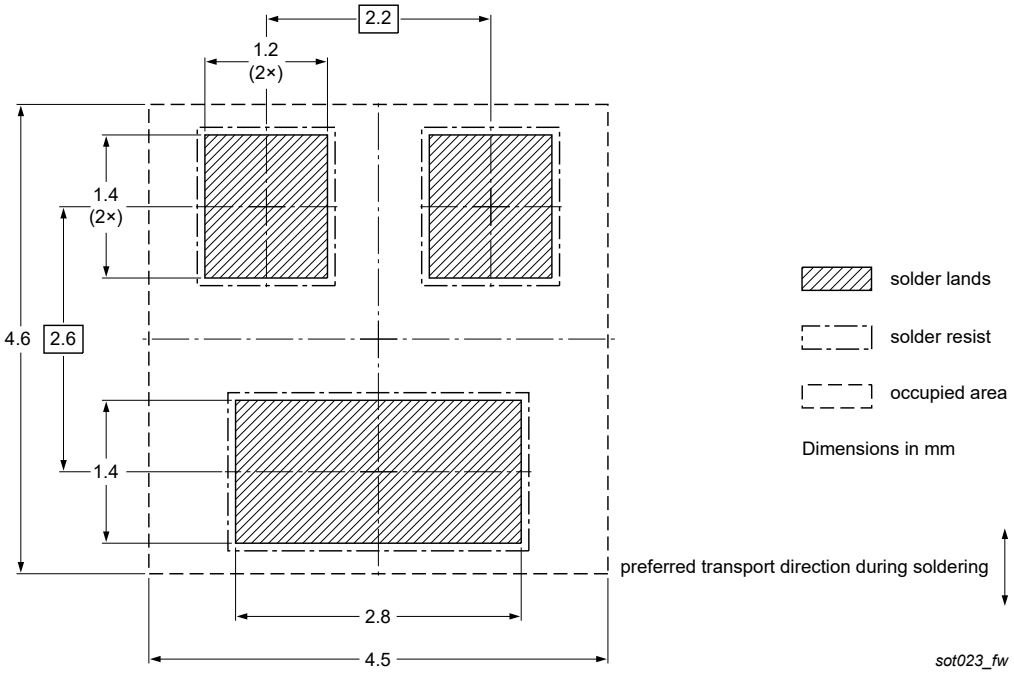


Fig. 16. Wave soldering footprint for SOT23

13. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMV213SN v.3	20201123	Product data sheet	-	PMV213SN v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate.			
PMV213SN v.2	20030219	Product data sheet	-	PMV213SN v.1
PMV213SN v.1	20030115	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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