

# PMXB350UPE

20 V, P-channel Trench MOSFET

24 January 2014

Product data sheet

## 1. General description

P-channel enhancement mode Field-Effect Transistor (FET) in a leadless ultra small DFN1010D-3 (SOT1215) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

## 2. Features and benefits

- Trench MOSFET technology
- Leadless ultra small and ultra thin SMD plastic package:  $1.1 \times 1.0 \times 0.37$  mm
- Exposed drain pad for excellent thermal conduction
- ElectroStatic Discharge (ESD) protection 1 kV HBM
- Drain-source on-state resistance  $R_{DSon} = 350$  m $\Omega$

## 3. Applications

- High-side load switch and charging switch for portable devices
- Power management in battery driven portables
- LED driver
- DC-to-DC converter

## 4. Quick reference data

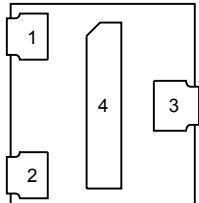
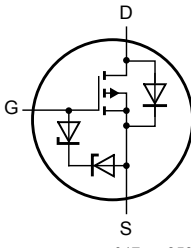
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j = 25$ °C	-	-	-20	V
$V_{GS}$	gate-source voltage		-8	-	8	V
$I_D$	drain current	$V_{GS} = -4.5$ V; $T_{amb} = 25$ °C	[1]	-	-1.2	A
<b>Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = -4.5$ V; $I_D = -1.2$ A; $T_j = 25$ °C	-	350	447	m $\Omega$

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain  $6$  cm<sup>2</sup>.

### 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>Transparent top view DFN1010D-3 (SOT1215)</p>	 <p>017aaa259</p>
2	S	source		
3	D	drain		
4	D	drain		

### 6. Ordering information

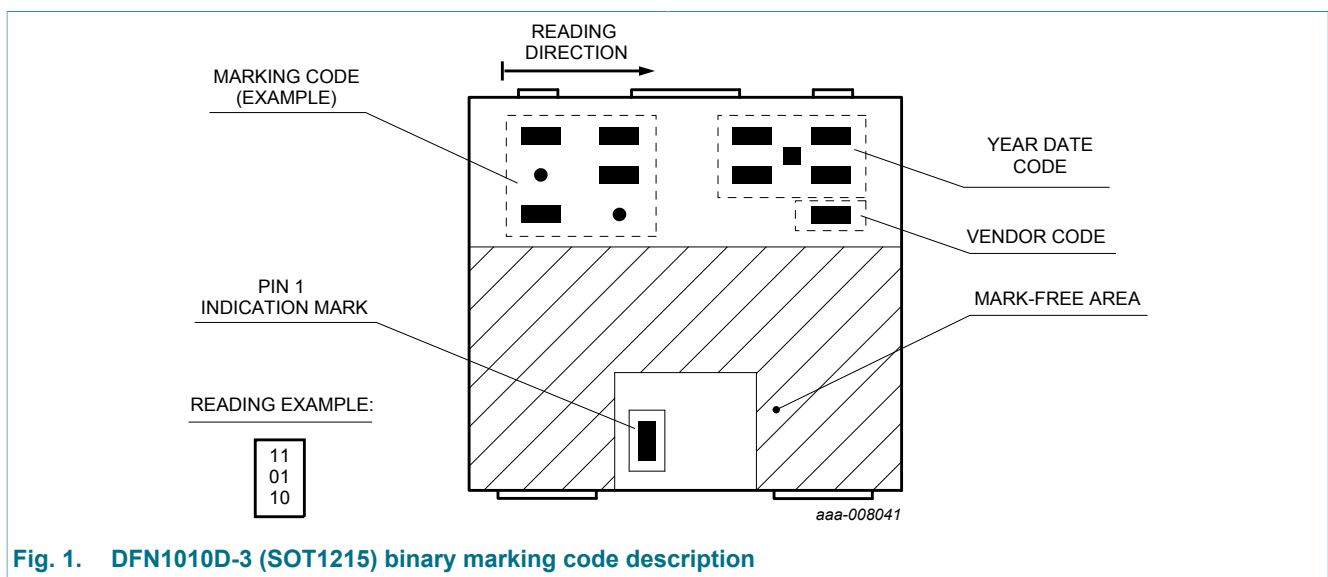
Table 3. Ordering information

Type number	Package		Version
	Name	Description	
PMXB350UPE	DFN1010D-3	DFN1010D-3: plastic thermal enhanced ultra thin small outline package; no leads; 3 terminals; body 1.1 x 1.0 x 0.37 mm	SOT1215

### 7. Marking

Table 4. Marking codes

Type number	Marking code
PMXB350UPE	11 10 00



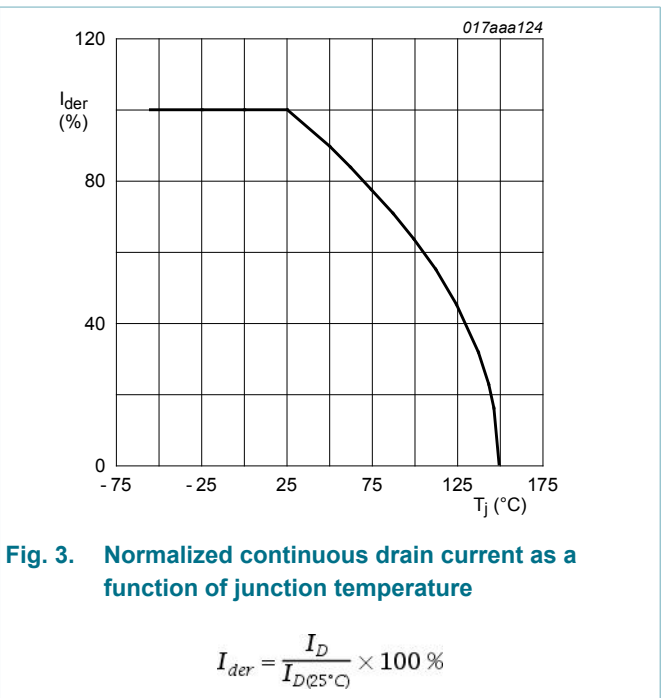
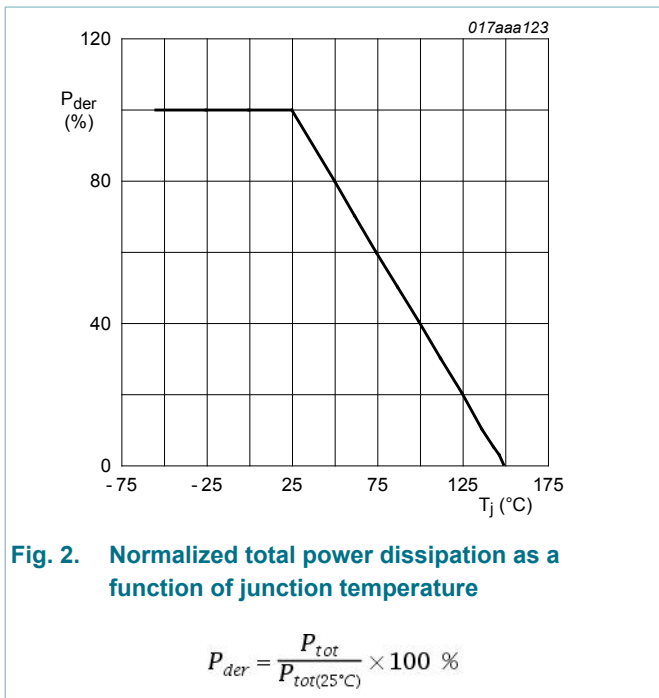
## 8. Limiting values

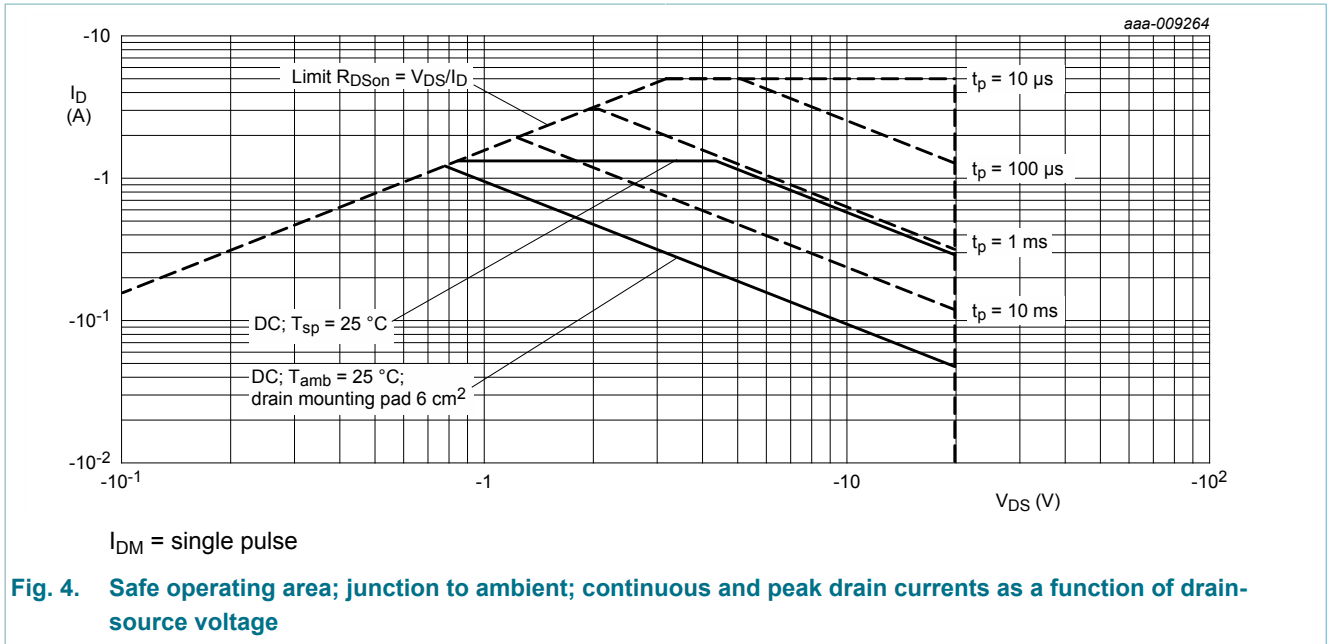
**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> = 25 °C		-	-20	V
V <sub>GS</sub>	gate-source voltage			-8	8	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = -4.5 V; T <sub>amb</sub> = 25 °C	[1]	-	-1.2	A
		V <sub>GS</sub> = -4.5 V; T <sub>amb</sub> = 100 °C	[1]	-	-1	A
I <sub>DM</sub>	peak drain current	T <sub>amb</sub> = 25 °C; single pulse; t <sub>p</sub> ≤ 10 μs		-	-5	A
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = 25 °C	[2]	-	360	mW
			[1]	-	930	mW
		T <sub>sp</sub> = 25 °C		-	5680	mW
T <sub>j</sub>	junction temperature			-55	150	°C
T <sub>amb</sub>	ambient temperature			-55	150	°C
T <sub>stg</sub>	storage temperature			-65	150	°C
<b>Source-drain diode</b>						
I <sub>S</sub>	source current	T <sub>amb</sub> = 25 °C	[1]	-	-0.9	A

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm<sup>2</sup>.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.





## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	303	348	K/W
			[2]	-	116	134	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	17	22	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain  $6\text{ cm}^2$ .

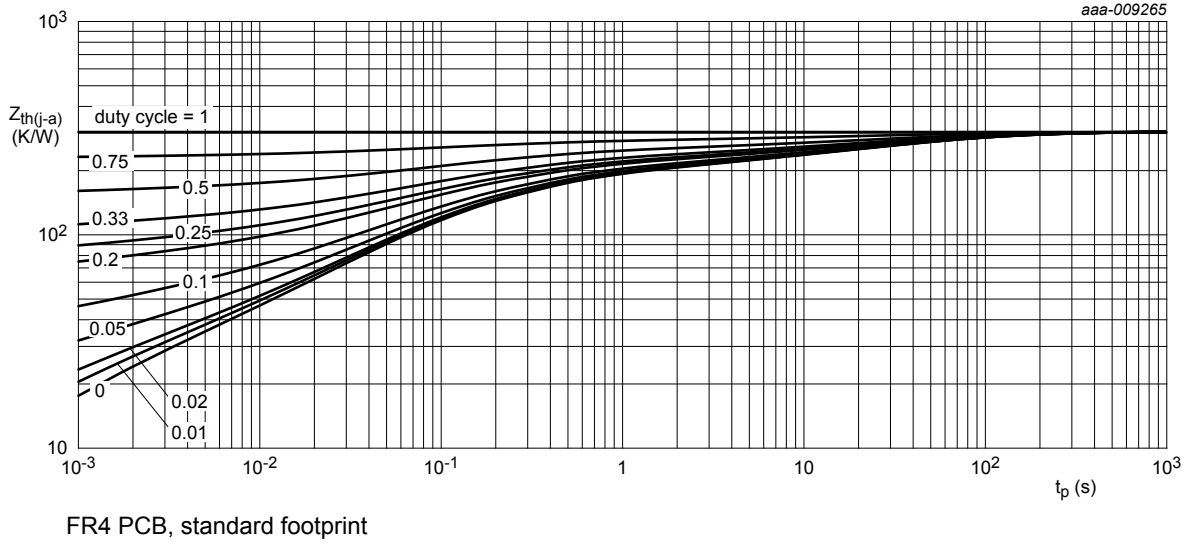


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

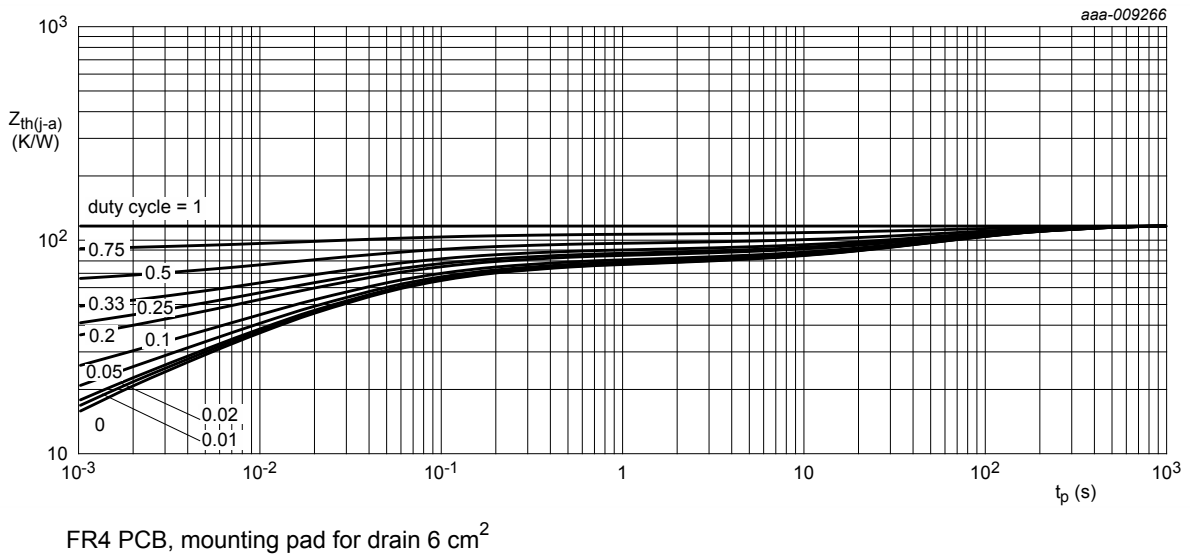
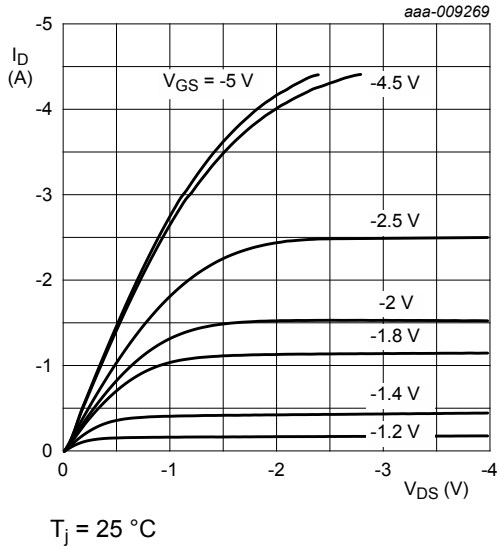


Fig. 6. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

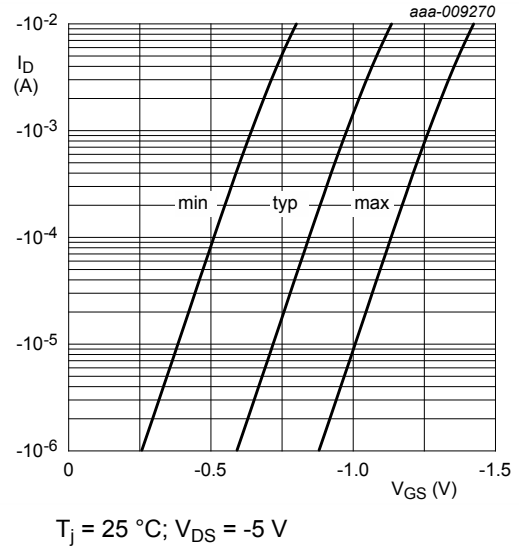
## 10. Characteristics

Table 7. Characteristics

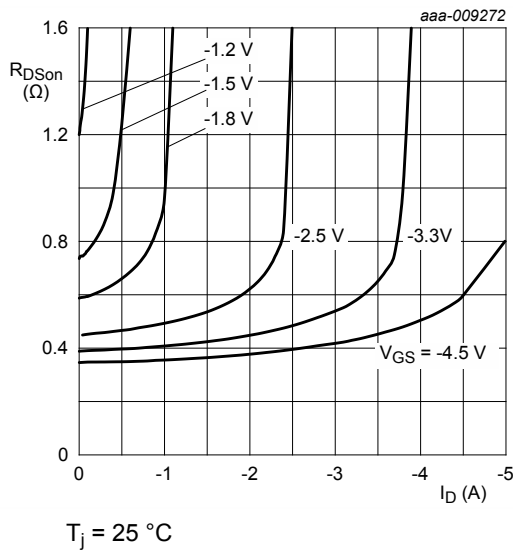
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -250 \mu\text{A}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-20	-	-	V
$V_{GSth}$	gate-source threshold voltage	$I_D = -250 \mu\text{A}$ ; $V_{DS} = V_{GS}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-0.45	-0.7	-0.95	V
$I_{DSS}$	drain leakage current	$V_{DS} = -20 \text{ V}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	-	-1	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = -8 \text{ V}$ ; $V_{DS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	-	-10	$\mu\text{A}$
		$V_{GS} = 8 \text{ V}$ ; $V_{DS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	-	10	$\mu\text{A}$
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = -4.5 \text{ V}$ ; $I_D = -1.2 \text{ A}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	350	447	m $\Omega$
		$V_{GS} = -4.5 \text{ V}$ ; $I_D = -1.2 \text{ A}$ ; $T_j = 150 \text{ }^\circ\text{C}$	-	508	650	m $\Omega$
		$V_{GS} = -2.5 \text{ V}$ ; $I_D = -1 \text{ A}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	450	645	m $\Omega$
		$V_{GS} = -1.8 \text{ V}$ ; $I_D = -0.4 \text{ A}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	600	940	m $\Omega$
		$V_{GS} = -1.5 \text{ V}$ ; $I_D = -10 \text{ mA}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	760	2000	m $\Omega$
		$V_{GS} = -1.2 \text{ V}$ ; $I_D = -1 \text{ mA}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	1200	-	m $\Omega$
$g_{fs}$	forward transconductance	$V_{DS} = -5 \text{ V}$ ; $I_D = -1.2 \text{ A}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	5.2	-	S
$R_G$	gate resistance	$f = 1 \text{ MHz}$	-	0.8	-	$\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$V_{DS} = -10 \text{ V}$ ; $I_D = -1.2 \text{ A}$ ; $V_{GS} = -4.5 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	1.25	2.3	nC
$Q_{GS}$	gate-source charge		-	0.27	-	nC
$Q_{GD}$	gate-drain charge		-	0.28	-	nC
$C_{iss}$	input capacitance	$V_{DS} = -10 \text{ V}$ ; $f = 1 \text{ MHz}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	116	-	pF
$C_{oss}$	output capacitance		-	16.5	-	pF
$C_{rss}$	reverse transfer capacitance		-	12.2	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = -10 \text{ V}$ ; $I_D = -1.2 \text{ A}$ ; $V_{GS} = -4.5 \text{ V}$ ; $R_{G(ext)} = 6 \text{ } \Omega$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	3	-	ns
$t_r$	rise time		-	9	-	ns
$t_{d(off)}$	turn-off delay time		-	18	-	ns
$t_f$	fall time		-	6	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = -0.9 \text{ A}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	-0.8	-1.2	V



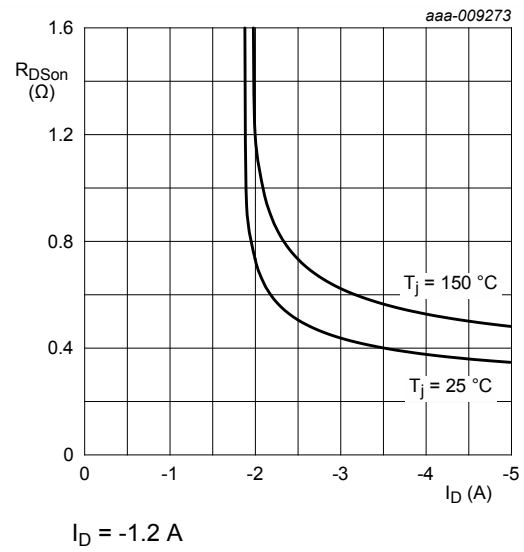
**Fig. 7. Output characteristics: drain current as a function of drain-source voltage; typical values**



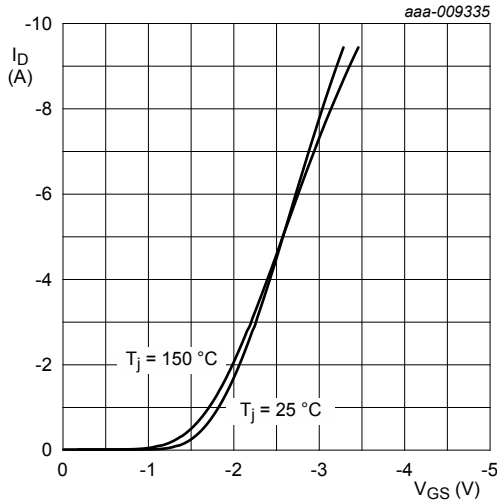
**Fig. 8. Sub-threshold drain current as a function of gate-source voltage**



**Fig. 9. Drain-source on-state resistance as a function of drain current; typical values**



**Fig. 10. Drain-source on-state resistance as a function of gate-source voltage; typical values**



$$V_{DS} > I_D \times R_{DS(on)}$$

Fig. 11. Transfer characteristics: drain current as a function of gate-source voltage; typical values

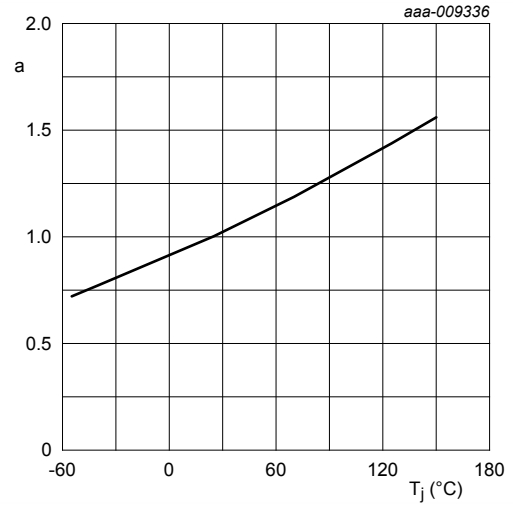
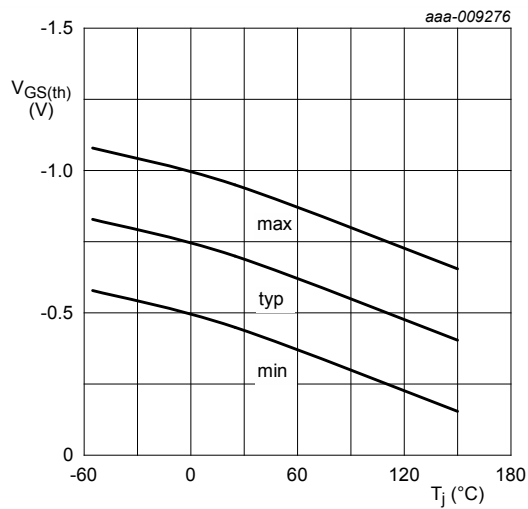


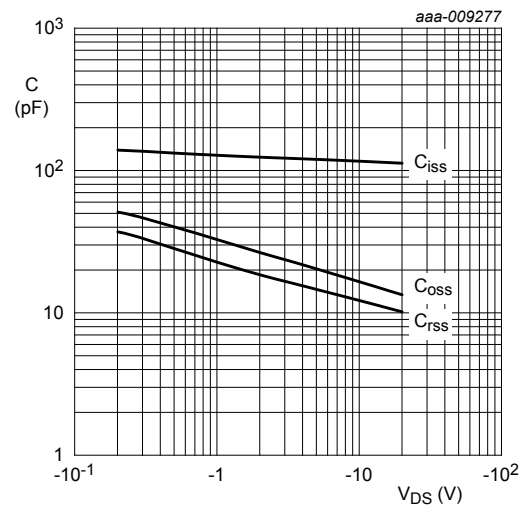
Fig. 12. Normalized drain-source on-state resistance as a function of junction temperature; typical values

$$a = \frac{R_{DS(on)}}{R_{DS(on)(25^\circ C)}}$$



$$I_D = -0.25 \text{ mA}; V_{DS} = V_{GS}$$

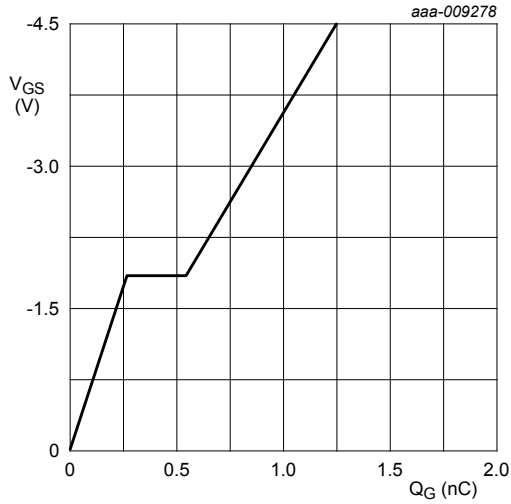
Fig. 13. Gate-source threshold voltage as a function of junction temperature



$$f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}$$

Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values





$I_D = -1.2 \text{ A}; V_{DS} = -10 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}$

Fig. 15. Gate-source voltage as a function of gate charge; typical values

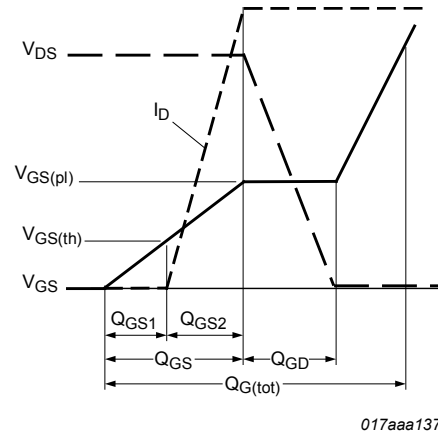
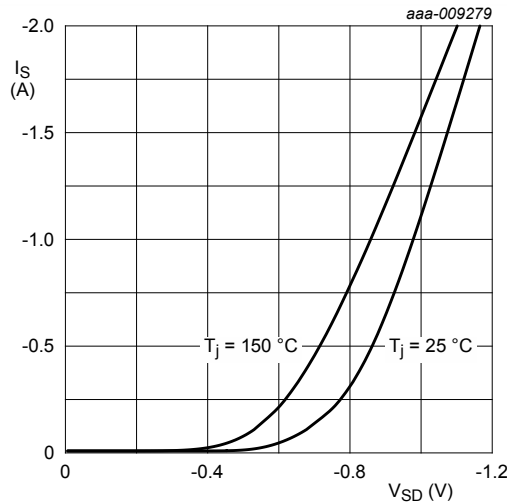


Fig. 16. MOSFET transistor: Gate charge waveform definitions



$V_{GS} = 0 \text{ V}$

Fig. 17. Source current as a function of source-drain voltage; typical values

## 11. Test information

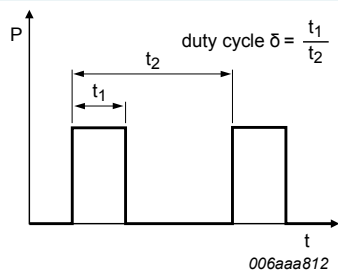


Fig. 18. Duty cycle definition

## 12. Package outline

DFN1010D-3: plastic thermal enhanced ultra thin small outline package; no leads;  
3 terminals; body: 1.1 x 1.0 x 0.37 mm

SOT1215

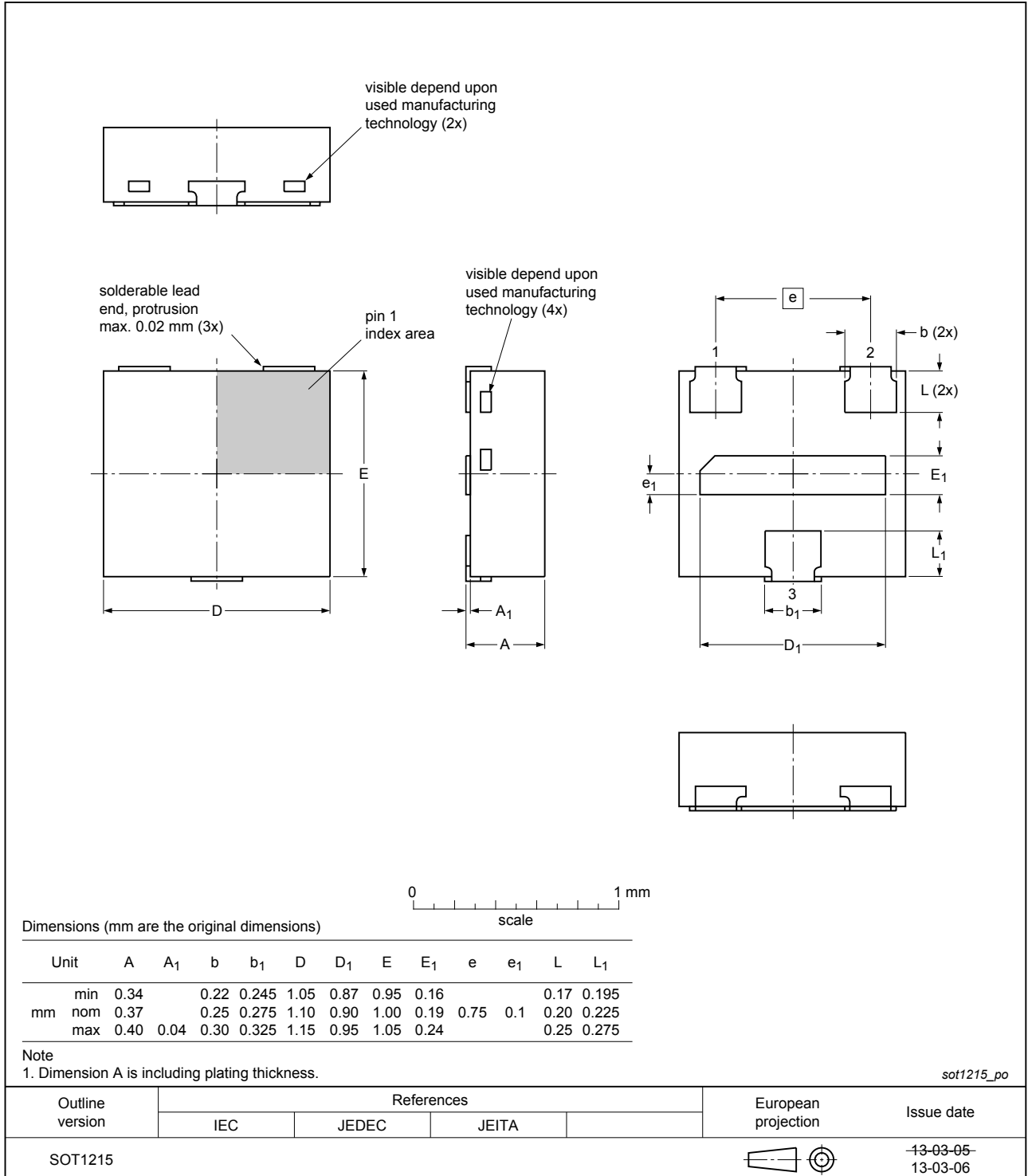


Fig. 19. Package outline DFN1010D-3 (SOT1215)

### 13. Soldering

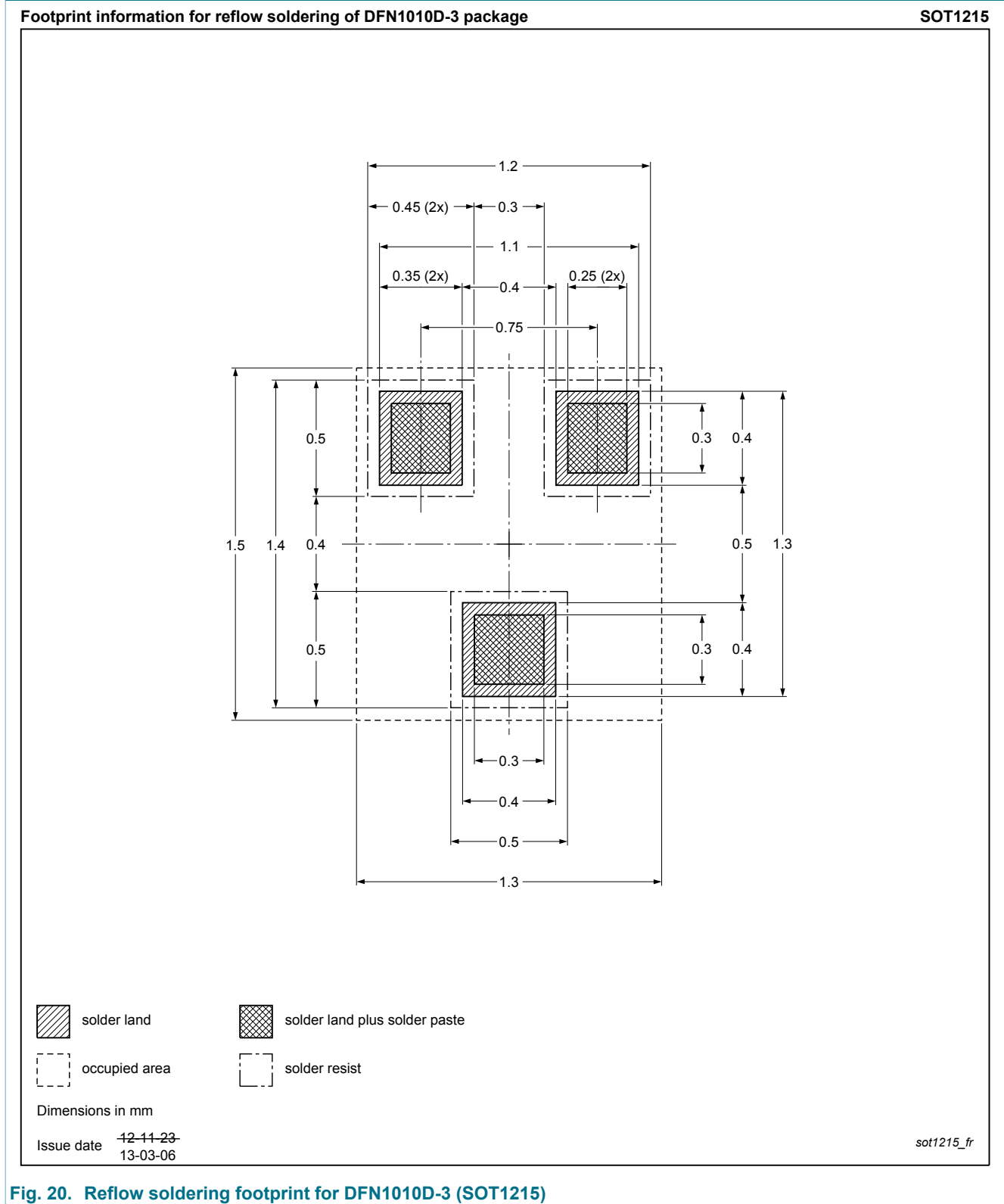


Fig. 20. Reflow soldering footprint for DFN1010D-3 (SOT1215)

## 14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMXB350UPE v.2	20140124	Product data sheet	-	PMXB350UPE v.1
Modifications:	<ul style="list-style-type: none"><li>Editorial update</li></ul>			
PMXB350UPE v.1	20130919	Product data sheet	-	-

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### 15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
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