Product data sheet

1. General description

N-channel enhancement mode Field-Effect Transistor (FET) in a leadless ultra small DFN1010D-3 (SOT1215) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Trench MOSFET technology
- Leadless ultra small and thin SMD plastic package: 1.1 × 1.0 × 0.37 mm
- · Exposed drain pad for excellent thermal conduction
- Very low Drain-Source on-state resistance R_{DSon} = 49 mΩ
- · Very fast switching

3. Applications

- · Low-side load switch and charging switch for portable devices
- Power management in battery-driven portables
- · LED driver
- DC-to-DC converters

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V _{DS}	drain-source voltage	T _j = 25 °C		-	-	30	V
V _{GS}	gate-source voltage			-20	-	20	V
I _D	drain current	V _{GS} = 10 V; T _{amb} = 25 °C	[1]	-	-	3.2	Α
Static characte	Static characteristics						
R _{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 3.2 \text{ A}; T_j = 25 ^{\circ}\text{C}$		-	49	55	mΩ

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².



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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		D I
2	S	source		
3	D	drain	4 3	G C
4	D	drain		s
			2	017aaa253
			Transparent top view DFN1010D-3 (SOT1215)	

6. Ordering information

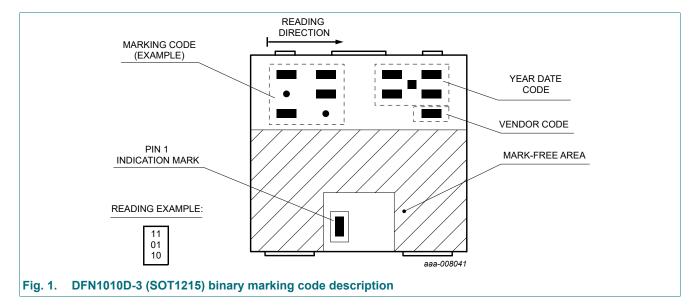
Table 3. Ordering information

Type number	Package					
	Name	Description	Version			
PMXB56EN	DFN1010D-3	plastic, leadless thermal enhanced ultra thin small outline package with side-wettable flanks (SWF); 3 terminals; 0.75 mm pitch; 1.1 mm x 1 mm x 0.37 mm body	SOT1215			

7. Marking

Table 4. Marking codes

Type number	Marking code
PMXB56EN	01
	10
	10



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8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	T _j = 25 °C		-	30	V
V _{GS}	gate-source voltage			-20	20	V
I _D	drain current	V _{GS} = 10 V; T _{amb} = 25 °C	[1]	-	3.2	Α
		V _{GS} = 10 V; T _{amb} = 100 °C	[1]	-	2.8	Α
I _{DM}	peak drain current	T_{amb} = 25 °C; single pulse; $t_p \le 10 \mu s$		-	15	Α
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	0.4	W
			[1]	-	1.07	W
		T _{sp} = 25 °C		-	8.33	W
Tj	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
Source-drain	n diode					
Is	source current	T _{amb} = 25 °C	[1]	-	1	А

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².
- [2] Device mounted on an FR4 Printed Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

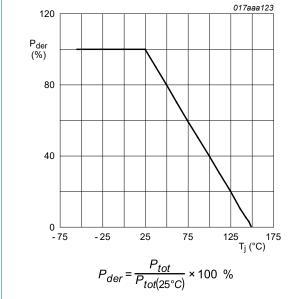


Fig. 2. Normalized total power dissipation as a function of junction temperature

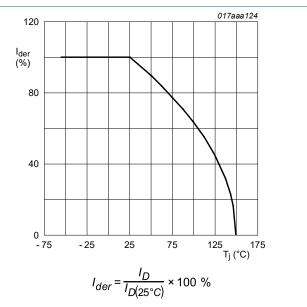


Fig. 3. Normalized continuous drain current as a function of junction temperature

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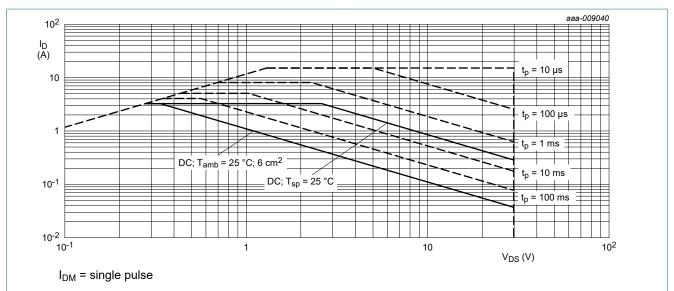


Fig. 4. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drainsource voltage

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
R _{th(j-a)}	thermal resistance from	in free air	[1]	-	271	312	K/W
junction to ambie	junction to ambient		[2]	-	102	117	K/W
R _{th(j-sp)}	thermal resistance from junction to solder point			-	10	15	K/W

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm².

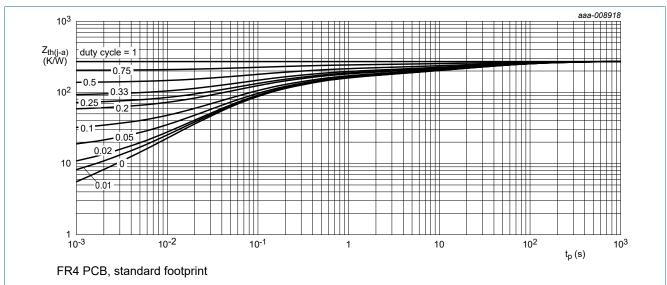
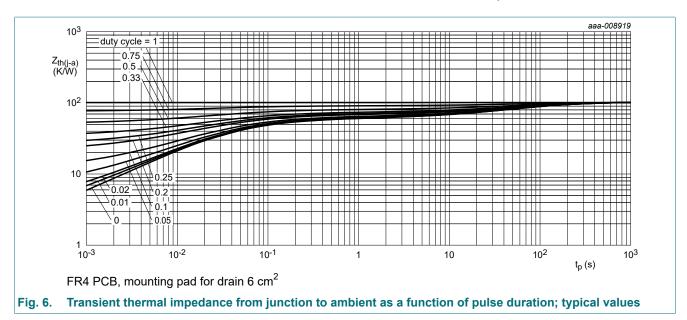


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

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10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics					
V _{(BR)DSS}	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 °C$	30	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = 250 \mu A; V_{DS} = V_{GS}; T_j = 25 \text{ °C}$	1	1.5	2	V
I _{DSS}	drain leakage current	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	1	μΑ
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C	-	-	100	nA
		V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C	-	-	-100	nA
R _{DSon}	drain-source on-state	V_{GS} = 10 V; I_D = 3.2 A; T_j = 25 °C	-	49	55	mΩ
	resistance	V_{GS} = 10 V; I_D = 2.8 A; T_j = 150 °C	-	77	87	mΩ
		$V_{GS} = 4.5 \text{ V}; I_D = 3.2 \text{ A}; T_j = 25 ^{\circ}\text{C}$	-	56	65	mΩ
9fs	forward transconductance	$V_{DS} = 10 \text{ V}; I_D = 3.2 \text{ A}; T_j = 25 \text{ °C}$	-	13	-	S
R_G	gate resistance	f = 1 MHz; T _j = 25 °C	-	2.3	-	Ω
Dynamic ch	aracteristics					'
Q _{G(tot)}	total gate charge	V_{DS} = 15 V; I_{D} = 3.2 A; V_{GS} = 10 V;	-	3.6	6.3	nC
Q _{GS}	gate-source charge	T _j = 25 °C	-	0.5	-	nC
Q _{GD}	gate-drain charge		-	0.4	-	nC
C _{iss}	input capacitance	V _{DS} = 15 V; f = 1 MHz; V _{GS} = 0 V;	-	209	-	pF
C _{oss}	output capacitance	T _j = 25 °C	-	50	-	pF
C _{rss}	reverse transfer capacitance		-	17	-	pF
t _{d(on)}	turn-on delay time	V_{DS} = 15 V; I_{D} = 3.2 A; V_{GS} = 10 V;	-	3	-	ns
t _r	rise time	$R_{G(ext)} = 6 \Omega; T_j = 25 °C$	-	12	-	ns
t _{d(off)}	turn-off delay time	1	-	11	-	ns
t _f	fall time	1	-	2	-	ns
Source-drai	in diode					
V _{SD}	source-drain voltage	I _S = 1 A; V _{GS} = 0 V; T _i = 25 °C	-	0.7	1.2	V

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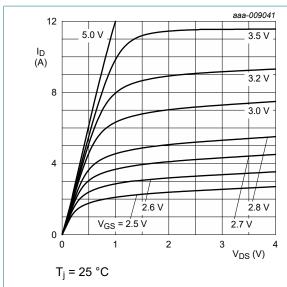


Fig. 7. Output characteristics: drain current as a function of drain-source voltage; typical values

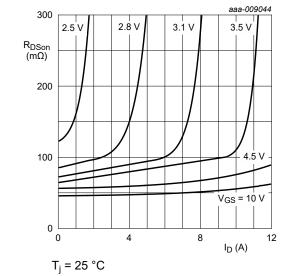


Fig. 9. Drain-source on-state resistance as a function of drain current; typical values

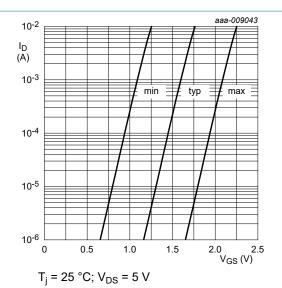


Fig. 8. Sub-threshold drain current as a function of gate-source voltage

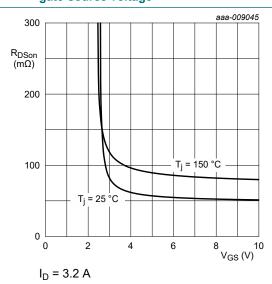


Fig. 10. Drain-source on-state resistance as a function of gate-source voltage; typical values

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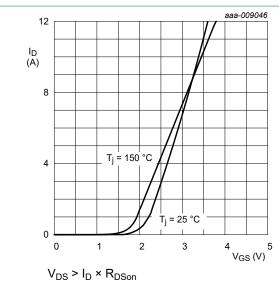


Fig. 11. Transfer characteristics: drain current as a function of gate-source voltage; typical values

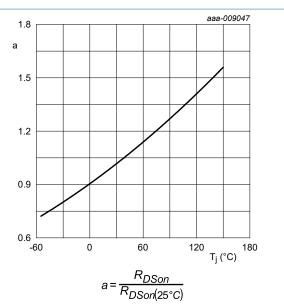


Fig. 12. Normalized drain-source on-state resistance as a function of junction temperature; typical values

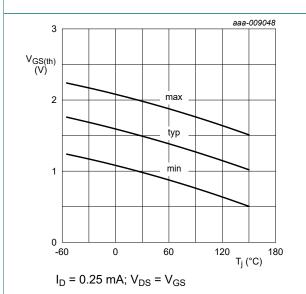
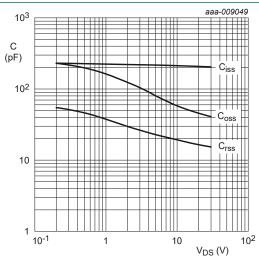


Fig. 13. Gate-source threshold voltage as a function of junction temperature



 $f = 1 MHz; V_{GS} = 0 V$

Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

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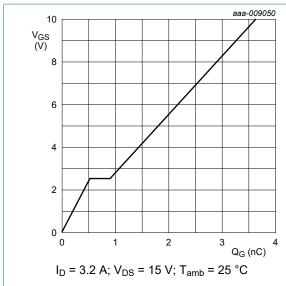


Fig. 15. Gate-source voltage as a function of gate charge; typical values

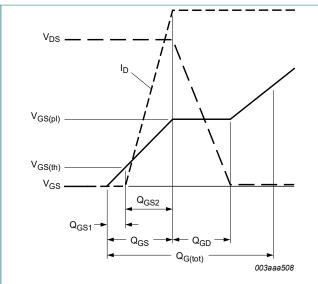


Fig. 16. Gate charge waveform definitions

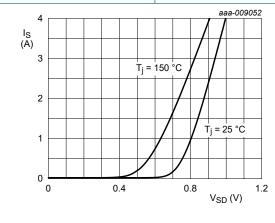
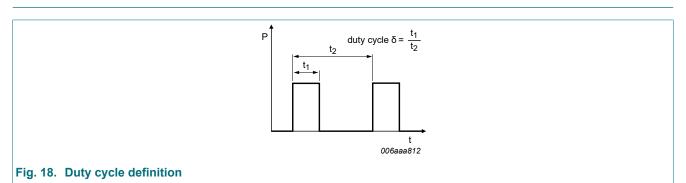


Fig. 17. Source current as a function of source-drain voltage; typical values

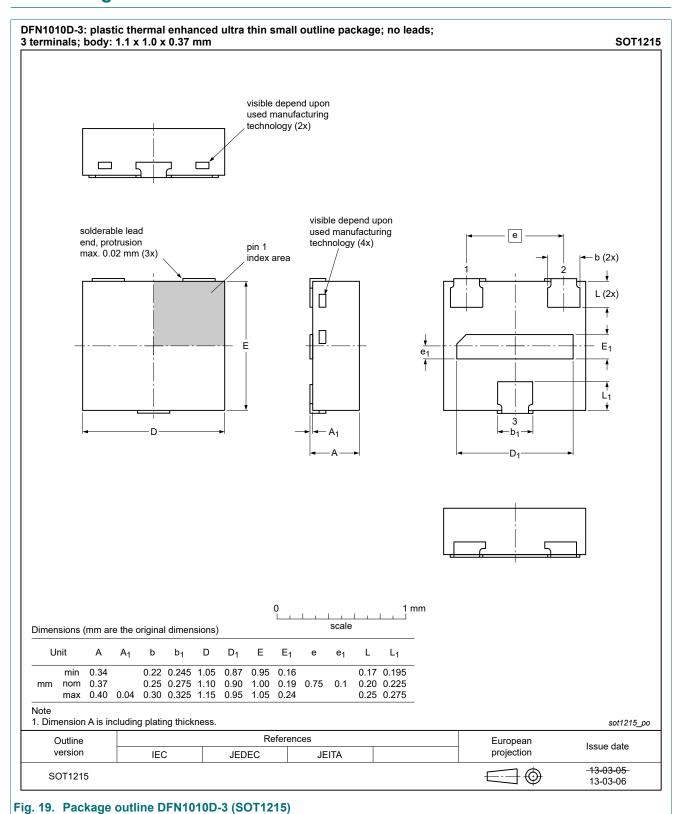
11. Test information

 $V_{GS} = 0 V$



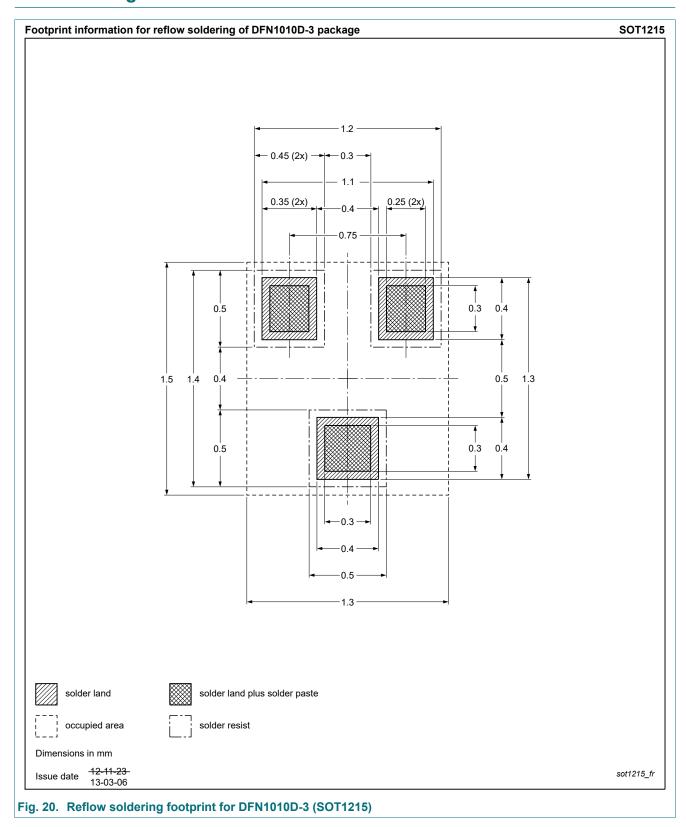
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12. Package outline



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13. Soldering



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14. Revision history

Table 8. Revision history

Table 6. Itevision in	istory			
Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMXB56EN v.4	20201027	Product data sheet	-	PMXB56EN v.3
Modifications:	Nexperia.	this data sheet has been rede ve been adapted to the new o		, ,
PMXB56EN v.3	20170111	Product data sheet	-	PMXB56EN v.2
PMXB56EN v.2	20140430	Product data sheet	-	PMXB56EN v.1
PMXB56EN v.1	20130925	Product data sheet	-	-

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15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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