



PMZ200UNE

30 V, N-channel Trench MOSFET

12 March 2015

Product data sheet

1. General description

N-channel enhancement mode Field-Effect Transistor (FET) in a leadless ultra small DFN1006-3 (SOT883) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Very fast switching
- Low threshold voltage
- Trench MOSFET technology
- ElectroStatic Discharge (ESD) protection: 2 kV HBM
- Leadless ultra small package: 1.0 × 0.6 × 0.48 mm

3. Applications

- Relay driver
- High-speed line driver
- Low-side loadswitch
- Switching circuits

4. Quick reference data

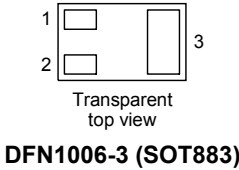
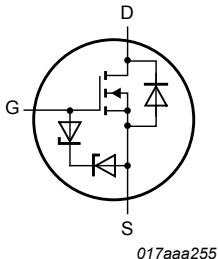
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_J = 25\text{ °C}$	-	-	30	V
V_{GS}	gate-source voltage		-8	-	8	V
I_D	drain current	$V_{GS} = 4.5\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	1.4	A
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}; I_D = 1.4\text{ A}; T_J = 25\text{ °C}$	-	210	250	mΩ

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm².

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>Transparent top view DFN1006-3 (SOT883)</p>	 <p>017aaa255</p>
2	S	source		
3	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMZ200UNE	DFN1006-3	DFN1006-3: leadless ultra small plastic package; 3 solder lands	SOT883

7. Marking

Table 4. Marking codes

Type number	Marking code
PMZ200UNE	ZV

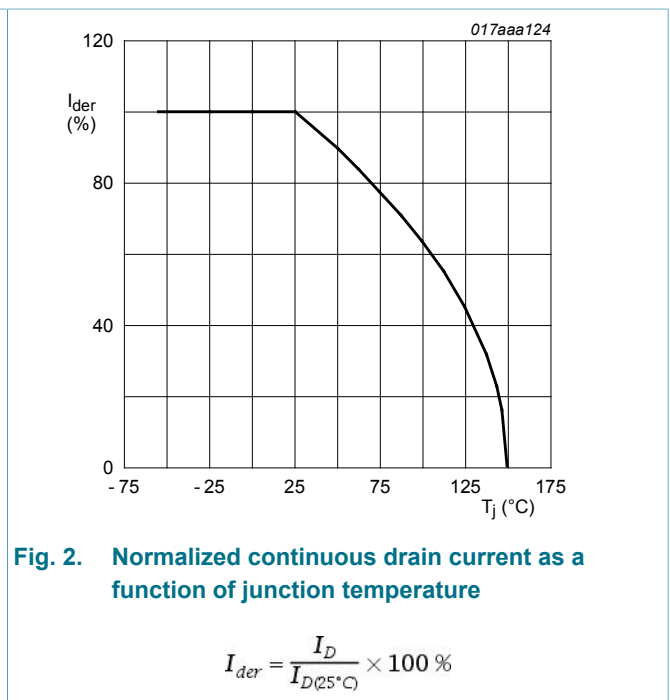
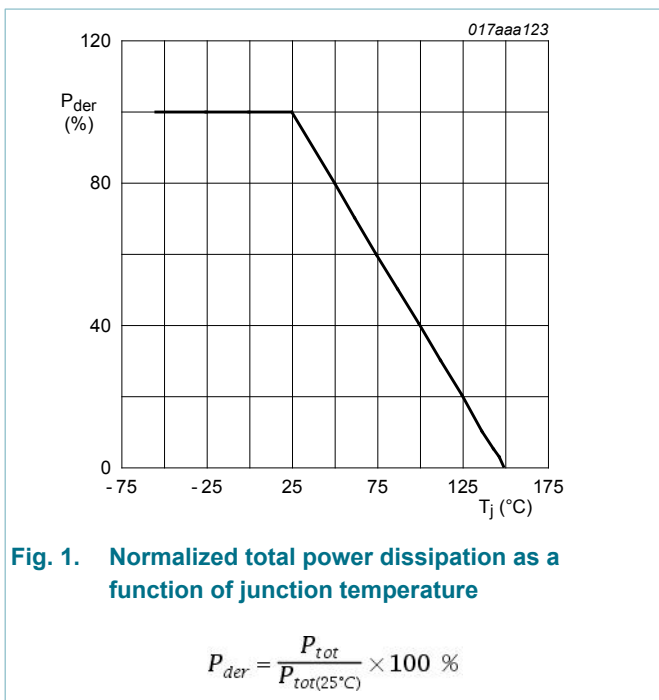
8. Limiting values

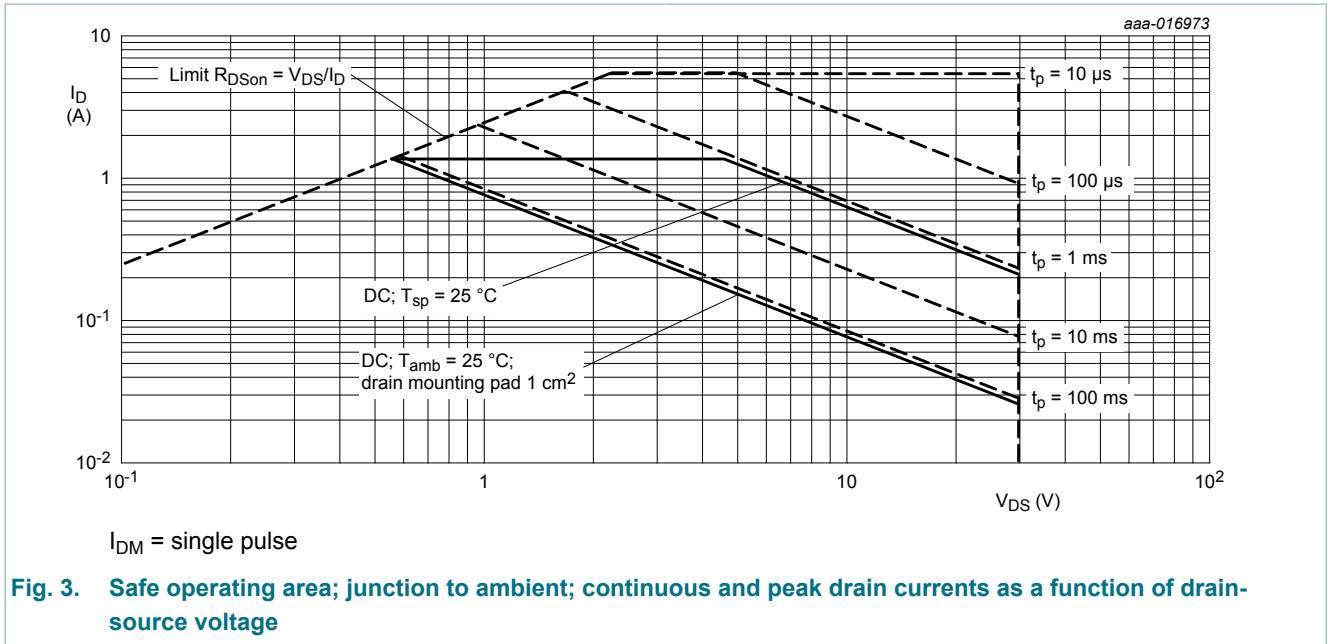
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	T _j = 25 °C		-	30	V
V _{GS}	gate-source voltage			-8	8	V
I _D	drain current	V _{GS} = 4.5 V; T _{amb} = 25 °C	[1]	-	1.4	A
		V _{GS} = 4.5 V; T _{amb} = 100 °C	[1]	-	0.9	A
I _{DM}	peak drain current	T _{amb} = 25 °C; single pulse; t _p ≤ 10 μs		-	5	A
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	350	mW
			[1]	-	760	mW
		T _{sp} = 25 °C		-	6250	mW
T _j	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
Source-drain diode						
I _S	source current	T _{amb} = 25 °C	[1]	-	0.7	A

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm².
- [2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.





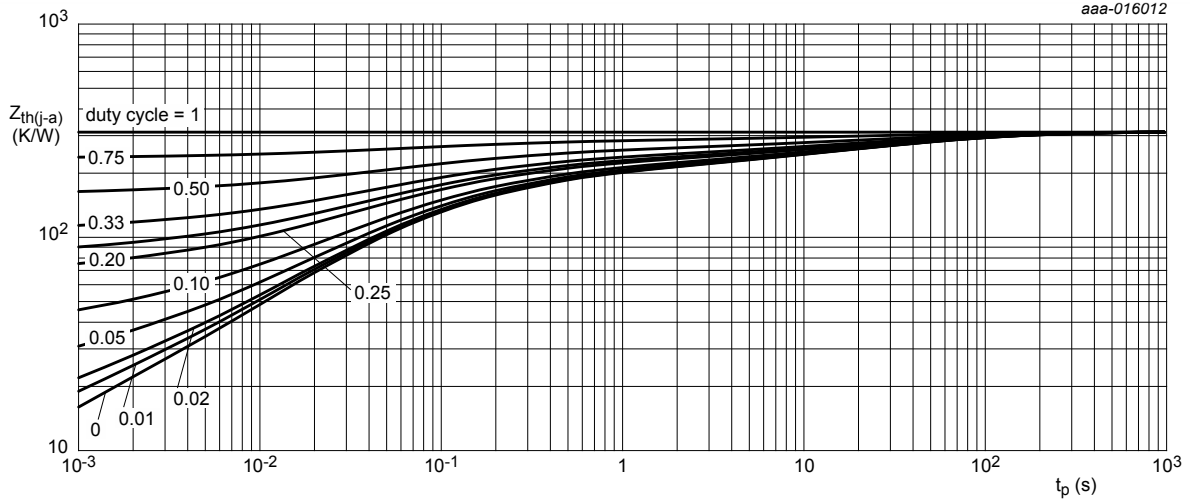
9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	315	360	K/W
			[2]	-	145	165	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	17	20	K/W

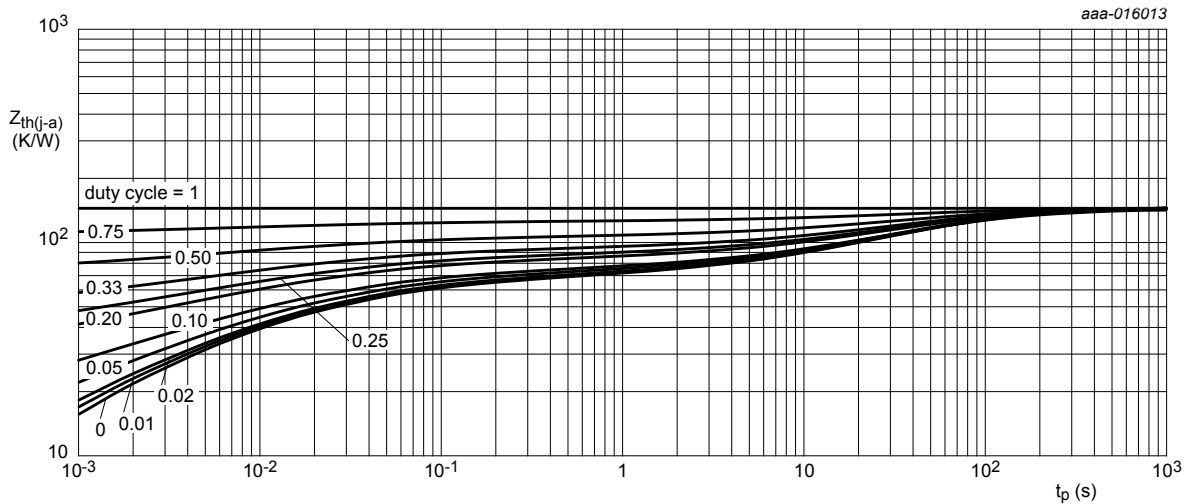
[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm^2 .



FR4 PCB, standard footprint

Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, mounting pad for drain 1 cm²

Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A$; $V_{GS} = 0 V$; $T_j = 25 \text{ }^\circ C$	30	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = 250 \mu A$; $V_{DS} = V_{GS}$; $T_j = 25 \text{ }^\circ C$	0.45	0.7	0.95	V
I_{DSS}	drain leakage current	$V_{DS} = 30 V$; $V_{GS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	-	1	μA
I_{GSS}	gate leakage current	$V_{GS} = 8 V$; $V_{DS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	-	5	μA
		$V_{GS} = -8 V$; $V_{DS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	-	-5	μA
		$V_{GS} = 4.5 V$; $V_{DS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	-	1	μA
		$V_{GS} = -4.5 V$; $V_{DS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	-	-1	μA
		$V_{GS} = 2.5 V$; $V_{DS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	-	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 4.5 V$; $I_D = 1.4 A$; $T_j = 25 \text{ }^\circ C$	-	210	250	m Ω
		$V_{GS} = 4.5 V$; $I_D = 1.4 A$; $T_j = 150 \text{ }^\circ C$	-	347	410	m Ω
		$V_{GS} = 2.5 V$; $I_D = 1.2 A$; $T_j = 25 \text{ }^\circ C$	-	240	310	m Ω
		$V_{GS} = 1.8 V$; $I_D = 1 A$; $T_j = 25 \text{ }^\circ C$	-	270	380	m Ω
		$V_{GS} = 1.5 V$; $I_D = 0.01 A$; $T_j = 25 \text{ }^\circ C$	-	300	490	m Ω
g_{fs}	forward transconductance	$V_{DS} = 10 V$; $I_D = 1 A$; $T_j = 25 \text{ }^\circ C$	-	4.1	-	S
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$V_{DS} = 15 V$; $I_D = 1.5 A$; $V_{GS} = 4.5 V$; $T_j = 25 \text{ }^\circ C$	-	1.6	2.7	nC
Q_{GS}	gate-source charge		-	0.1	-	nC
Q_{GD}	gate-drain charge		-	0.4	-	nC
C_{iss}	input capacitance	$V_{DS} = 15 V$; $f = 1 \text{ MHz}$; $V_{GS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	89	-	pF
C_{oss}	output capacitance		-	11	-	pF
C_{rss}	reverse transfer capacitance		-	9	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 15 V$; $I_D = 0.8 A$; $V_{GS} = 4.5 V$; $R_{G(ext)} = 6 \Omega$; $T_j = 25 \text{ }^\circ C$	-	5	-	ns
t_r	rise time		-	10	-	ns
$t_{d(off)}$	turn-off delay time		-	17	-	ns
t_f	fall time		-	3	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 0.7 A$; $V_{GS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	0.86	1.2	V

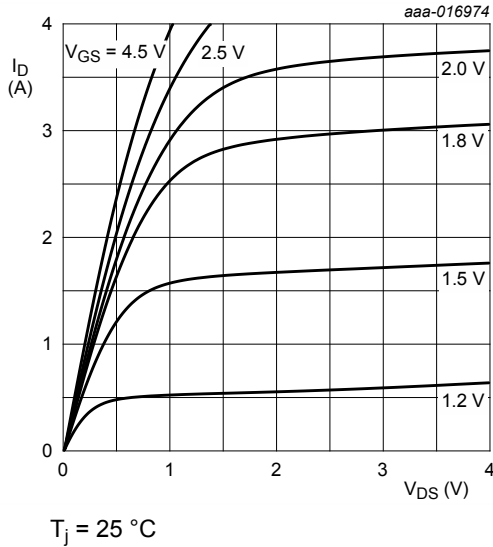


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

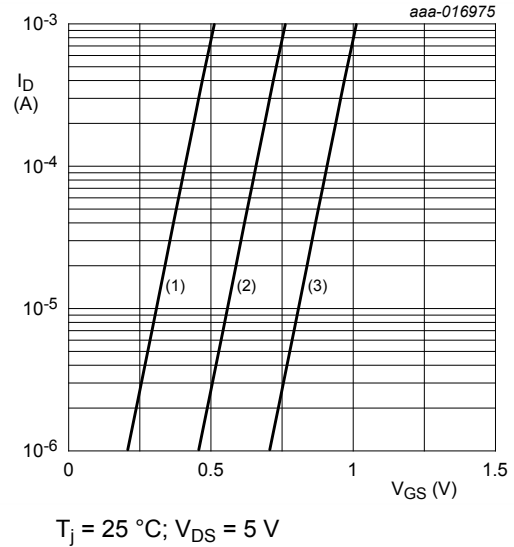


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

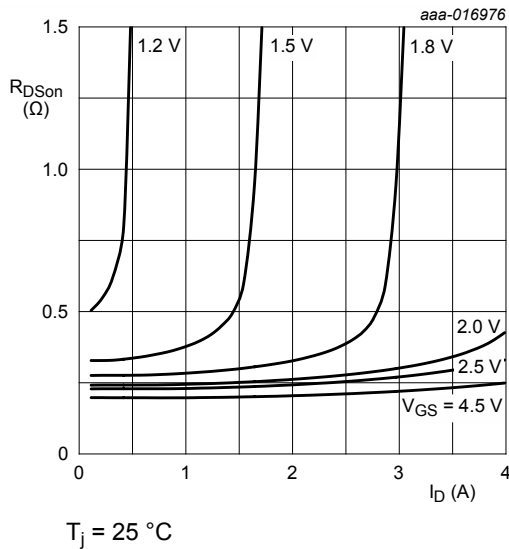


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

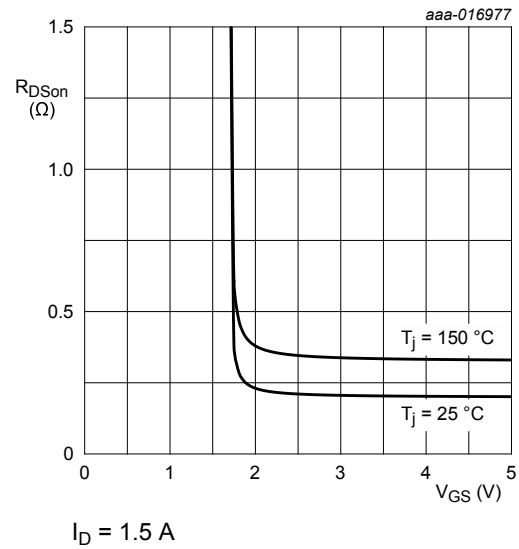
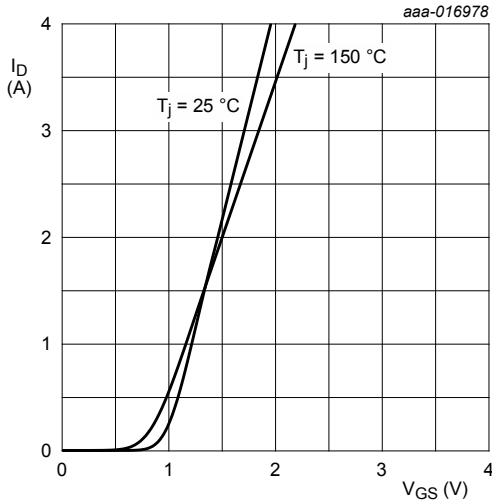


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values



$$V_{DS} > I_D \times R_{DSon}$$

Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

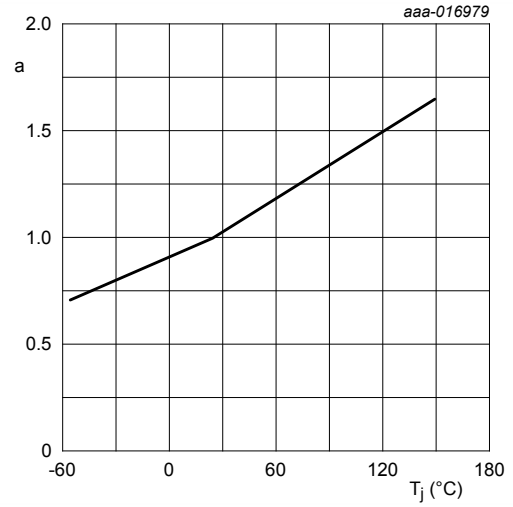
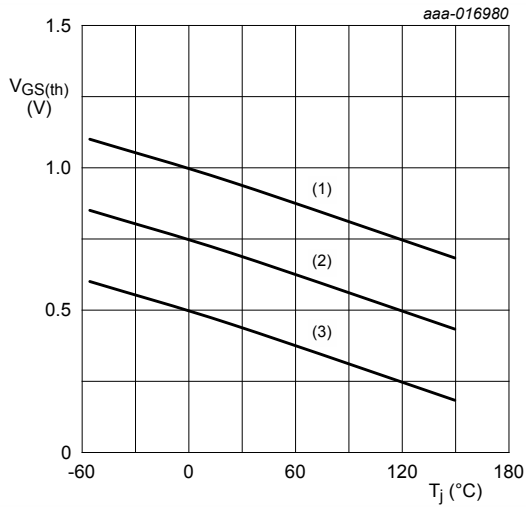


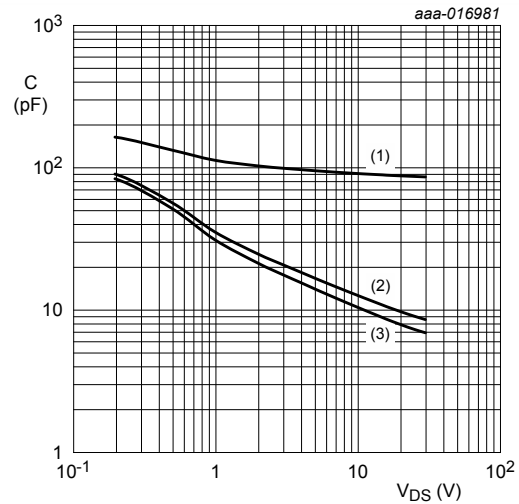
Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

$$a = \frac{R_{DSon}}{R_{DSon(25^\circ C)}}$$



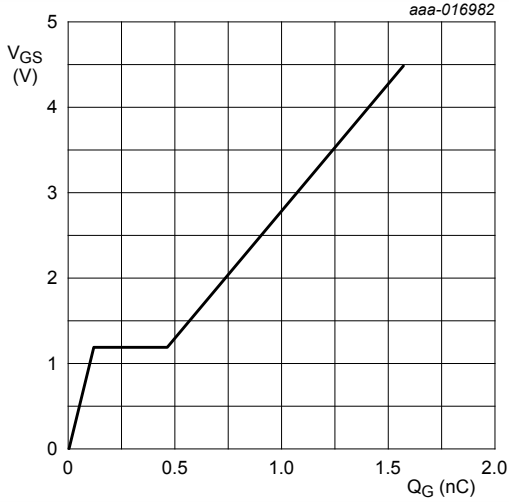
$I_D = 0.25 \text{ mA}; V_{DS} = V_{GS}$
 (1) maximum values
 (2) typical values
 (3) minimum values

Fig. 12. Gate-source threshold voltage as a function of junction temperature



$f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}$
 (1) C_{iss}
 (2) C_{oss}
 (3) C_{rss}

Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$I_D = 0.8 \text{ A}$; $V_{DS} = 15 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$

Fig. 14. Gate-source voltage as a function of gate charge; typical values

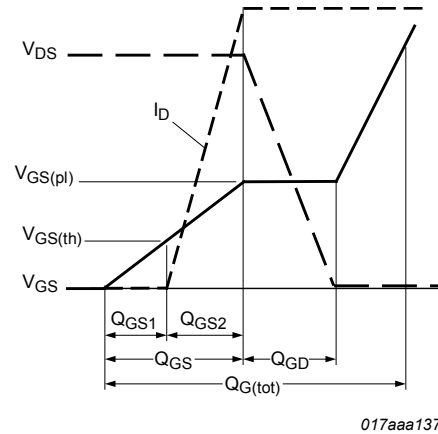
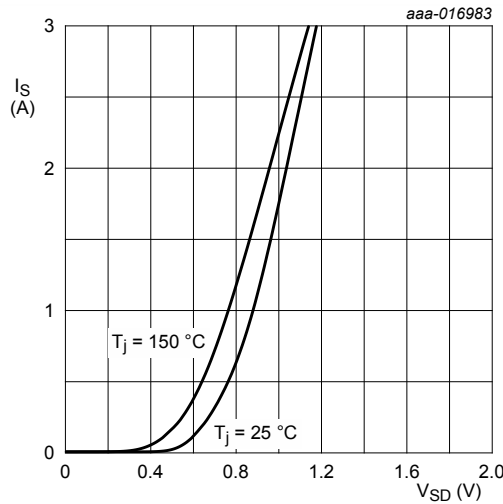


Fig. 15. MOSFET transistor: Gate charge waveform definitions



$V_{GS} = 0 \text{ V}$

Fig. 16. Source current as a function of source-drain voltage; typical values

11. Test information

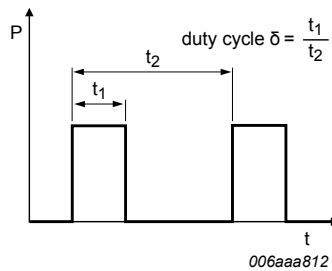


Fig. 17. Duty cycle definition

12. Package outline

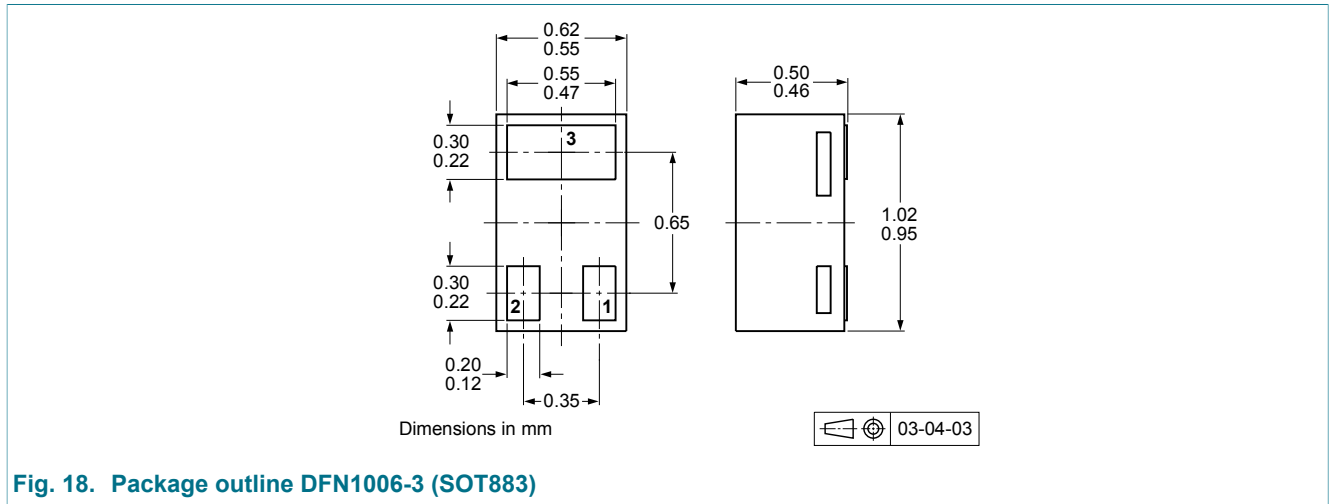


Fig. 18. Package outline DFN1006-3 (SOT883)

13. Soldering

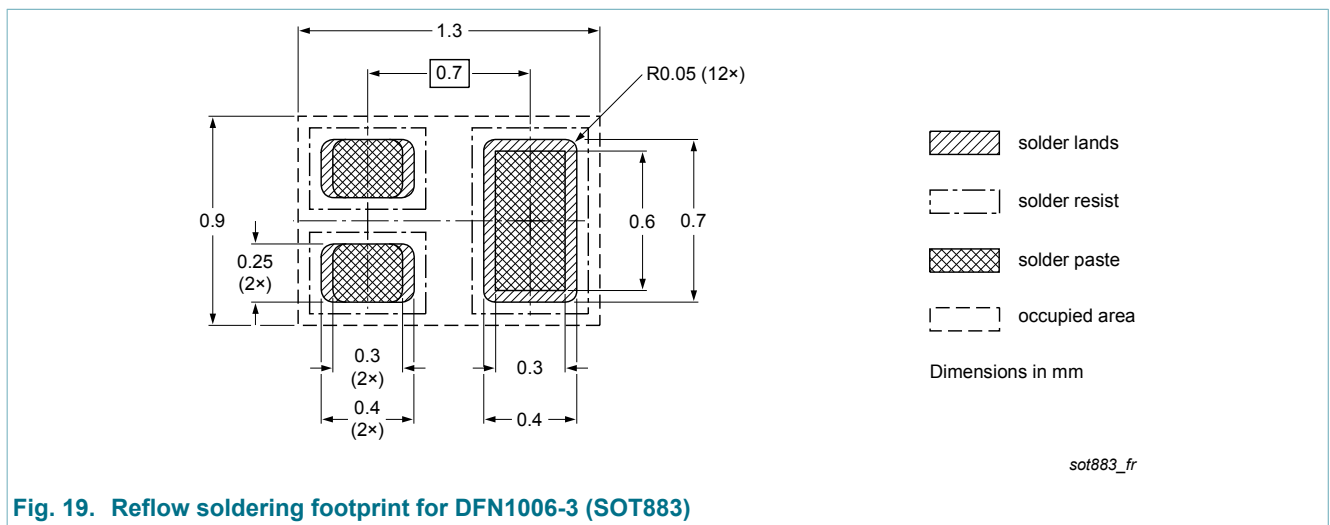


Fig. 19. Reflow soldering footprint for DFN1006-3 (SOT883)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMZ200UNE v.1	20150312	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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