



# PSMN011-60MS

N-channel 60 V 11.3 mΩ standard level MOSFET in LFPAK33

4 June 2013

Product data sheet

## 1. General description

Standard level enhancement mode N-channel MOSFET in LFPAK33 package. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

## 2. Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for standard level gate drive sources
- LFPAK33 package is footprint compatible with other 3.3mm types
- Qualified to 175 °C

## 3. Applications

- AC-to-DC converters
- Synchronous rectification
- DC-DC converters

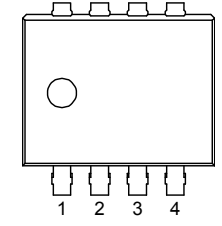
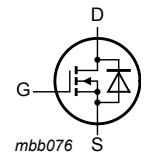
## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j = 25\text{ °C}$	-	-	60	V
$I_D$	drain current	$T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V};$ <a href="#">Fig. 1</a>	-	-	61	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C};$ <a href="#">Fig. 2</a>	-	-	91	W
$T_j$	junction temperature		-55	-	175	°C
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 15\text{ A}; T_j = 25\text{ °C};$ <a href="#">Fig. 12</a>	-	9.6	11.3	mΩ
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = 10\text{ V}; I_D = 15\text{ A}; V_{DS} = 30\text{ V};$ $T_j = 25\text{ °C};$ <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>	-	5.8	-	nC

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>LFAK33 (SOT1210)</p>	
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN011-60MS	LFAK33	Plastic single ended surface mounted package (LFAK33); 4 leads	SOT1210

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN011-60MS	M11S60

## 8. Limiting values

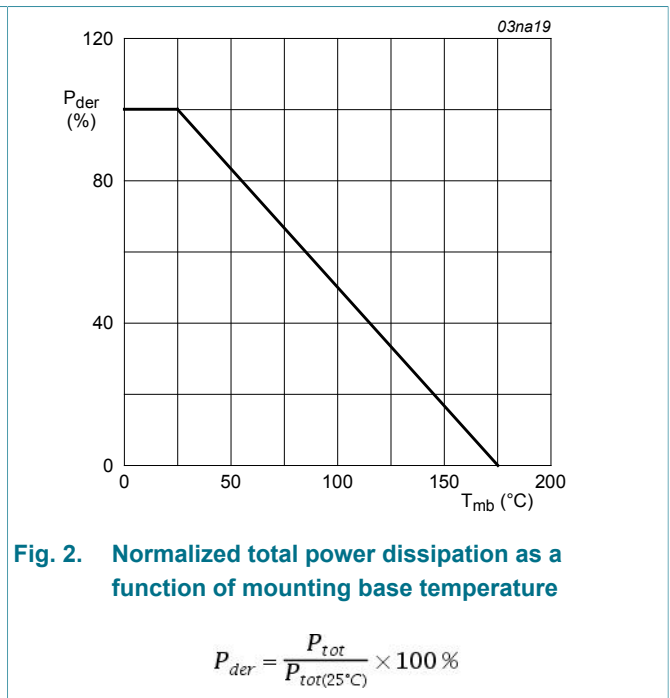
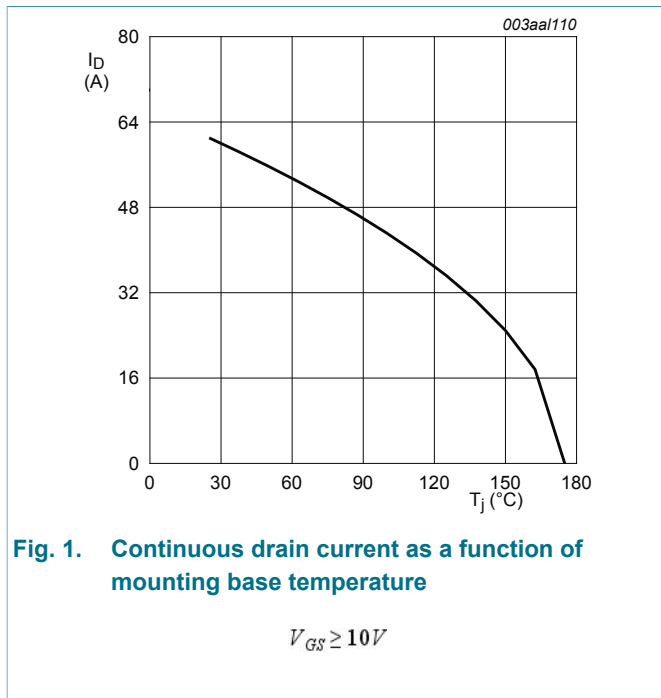
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j = 25\text{ °C}$	-	60	V
$V_{GS}$	gate-source voltage		-20	20	V
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 1</a>	-	61	A
		$V_{GS} = 10\text{ V}$ ; $T_{mb} = 100\text{ °C}$ ; <a href="#">Fig. 1</a>	-	43	A
$I_{DM}$	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 4</a>	-	244	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 2</a>	-	91	W
$T_{stg}$	storage temperature		-55	175	°C
$T_j$	junction temperature		-55	175	°C

Symbol	Parameter	Conditions		Min	Max	Unit
$T_{sld(M)}$	peak soldering temperature			-	260	°C
<b>Source-drain diode</b>						
$I_S$	source current	$T_{mb} = 25\text{ °C}$	[1]	-	70	A
$I_{SM}$	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$		-	244	A
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$ ; $T_{j(\text{init})} = 25\text{ °C}$ ; $I_D = 61\text{ A}$ ; $V_{sup} \leq 60\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; unclamped; <a href="#">Fig. 3</a>		-	48.1	mJ

[1] Continuous current is limited by package



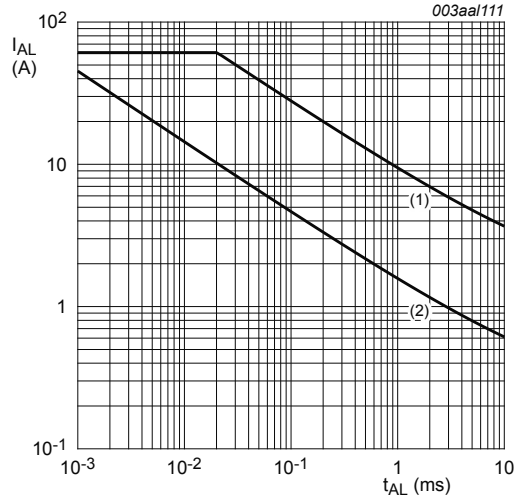


Fig. 3. Single pulse avalanche rating; avalanche current as a function of avalanche time

(1)  $T_{j (init)} = 25^{\circ}C$ ; (2)  $T_{j (init)} = 100^{\circ}C$

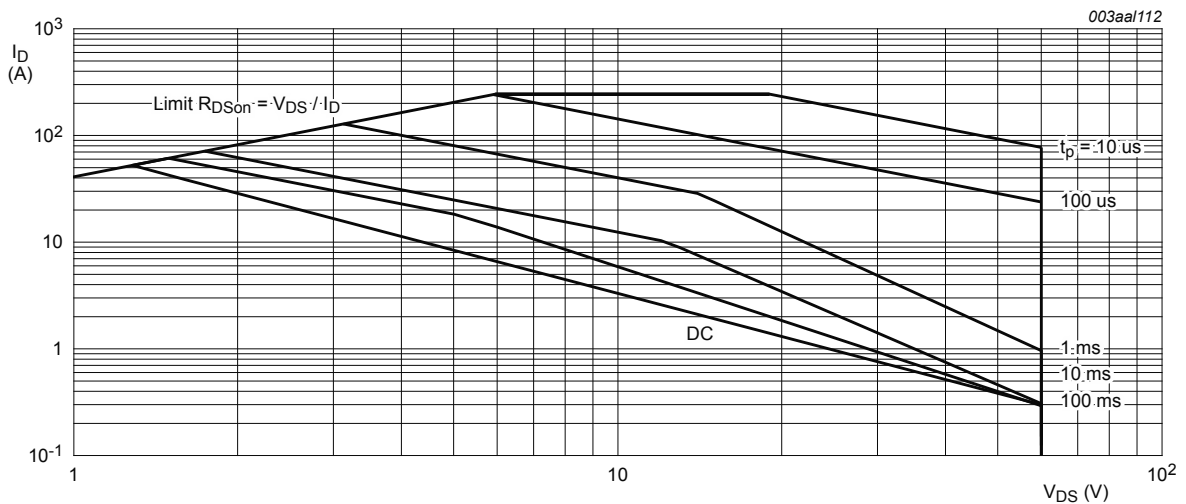


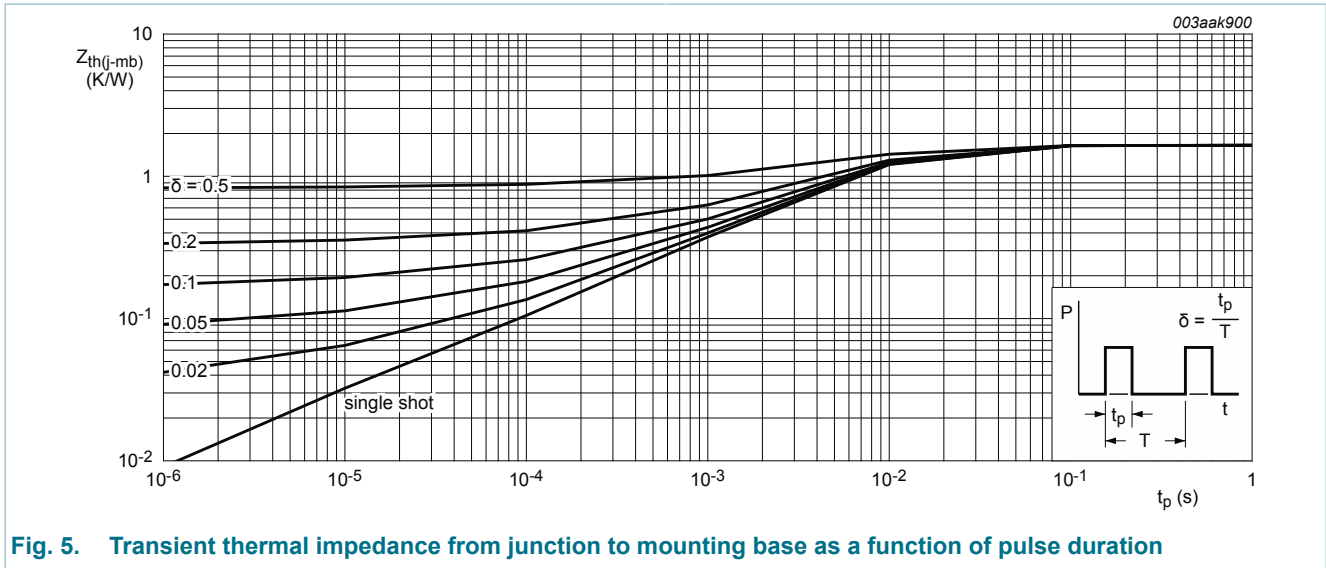
Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^{\circ}C$ ;  $I_{DM}$  is a single pulse

## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	<a href="#">Fig. 5</a>	-	1.44	1.65	K/W

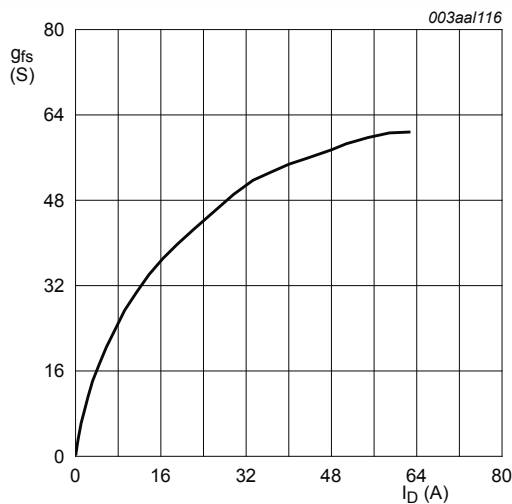


## 10. Characteristics

Table 7. Characteristics

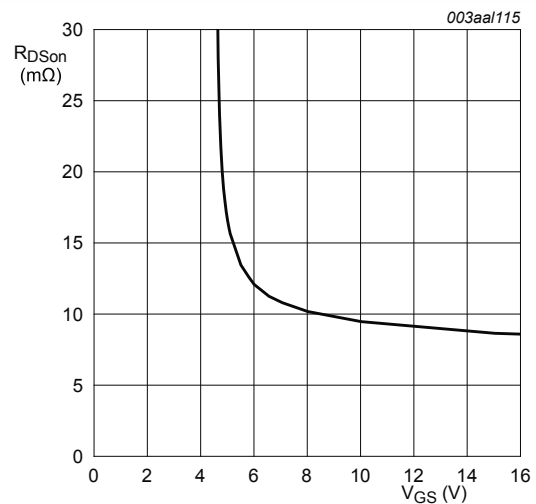
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	60	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	54	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C$ ; <a href="#">Fig. 10</a>	1	-	-	V
$V_{GSth}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$ ; <a href="#">Fig. 10</a> ; <a href="#">Fig. 11</a>	2.3	3	4	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C$ ; <a href="#">Fig. 10</a>	-	-	4.6	V
$I_{DSS}$	drain leakage current	$V_{DS} = 60 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.054	1	$\mu A$
		$V_{DS} = 60 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ C$	-	-	500	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	-	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	-	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 25 \text{ }^\circ C$ ; <a href="#">Fig. 12</a>	-	9.6	11.3	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 175 \text{ }^\circ C$ ; <a href="#">Fig. 13</a>	-	-	24.4	mΩ
$R_G$	gate resistance	$f = 1 \text{ MHz}$	-	2.75	-	Ω
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 15 \text{ A}; V_{DS} = 30 \text{ V}; V_{GS} = 10 \text{ V}; T_j = 25 \text{ }^\circ C$ ; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>	-	23	-	nC

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$Q_{GS}$	gate-source charge	$I_D = 15\text{ A}; V_{DS} = 30\text{ V}; V_{GS} = 10\text{ V};$ $T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>	-	6.1	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	3.9	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	2.2	-	nC
$Q_{GD}$	gate-drain charge		-	5.8	-	nC
$C_{iss}$	input capacitance	$V_{DS} = 30\text{ V}; V_{GS} = 0\text{ V}; f = 1\text{ MHz};$ $T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 16</a>	-	1368	-	pF
$C_{oss}$	output capacitance		-	191	-	pF
$C_{rss}$	reverse transfer capacitance		-	108	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30\text{ V}; R_L = 2\text{ }^\Omega; V_{GS} = 10\text{ V};$ $R_{G(ext)} = 5\text{ }^\Omega; T_j = 25\text{ }^\circ\text{C}$	-	6.7	-	ns
$t_r$	rise time		-	8.46	-	ns
$t_{d(off)}$	turn-off delay time		-	16.9	-	ns
$t_f$	fall time		-	9.18	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 15\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 17</a>	-	0.84	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 15\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$	-	21.7	-	ns
$Q_r$	recovered charge	$V_{DS} = 30\text{ V}; T_j = 25\text{ }^\circ\text{C}$	-	19.2	-	nC



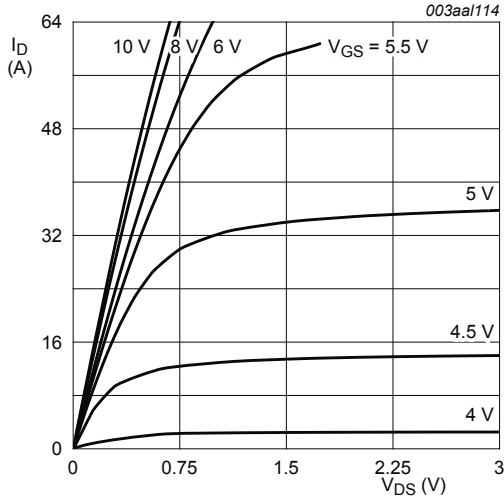
**Fig. 6. Forward transconductance as a function of drain current; typical values**

$T_j = 25^\circ\text{C}; V_{DS} = 10\text{V}$



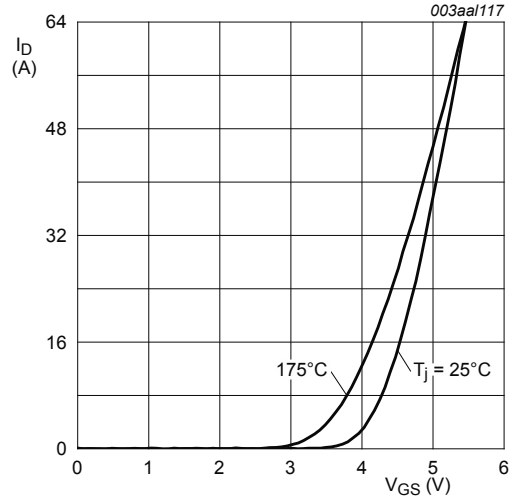
**Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values**

$T_j = 25^\circ\text{C}; I_D = 15\text{A}$



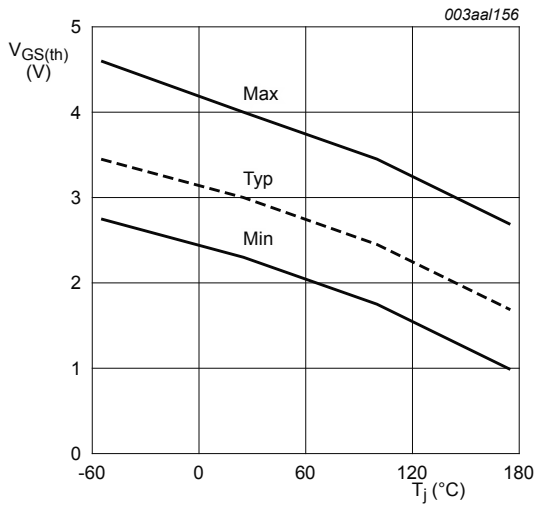
$T_j = 25\text{ }^\circ\text{C}; t_p = 300\text{ }\mu\text{s}$

**Fig. 8. Output characteristics; drain current as a function of drain-source voltage; typical values**



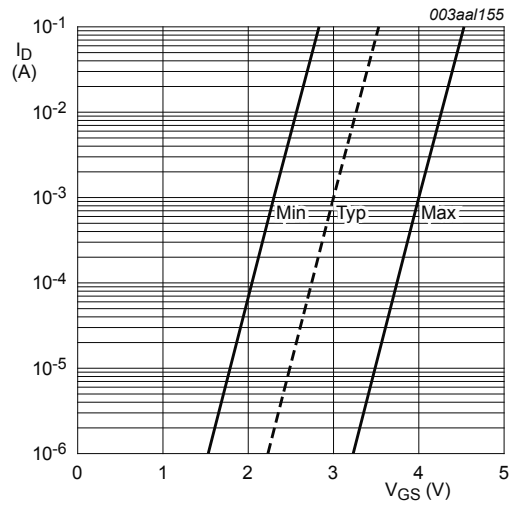
$V_{DS} = 10\text{ V}$

**Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values**



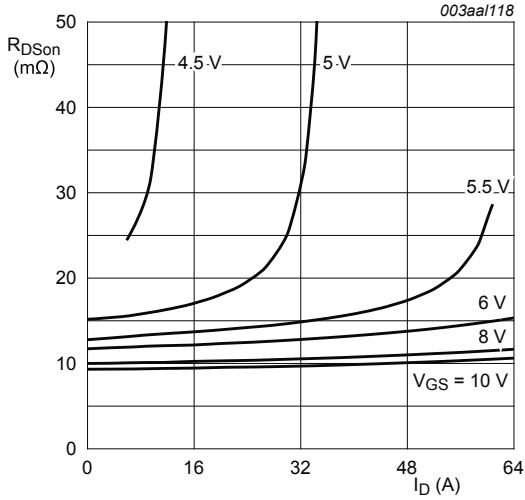
**Fig. 10. Gate-source threshold voltage as a function of junction temperature**

$I_D = 1\text{ mA}; V_{DS} = V_{GS}$



$T_j = 25\text{ }^\circ\text{C}; V_{DS} = 5\text{ V}$

**Fig. 11. Sub-threshold drain current as a function of gate-source voltage**



$T_j = 25^\circ\text{C}; t_p = 300 \mu\text{s}$

Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

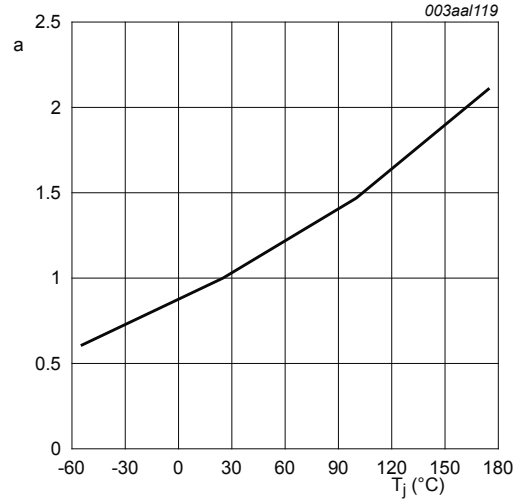


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DS(on)}}{R_{DS(on)}(25^\circ\text{C})}$$

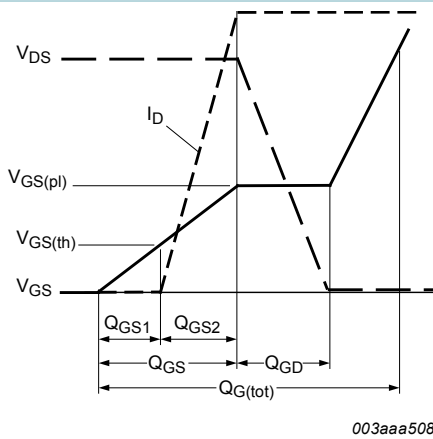


Fig. 14. Gate charge waveform definitions

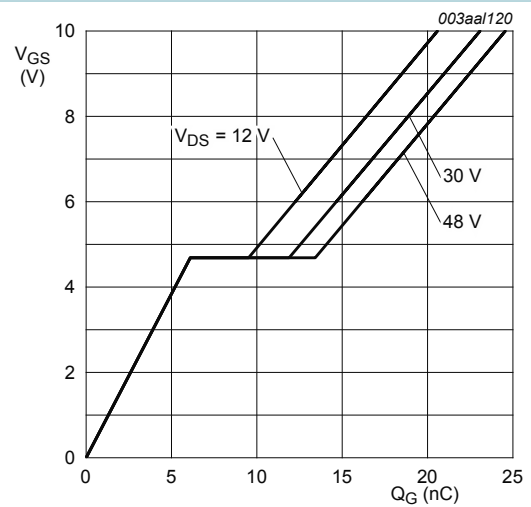
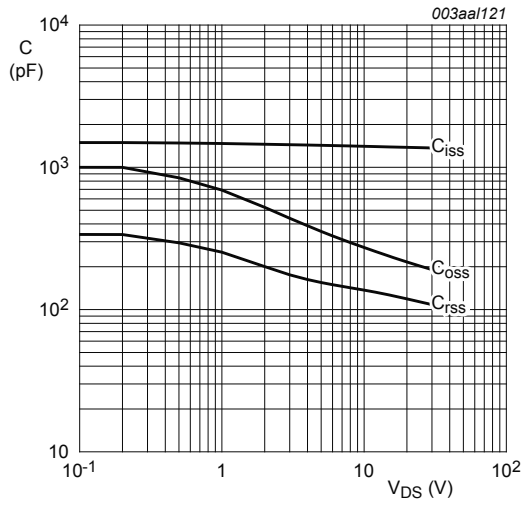


Fig. 15. Gate-source voltage as a function of gate charge; typical values

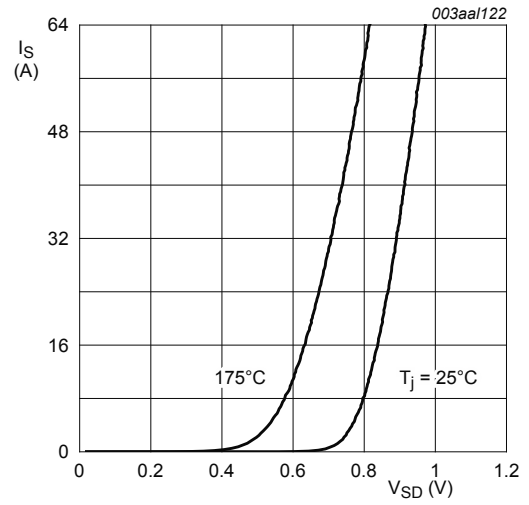
$T_j = 25^\circ\text{C}; I_D = 15\text{ A}$





**Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**

$$V_{GS} = 0V; f = 1MHz$$



**Fig. 17. Source current as a function of source-drain voltage; typical values**

$$V_{GS} = 0V$$

### 11. Package outline

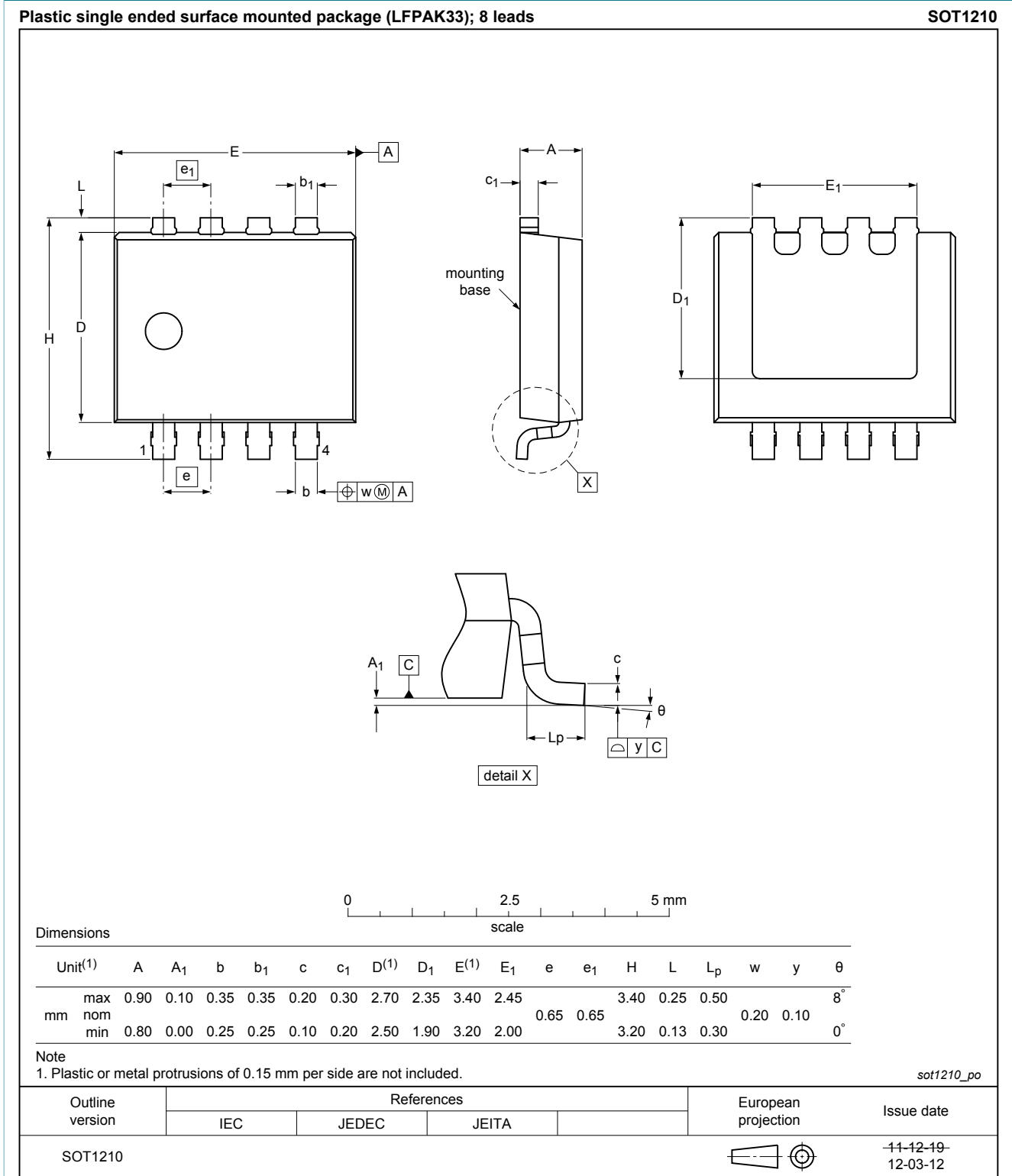


Fig. 18. Package outline LPAK33 (SOT1210)

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