PSMN012-60HL

N-channel 60 V, 12.5 mOhm, logic level MOSFET in LFPAK56D using TrenchMOS technology enhanced for repetitive avalanche

30 September 2022 **Product data sheet**

1. General description

Dual logic level N-channel MOSFET in an LFPAK56D (Dual Power-SO8) package, using application specific (ASFET) repetitive avalanche silicon technology.

2. Features and benefits

- High reliability LFPAK56D package, copper-clip, solder die attach and qualified to 175 °C
- Tested to 1 Bn avalanche events
- LFPAK copper clip package technology
- Copper-clip, solder die attach
- High robustness and reliability

3. Applications

- Brushless DC and Brushed DC motor control
- DC-to-DC converters
- High-performance synchronous rectification

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	-	60	V
I_D	drain current	V_{GS} = 5 V; T_{mb} = 25 °C; Fig. 2		-	-	40	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	64	W
T_j	junction temperature			-55	-	175	°C
Static characteristics FET1 and FET2							
R_{DSon}	drain-source on-state resistance	V_{GS} = 5 V; I_D = 10 A; T_j = 25 °C; Fig. 14		6.1	10	12.5	mΩ
		V_{GS} = 5 V; I_D = 10 A; T_j = 175 °C; Fig. 14; Fig. 15		-	22	28.3	mΩ
Dynamic characteristics FET1 and FET2							
Q_{GD}	gate-drain charge	I_D = 10 A; V_{DS} = 48 V; V_{GS} = 5 V; T_j = 25 °C; Fig. 16; Fig. 17		-	7.9	-	nC
$Q_{G(tot)}$	total gate charge			-	22.4	-	nC
Avalanche Ruggedness FET1 and FET2							
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 40 A; V_{sup} ≤ 60 V; R_{GS} = 50 Ω; V_{GS} = 5 V; $T_{j(init)}$ = 25 °C; unclamped; Fig. 7	[1] [2]	-	-	82	mJ

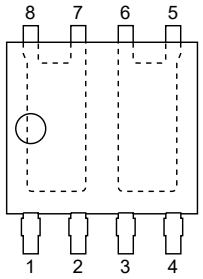
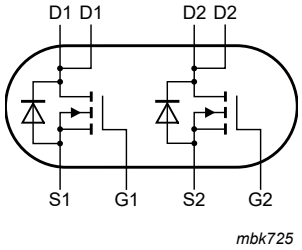
nexperia

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Source-drain diode FET1 and FET2							
Q_r	recovered charge	I_S = 10 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 30 V; T_j = 25 °C		-	18.9	-	nC

[1] Refer to application note AN10273 for further information
[2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	 **LFPAK56D; Dual LFPAK (SOT1205)**	
2	G1	gate1		
3	S2	source2		
4	G2	gate2		
5	D2	drain2		
6	D2	drain2		
7	D1	drain1		
8	D1	drain1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN012-60HL	LFPAK56D; Dual LFPAK	plastic, single ended surface mounted package (LFPAK56D); 8 leads	SOT1205

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN012-60HL	12RL60H

8. Limiting values

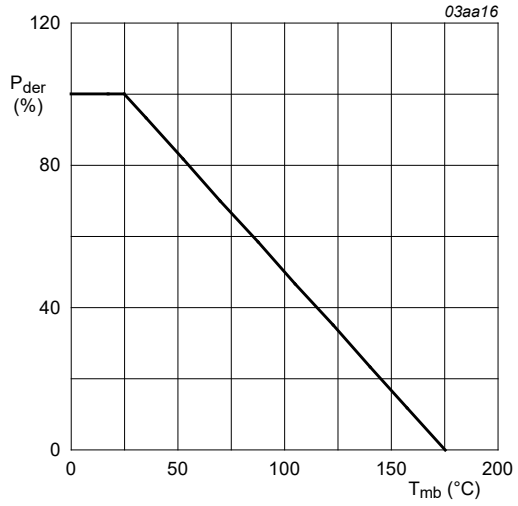
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	60	V
V_{DGR}	drain-gate voltage	R_{GS} = 20 kΩ		-	60	V
V_{GS}	gate-source voltage	DC; T_j ≤ 175 °C		-10	10	V
		Pulsed; T_j ≤ 175 °C	[1] [2]	-15	15	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	64	W

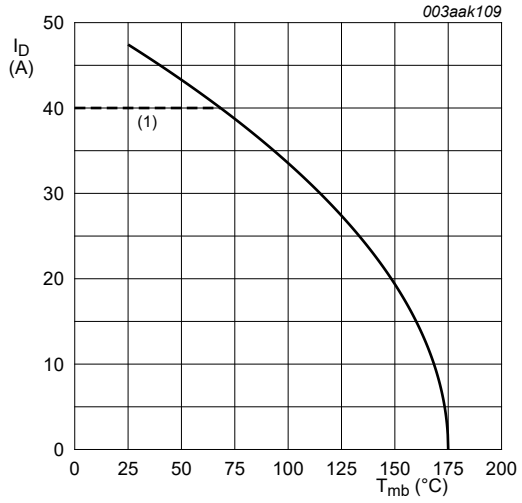
Symbol	Parameter	Conditions		Min	Max	Unit
I_D	drain current	V_{GS} = 5 V; T_{mb} = 25 °C; Fig. 2		-	40	A
		V_{GS} = 5 V; T_{mb} = 100 °C; Fig. 2		-	33	A
I_{DM}	peak drain current	pulsed; $t_p \leq$ 10 µs; T_{mb} = 25 °C; Fig. 3		-	190	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
I_S	source current	T_{mb} = 25 °C		-	40	A
I_{SM}	peak source current	pulsed; $t_p \leq$ 10 µs; T_{mb} = 25 °C		-	190	A
Avalanche ruggedness						
$E_{DS(AL)R}$	repetitive drain-source avalanche energy	I_D = 1.92 A; $V_{sup} \leq$ 60 V; R_{GS} = 10 Ω; V_{GS} =10 V; $T_{j(rise)} \leq$ 30 °C; unclamped; Fig. 4; Fig. 5; Fig. 6	[3] [4] [5]	-	75.2	mJ
Avalanche Ruggedness FET1 and FET2						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 40 A; $V_{sup} \leq$ 60 V; R_{GS} = 50 Ω; V_{GS} = 5 V; $T_{j(init)}$ = 25 °C; unclamped; Fig. 7	[6] [7]	-	82	mJ

[1] Accumulated Pulse duration up to 50 hours delivers zero defect ppm
[2] Significantly longer life times are achieved by lowering T_j and or V_{GS}.
[3] Repetitive avalanche rating is limited by maximum junction temperature of 175 °C and junction rise of 30 °C
[4] Refer to Fig. 5 for the limiting number of avalanche events
[5] Refer to Fig. 6 Rdson at Vgs=5V will increase as a function of repetitive avalanche cycles
[6] Refer to application note AN10273 for further information
[7] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C



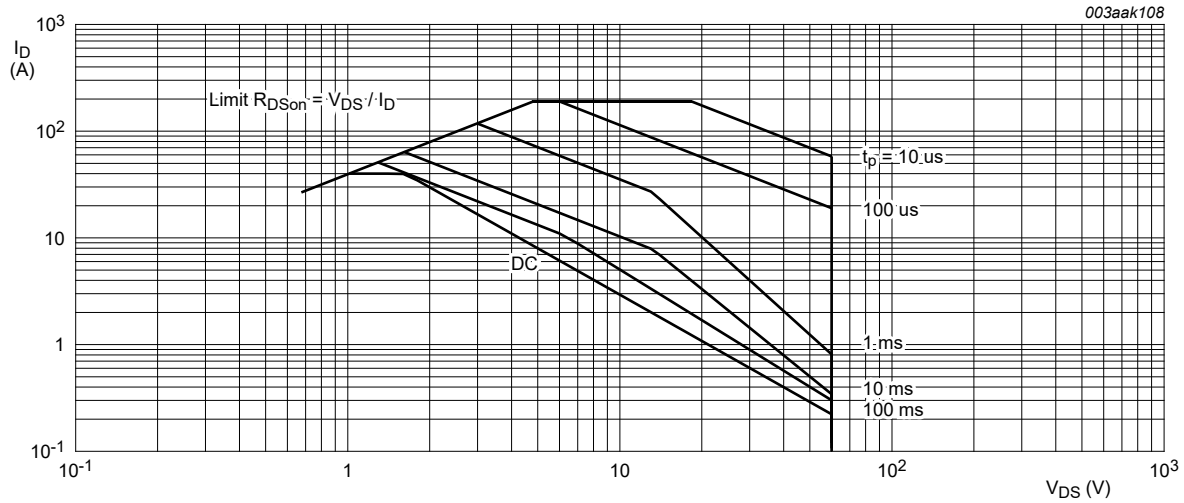
$$P_{der} = \frac{P_{tot}}{P_{tot\,(25\,°C)}} \times 100\,\%$$

Fig. 1. Normalized total power dissipation as a function of mounting base temperature



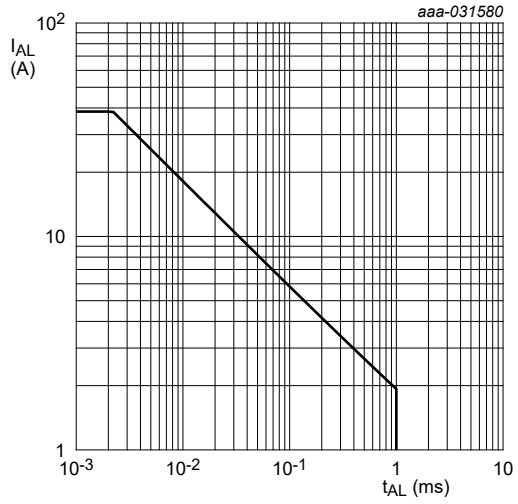
(1) Capped at 40 A due to package
VGS ≥ 5 V

Fig. 2. Continuous drain current as a function of mounting base temperature



T_{mb} = 25°C; I_{DM} is a single pulse

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



T_j is limited to 175 °C and $T_{j(rise)}$ is limited to 30 °C

Fig. 4. Repetitive avalanche rating; avalanche current as a function of avalanche time

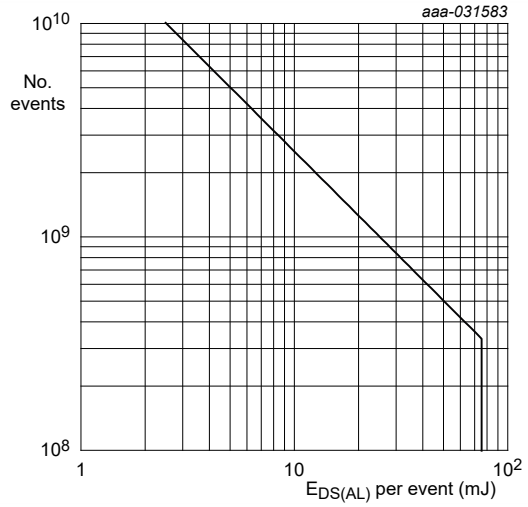


Fig. 5. Repetitive avalanche rating; maximum number of avalanche events as a function of avalanche energy

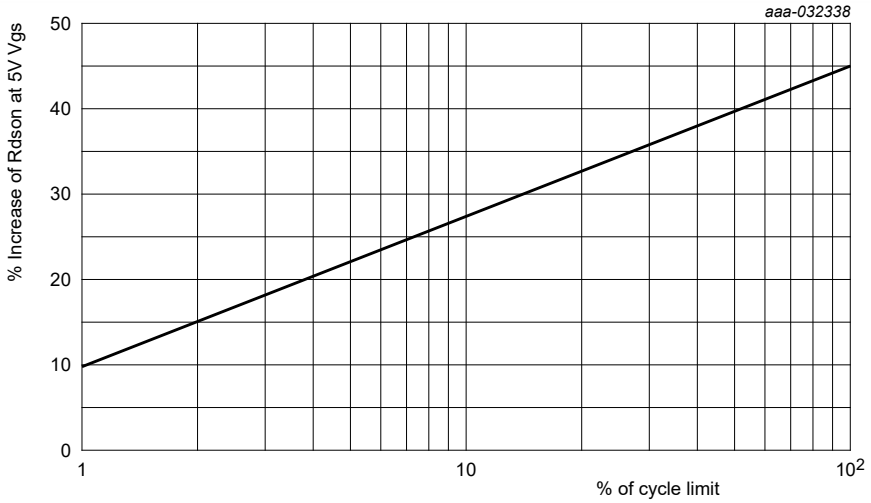
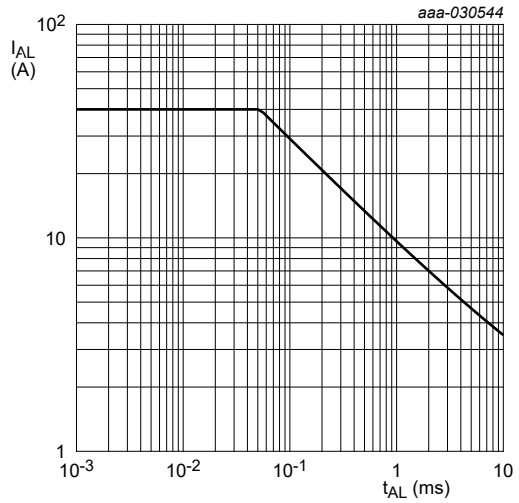


Fig. 6. Percentage Rdson at 5V increase as a function of avalanche cycles



$T_{j\ (init)}$ = 25 °C

Fig. 7. Single pulse avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j\text{-}mb)}$	thermal resistance from junction to mounting base	Fig. 8		-	-	2.36	K/W
$R_{th(j\text{-}a)}$	thermal resistance from junction to ambient	Minimum footprint; mounted on a printed circuit board		-	95	-	K/W

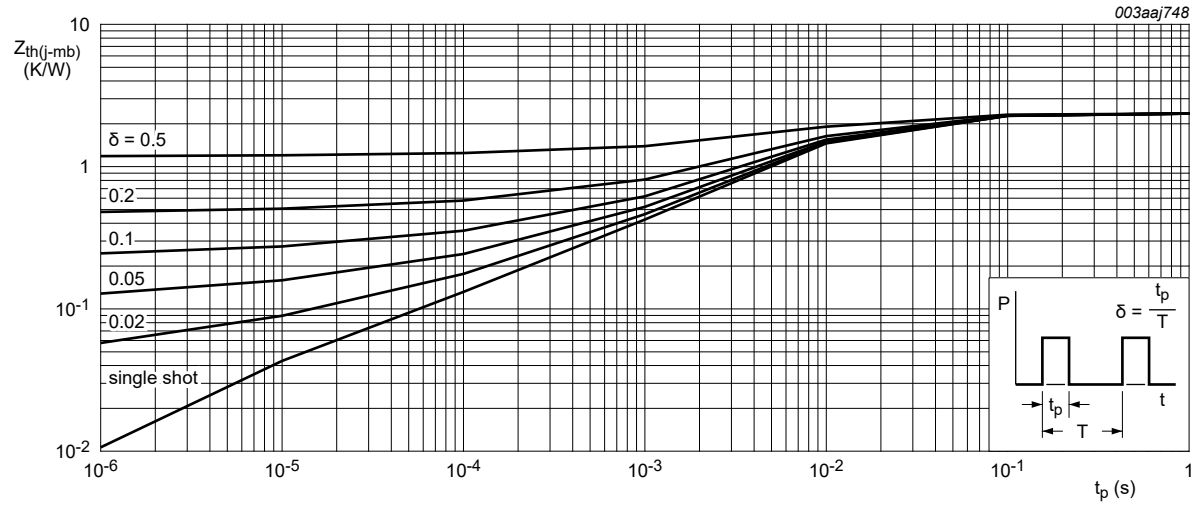
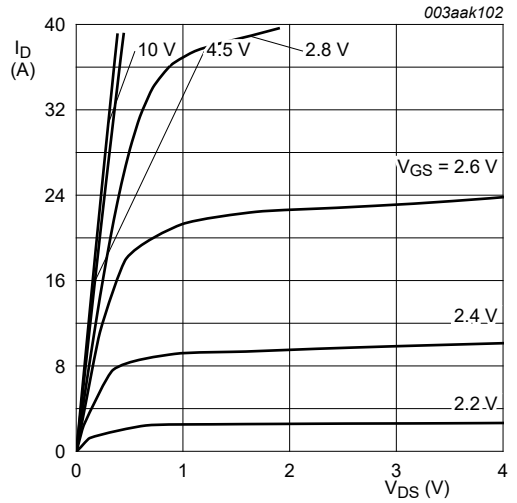


Fig. 8. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

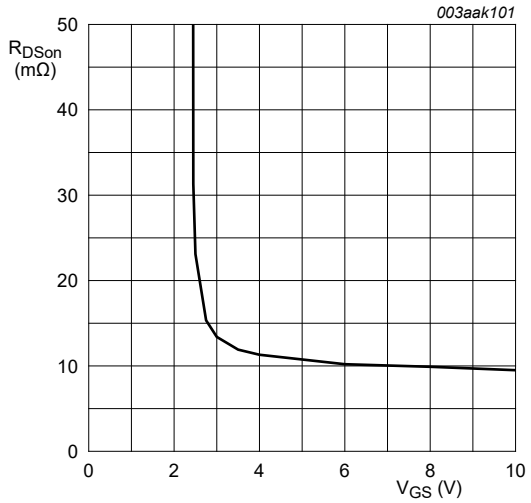
Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics FET1 and FET2							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C		54	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		60	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS}=V_{GS}; T_j = 25 °C; Fig. 12; Fig. 13		1.4	1.7	2.1	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = 175 °C; Fig. 12		0.5	-	-	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = -55 °C; Fig. 12		-	-	2.45	V
I_{DSS}	drain leakage current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 °C		-	0.02	1	µA
		V_{DS} = 60 V; V_{GS} = 0 V; T_j = 175 °C		-	-	500	µA
I_{GSS}	gate leakage current	V_{GS} = -10 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
		V_{GS} = 10 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 5 V; I_D = 10 A; T_j = 25 °C; Fig. 14		6.1	10	12.5	mΩ
		V_{GS} = 5 V; I_D = 10 A; T_j = 175 °C; Fig. 14; Fig. 15		-	22	28.3	mΩ
		V_{GS} = 10 V; I_D = 10 A; T_j = 25 °C; Fig. 14		5.4	9	11.2	mΩ
Dynamic characteristics FET1 and FET2							
$Q_{G(tot)}$	total gate charge	I_D = 10 A; V_{DS} = 48 V; V_{GS} = 5 V; T_j = 25 °C; Fig. 16; Fig. 17		-	22.4	-	nC
Q_{GS}	gate-source charge			-	5.2	-	nC
Q_{GD}	gate-drain charge			-	7.9	-	nC
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; Fig. 18		-	2215	2953	pF
C_{oss}	output capacitance			-	225	270	pF
C_{rss}	reverse transfer capacitance			-	116	159	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 48 V; R_L = 5 Ω; V_{GS} = 5 V; $R_{G(ext)}$ = 5 Ω; T_j = 25 °C		-	13	-	ns
t_r	rise time			-	22.1	-	ns
$t_{d(off)}$	turn-off delay time			-	30.5	-	ns
t_f	fall time			-	21.8	-	ns
Source-drain diode FET1 and FET2							
V_{SD}	source-drain voltage	I_S = 10 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 19		-	0.78	1.2	V
t_{rr}	reverse recovery time	I_S = 10 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 30 V; T_j = 25 °C		-	22.7	-	ns
Q_r	recovered charge			-	18.9	-	nC



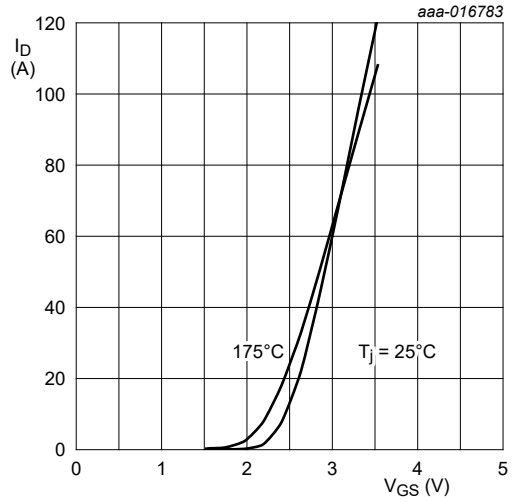
T_j = 25 °C; t_p = 300 µs

Fig. 9. Output characteristics; drain current as a function of drain-source voltage; typical values



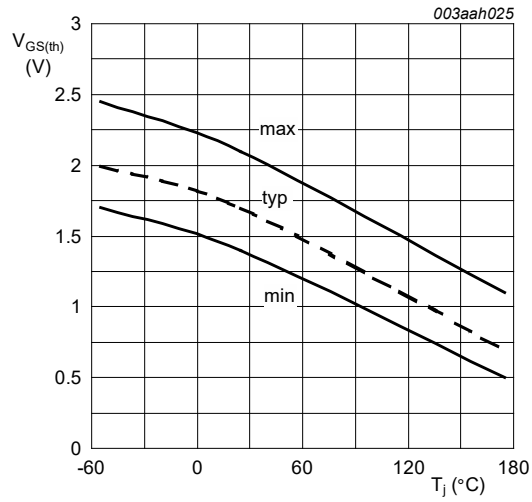
T_j = 25 °C; I_D = 10 A

Fig. 10. Drain-source on-state resistance as a function of gate-source voltage; typical values



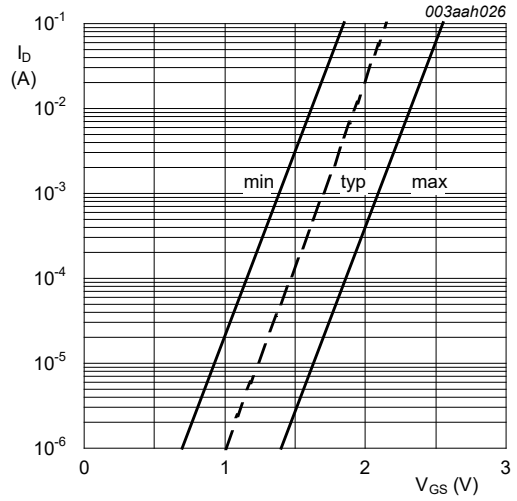
V_{DS} = 10 V

Fig. 11. Transfer characteristics; drain current as a function of gate-source voltage; typical values



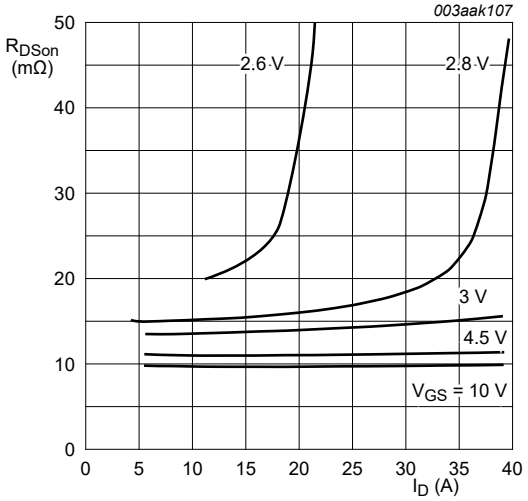
I_D = 1 mA; V_{DS} = V_{GS}

Fig. 12. Gate-source threshold voltage as a function of junction temperature



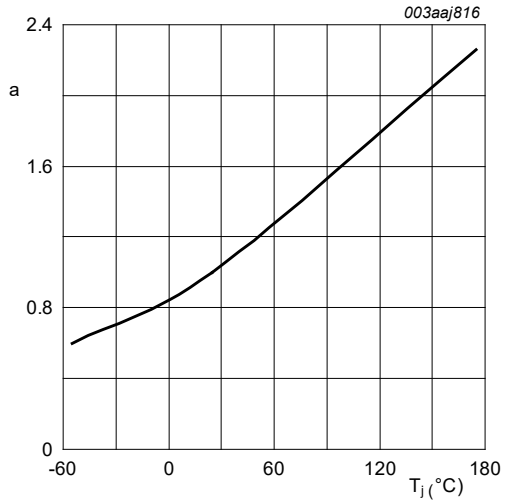
Tj = 25 °C; VDS = 5 V

Fig. 13. Sub-threshold drain current as a function of gate-source voltage



T_j = 25 °C; t_p = 300 µs

Fig. 14. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon\ (25°C)}}$$

Fig. 15. Normalized drain-source on-state resistance factor as a function of junction temperature

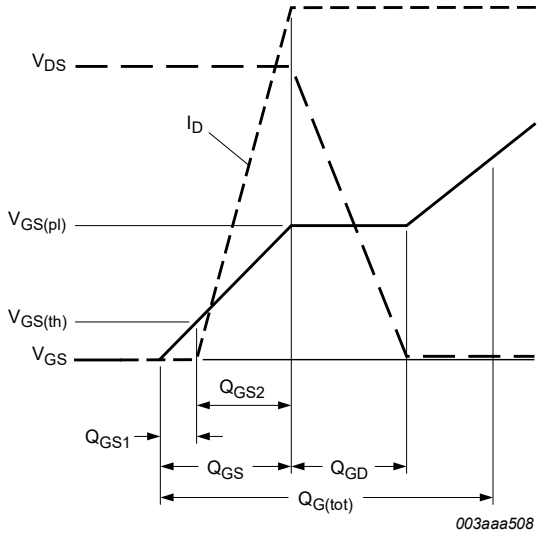
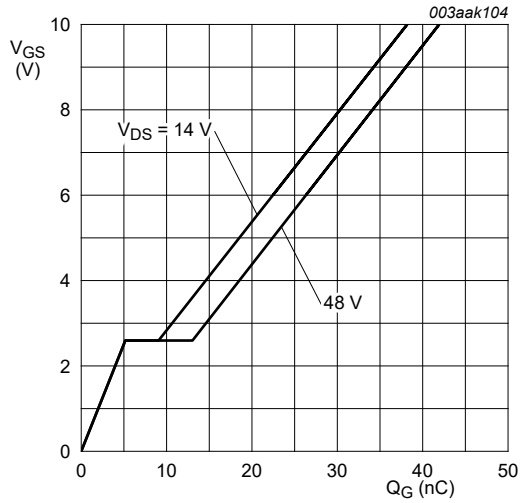
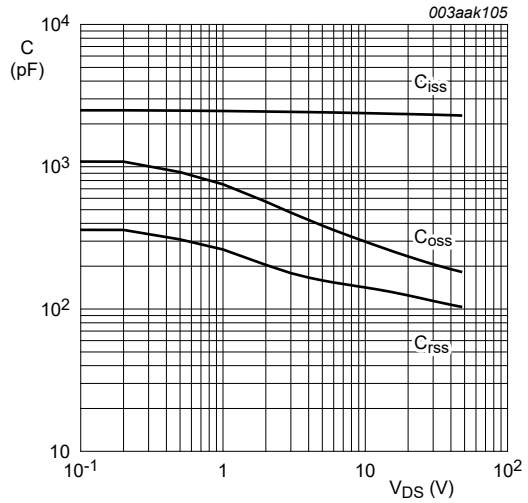


Fig. 16. Gate charge waveform definitions



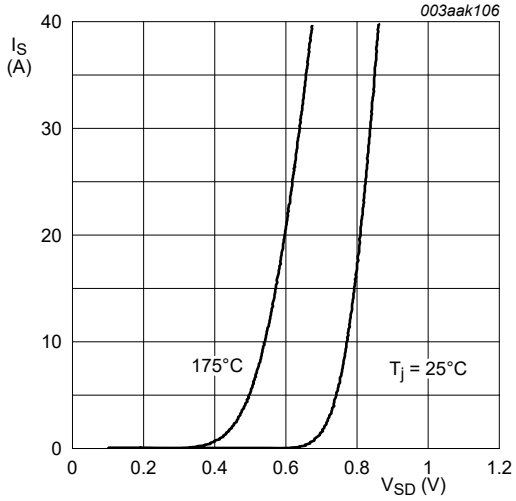
T_j = 25 °C; I_D = 10 A

Fig. 17. Gate-source voltage as a function of gate charge; typical values



V_{GS} = 0 V; f = 1 MHz

Fig. 18. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

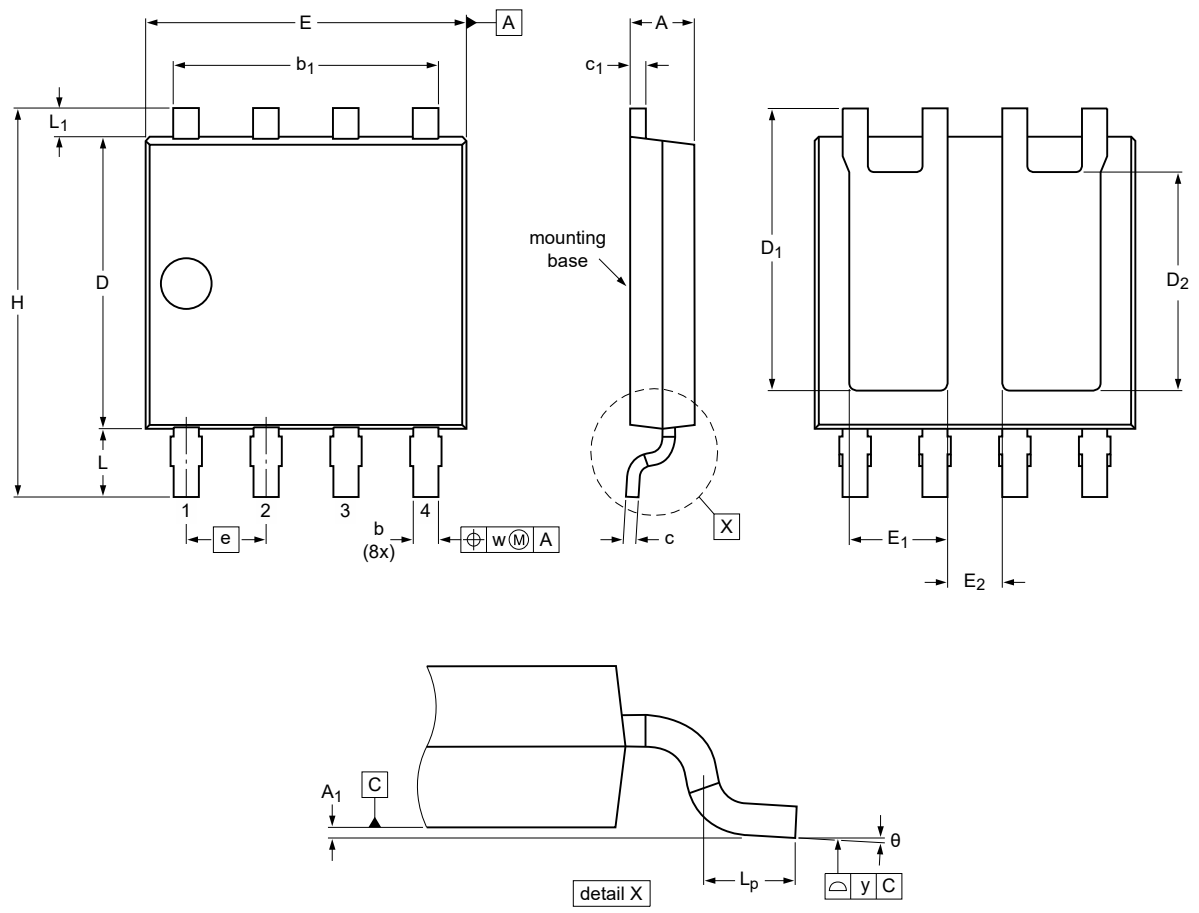


V_{GS} = 0 V

Fig. 19. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

11. Package outline

Plastic single ended surface mounted package LFPAK56D; 8 leads **SOT1205**



Dimensions

Unit		A	A_1	b	b_1	c	c_1	$D^{(1)}$	$D_1{}^{(1)}$	D_2 (ref)	$E^{(1)}$	$E_1{}^{(1)}$	E_2	e	H	L	L_1	L_p	w	y	θ
mm	max	1.05	0.1	0.50	4.4	0.25	0.30	4.70	4.55	3.5	5.30	1.8	0.85		6.2	1.3	0.55	0.85			8°
	nom													1.27					0.25	0.1	
	min	1.02	0.0	0.35	4.1	0.19	0.24	4.45	4.35	3.4	4.95	1.6	0.60		5.9	0.8	0.30	0.40			0°

Note
1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

sot1205_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1205						~~14-08-21~~ 14-10-28

Fig. 20. Package outline LFPAK56D; Dual LFPAK (SOT1205)

12. Soldering

Footprint information for reflow soldering of LFPAK56D package **SOT1205**

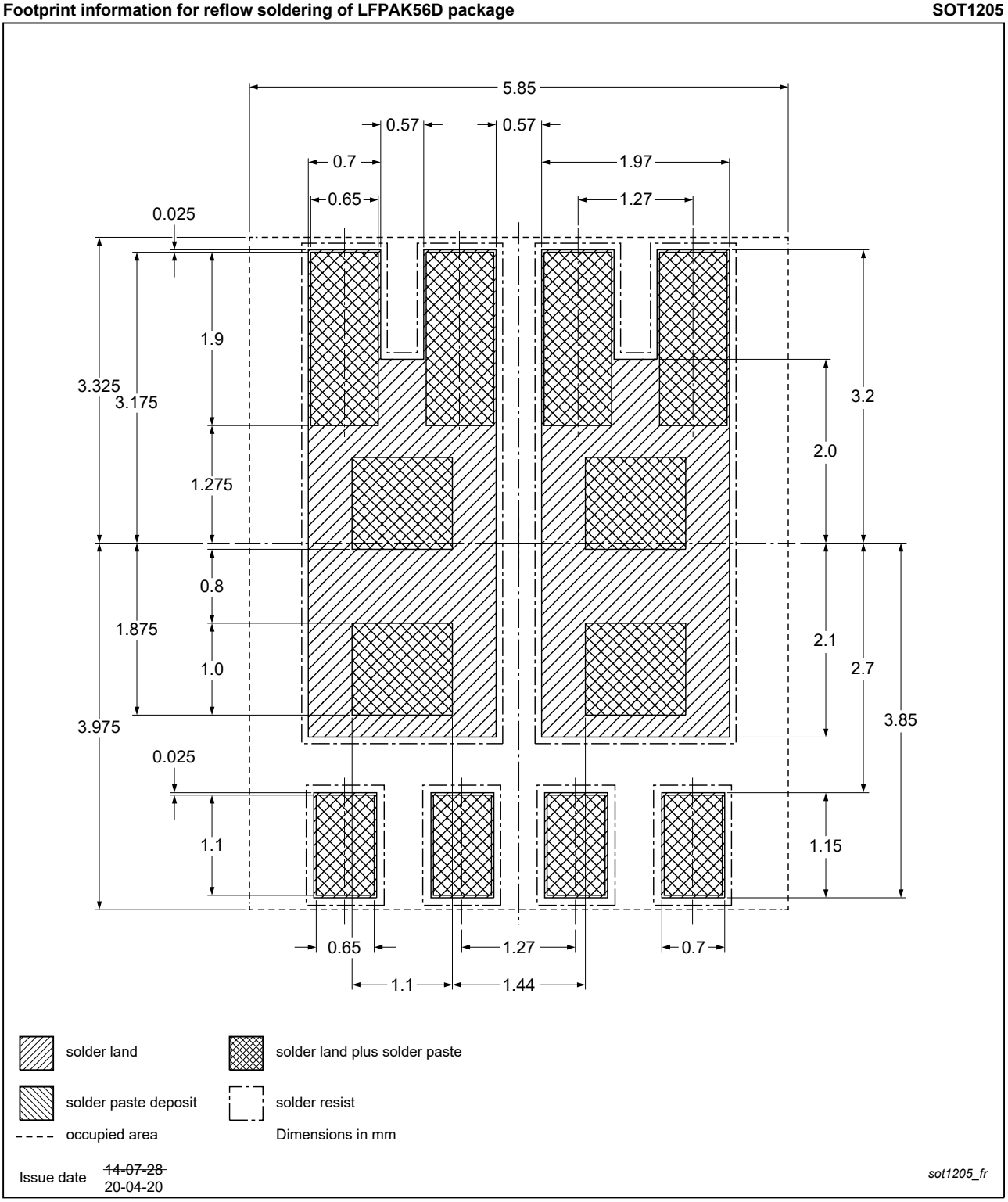


Fig. 21. Reflow soldering footprint for LFPAK56D; Dual LFPAK (SOT1205)

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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