



# PSMN018-80YS

N-channel LFPAK 80 V 18 mΩ standard level MOSFET

Rev. 02 — 28 October 2010

Product data sheet

## 1. Product profile

### 1.1 General description

Standard level N-channel MOSFET in LFPAK package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

### 1.2 Features and benefits

- Advanced TrenchMOS provides low RDSon and low gate charge
- High efficiency gains in switching power converters
- Improved mechanical and thermal characteristics
- LFPAK provides maximum power density in a Power SO8 package

### 1.3 Applications

- DC-to-DC converters
- Lithium-ion battery protection
- Load switching
- Motor control
- Server power supplies

### 1.4 Quick reference data

Table 1. Quick reference data

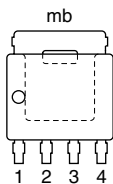
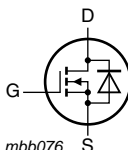
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	-	80	V
$I_D$	drain current	$T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V};$ see <a href="#">Figure 1</a>	-	-	45	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C};$ see <a href="#">Figure 2</a>	-	-	89	W
$T_j$	junction temperature		-55	-	175	°C
<b>Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 5\text{ A};$ $T_j = 100\text{ °C};$ see <a href="#">Figure 12</a>	-	-	28	mΩ
		$V_{GS} = 10\text{ V}; I_D = 5\text{ A};$ $T_j = 25\text{ °C};$ see <a href="#">Figure 12</a> ; see <a href="#">Figure 13</a>	-	15	18	mΩ

Table 1. Quick reference data ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = 10\text{ V}$ ; $I_D = 25\text{ A}$ ;	-	6	-	nC
$Q_{G(\text{tot})}$	total gate charge	$V_{DS} = 40\text{ V}$ ; see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>	-	26	-	nC
<b>Avalanche ruggedness</b>						
$E_{DS(\text{AL})S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$ ; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$ ; $I_D = 45\text{ A}$ ; $V_{\text{sup}} \leq 80\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; unclamped	-	-	64	mJ

## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

**SOT669 (LPAK)**

## 3. Ordering information

Table 3. Ordering information

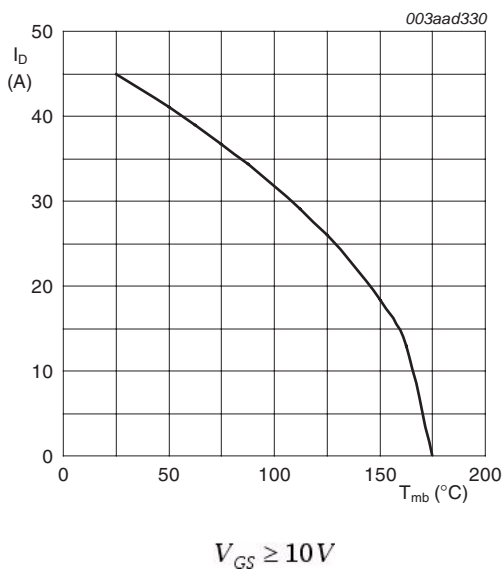
Type number	Package		Version
	Name	Description	
PSMN018-80YS	LPAK	plastic single-ended surface-mounted package (LPAK); 4 leads	SOT669

## 4. Limiting values

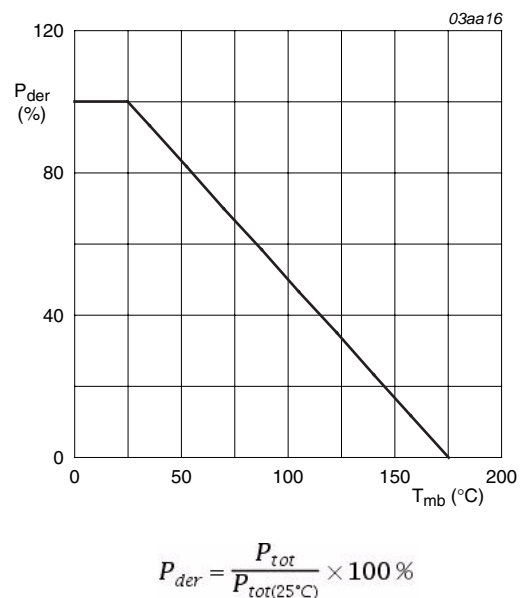
**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

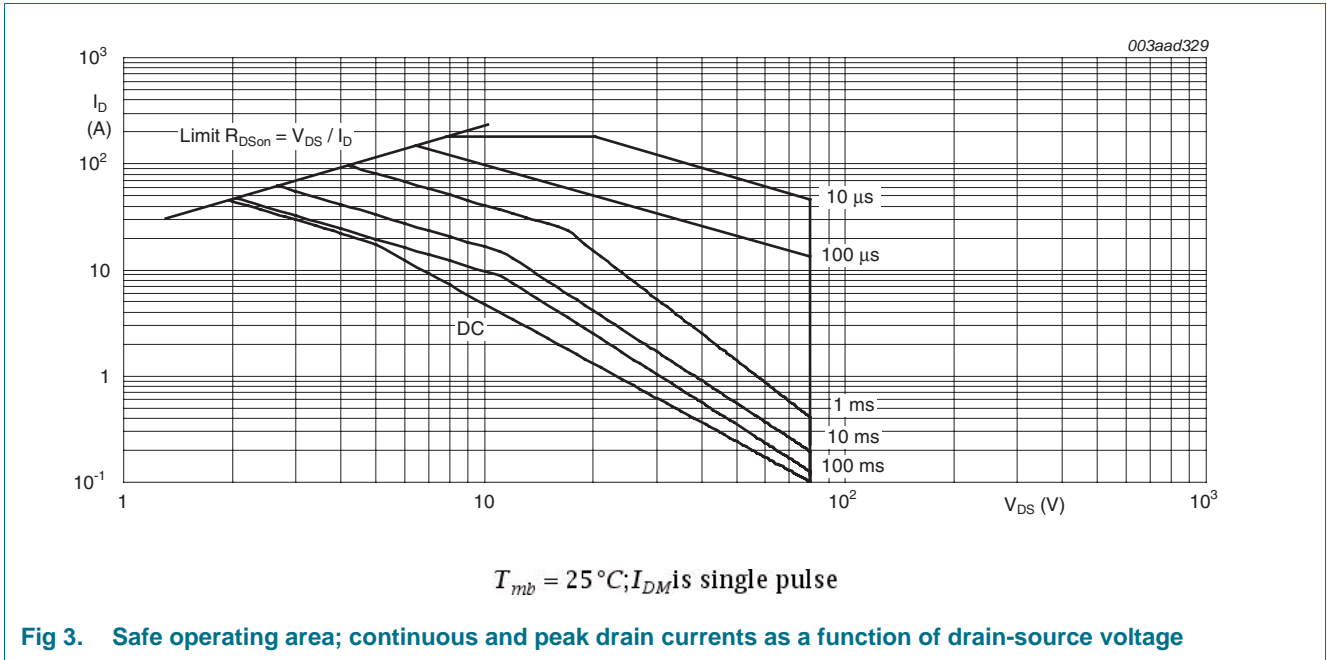
Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$	-	80	V
$V_{DGR}$	drain-gate voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$	-	80	V
$V_{GS}$	gate-source voltage		-20	20	V
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 100\text{ °C}$ ; see <a href="#">Figure 1</a>	-	32	A
		$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 1</a>	-	45	A
$I_{DM}$	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 3</a>	-	182	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	-	89	W
$T_{stg}$	storage temperature		-55	175	°C
$T_j$	junction temperature		-55	175	°C
$T_{sld(M)}$	peak soldering temperature		-	260	°C
<b>Source-drain diode</b>					
$I_S$	source current	$T_{mb} = 25\text{ °C}$	-	45	A
$I_{SM}$	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$	-	182	A
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$ ; $T_{j(\text{init})} = 25\text{ °C}$ ; $I_D = 45\text{ A}$ ; $V_{sup} \leq 80\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; unclamped	-	64	mJ



**Fig 1. Continuous drain current as a function of mounting base temperature**



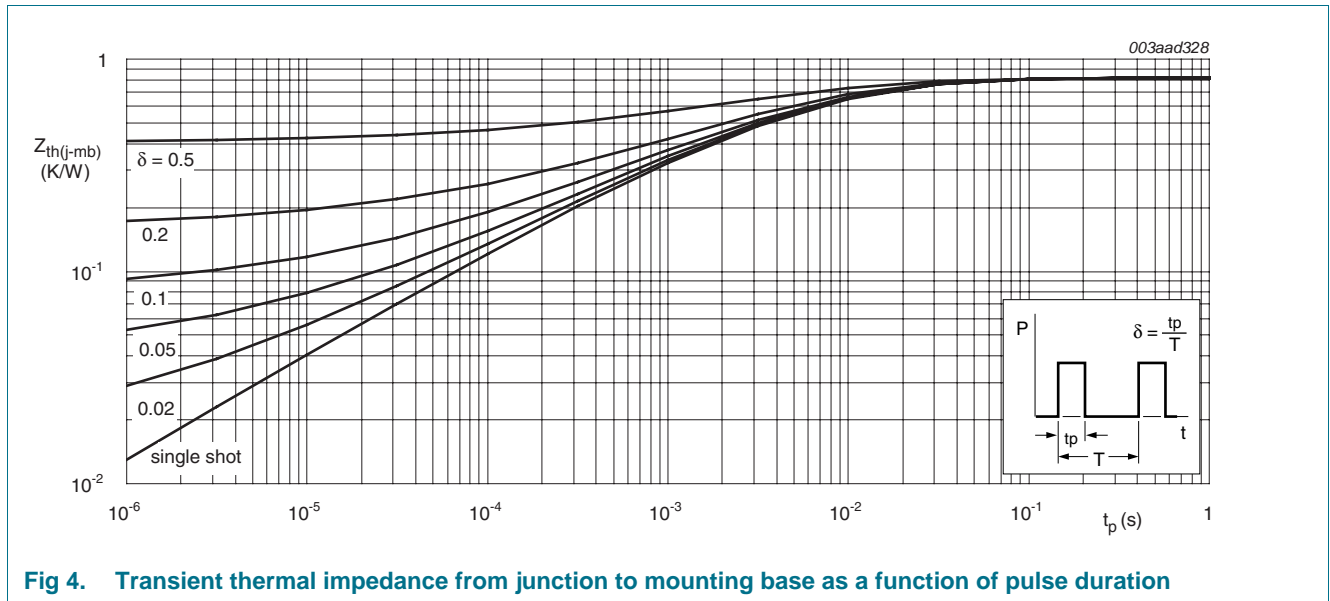
**Fig 2. Normalized total power dissipation as a function of mounting base temperature**



## 5. Thermal characteristics

**Table 5. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 4</a>	-	0.81	1.7	K/W



**Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration**

## 6. Characteristics

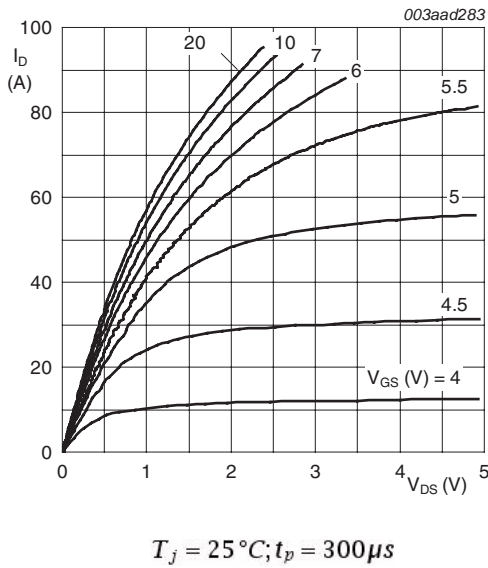
**Table 6. Characteristics**

Tested to JEDEC standards where applicable.

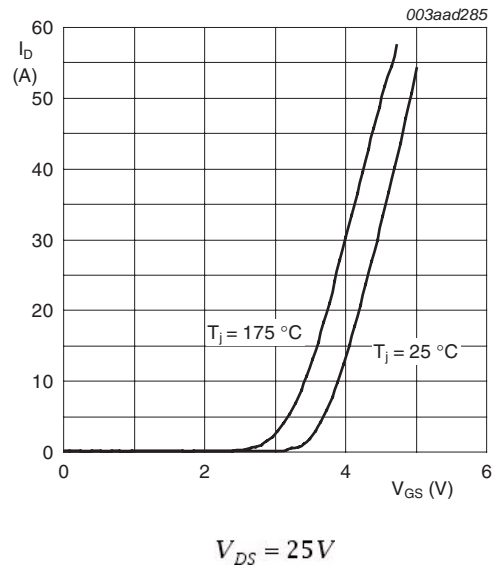
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	73	-	-	V
		$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	80	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ\text{C};$ see <a href="#">Figure 10</a>	1	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ see <a href="#">Figure 10</a>	-	-	4.6	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 11</a> ; see <a href="#">Figure 10</a>	2	3	4	V
$I_{DSS}$	drain leakage current	$V_{DS} = 80 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	2	$\mu\text{A}$
		$V_{DS} = 80 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ\text{C}$	-	-	50	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA
		$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 5 \text{ A}; T_j = 175 \text{ }^\circ\text{C};$ see <a href="#">Figure 12</a>	-	-	43	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 5 \text{ A}; T_j = 100 \text{ }^\circ\text{C};$ see <a href="#">Figure 12</a>	-	-	28	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 12</a> ; see <a href="#">Figure 13</a>	-	15	18	mΩ
$R_G$	internal gate resistance (AC)	$f = 1 \text{ MHz}$	-	0.56	-	Ω
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$	-	23	-	nC
		$I_D = 25 \text{ A}; V_{DS} = 40 \text{ V}; V_{GS} = 10 \text{ V};$ see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>	-	26	-	nC
$Q_{GS}$	gate-source charge		-	8	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	4.7	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	3.3	-	nC
$Q_{GD}$	gate-drain charge		-	6	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25 \text{ A}; V_{DS} = 40 \text{ V};$ see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>	-	4.8	-	V
$C_{iss}$	input capacitance	$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 16</a>	-	1640	-	pF
$C_{oss}$	output capacitance		-	170	-	pF
$C_{rss}$	reverse transfer capacitance		-	95	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 40 \text{ V}; R_L = 1.6 \text{ }^\circ\Omega; V_{GS} = 10 \text{ V};$ $R_{G(ext)} = 4.7 \text{ }^\circ\Omega$	-	16	-	ns
$t_r$	rise time		-	8	-	ns
$t_{d(off)}$	turn-off delay time		-	30	-	ns
$t_f$	fall time		-	7	-	ns

**Table 6. Characteristics ...continued**  
Tested to JEDEC standards where applicable.

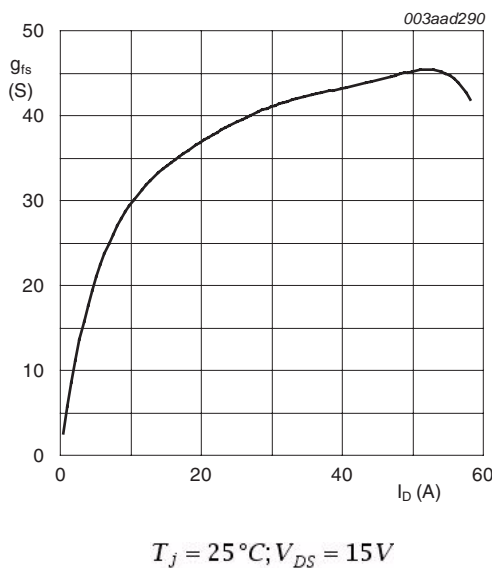
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 5\text{ A}$ ; $V_{GS} = 0\text{ V}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 17</a>	-	0.8	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 40\text{ A}$ ; $di_S/dt = 100\text{ A}/\mu\text{s}$ ;	-	50	-	ns
$Q_r$	recovered charge	$V_{GS} = 0\text{ V}$ ; $V_{DS} = 40\text{ V}$	-	80	-	nC



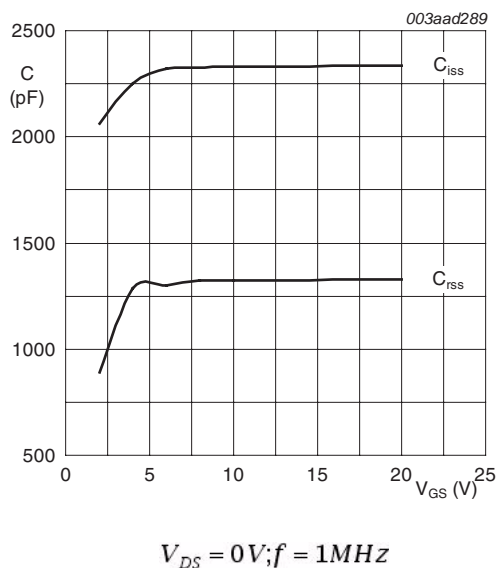
**Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values**



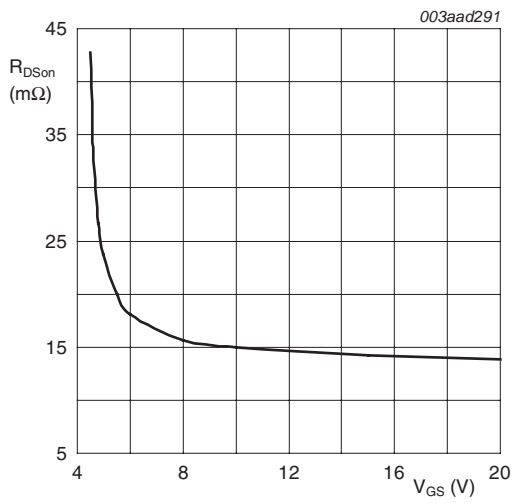
**Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values**



**Fig 7. Forward transconductance as a function of drain current; typical values**

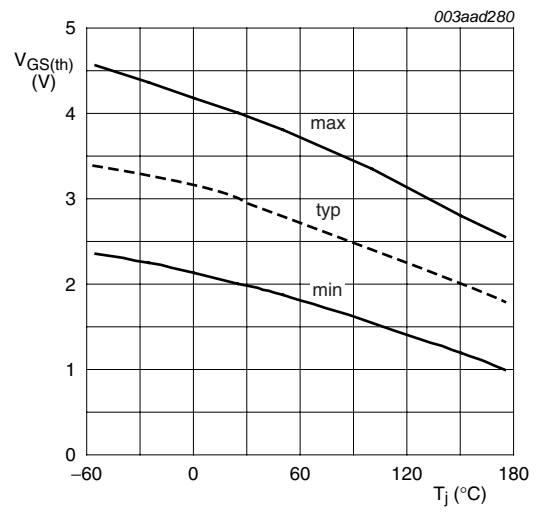


**Fig 8. Input and reverse transfer capacitances as a function of gate-source voltage; typical values**



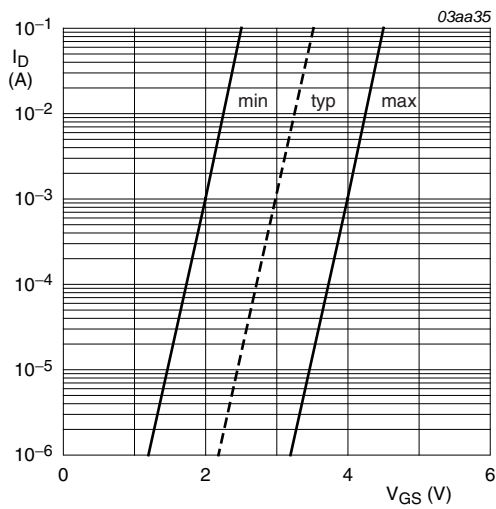
$T_j = 25^\circ C; I_D = 25A$

Fig 9. Drain-source on-state resistance as a function of gate-source voltage; typical values



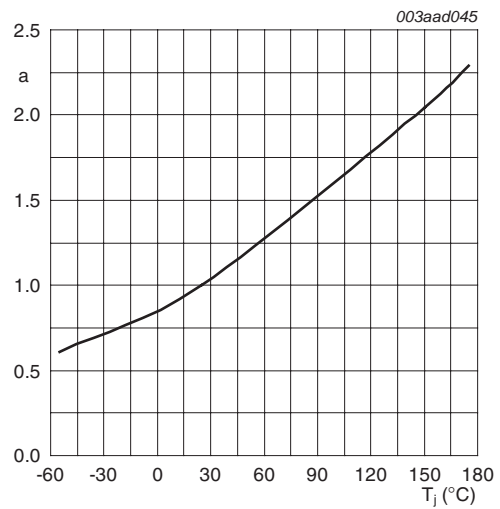
$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

Fig 10. Gate-source threshold voltage as a function of junction temperature



$T_j = 25^\circ C; V_{DS} = 5V$

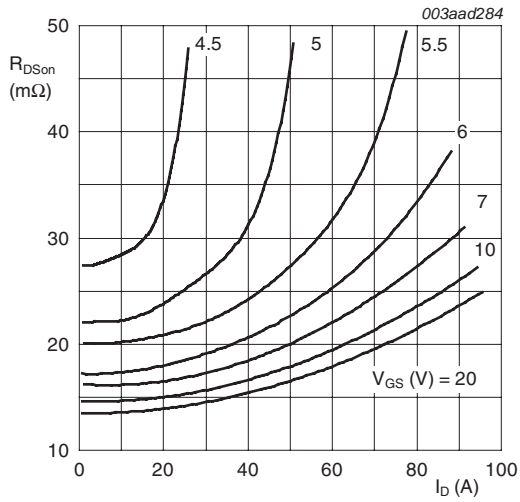
Fig 11. Sub-threshold drain current as a function of gate-source voltage



$$a = \frac{R_{DS(on)}}{R_{DS(on)@25^\circ C}}$$

Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature





$T_j = 25^\circ\text{C}; t_p = 300\mu\text{s}$

Fig 13. Drain-source on-state resistance as a function of drain current; typical values

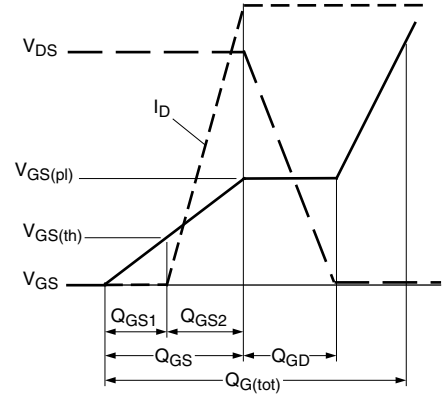
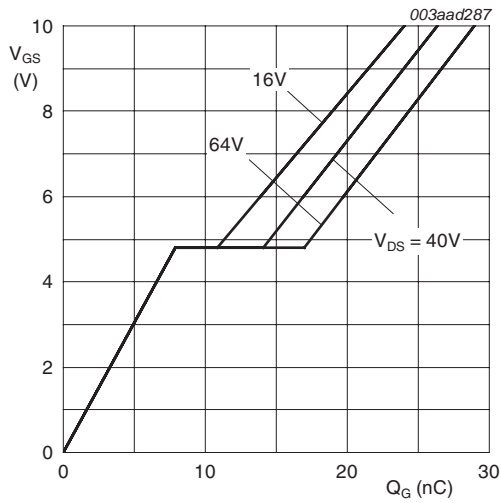
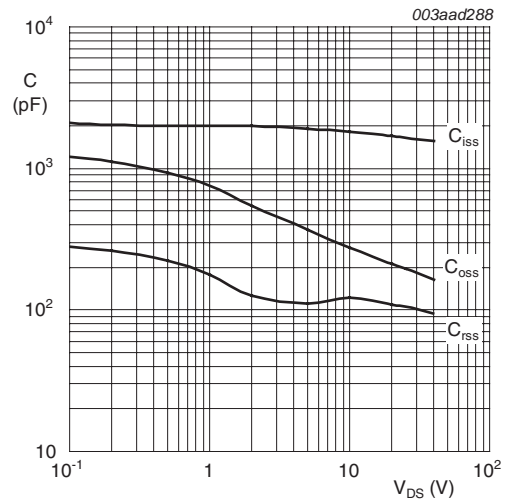


Fig 14. Gate charge waveform definitions



$T_j = 25^\circ\text{C}; I_D = 25\text{A}$

Fig 15. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0\text{V}; f = 1\text{MHz}$

Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

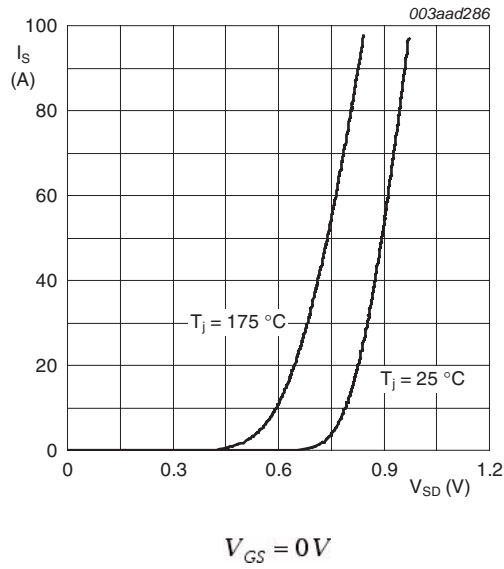


Fig 17. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (LPAK); 4 leads

SOT669

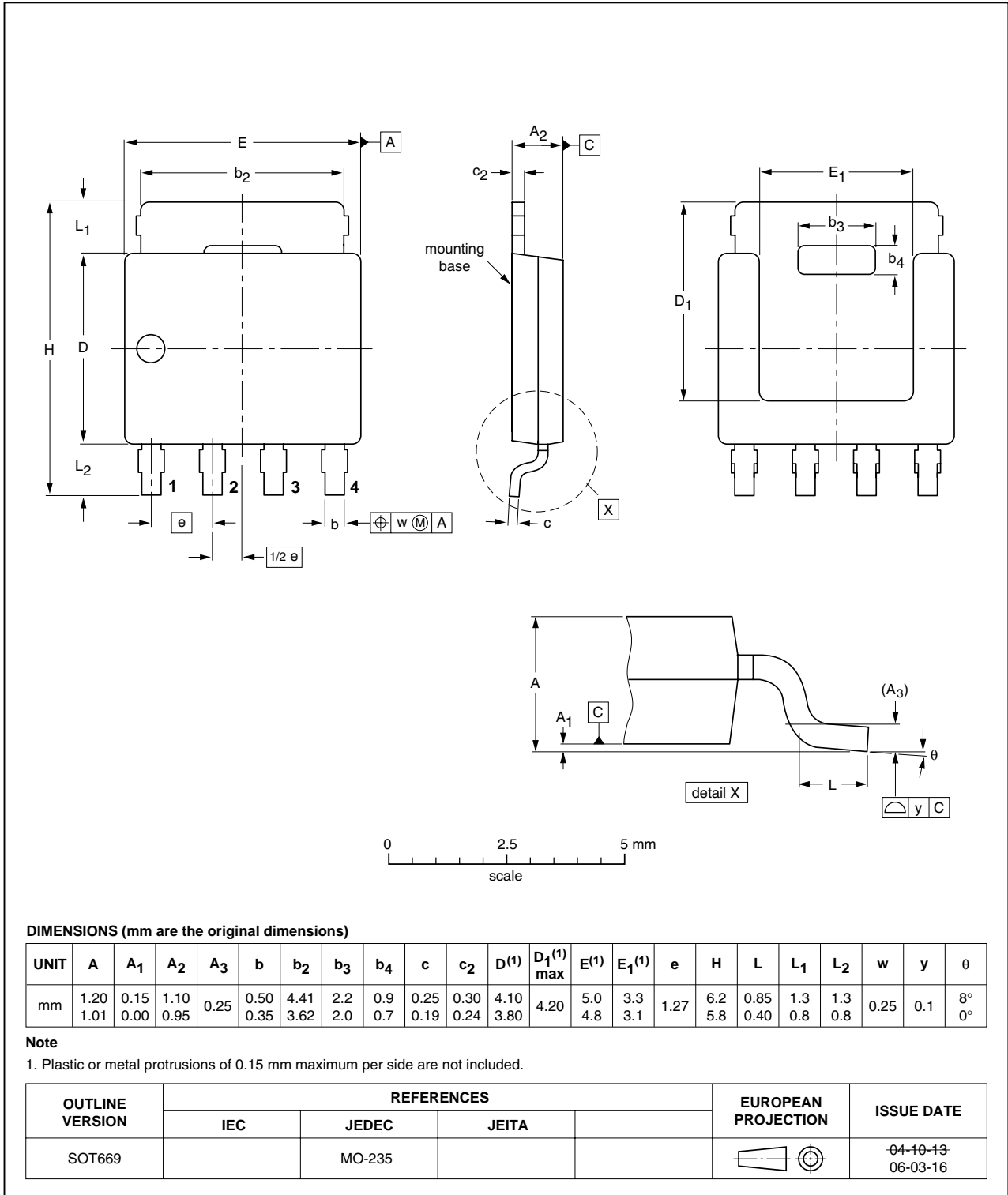


Fig 18. Package outline SOT669 (LPAK)

## 8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN018-80YS v.2	20101028	Product data sheet	-	PSMN018-80YS v.1
Modifications:	• Various changes to content.			
PSMN018-80YS v.1	20101026	Product data sheet	-	-

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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[IPS70R2K0CEAKMA1](#) [BUK954R8-60E](#) [DMN3404LQ-7](#) [NTE6400](#) [SQJ402EP-T1-GE3](#) [2SK2614\(TE16L1,Q\)](#) [2N7002KW-FAI](#)  
[DMN1017UCP3-7](#) [EFC2J004NUZTDG](#) [ECH8691-TL-W](#) [FCAB21350L1](#) [P85W28HP2F-7071](#) [DMN1053UCP4-7](#) [NTE221](#) [NTE2384](#)  
[NTE2903](#) [NTE2941](#) [NTE2945](#) [NTE2946](#) [NTE2960](#) [NTE2967](#) [NTE2969](#) [NTE2976](#) [NTE455](#) [NTE6400A](#) [NTE2910](#) [NTE2916](#) [NTE2956](#)  
[NTE2911](#) [US6M2GTR](#) [TK10A80W,S4X\(S](#) [SSM6P69NU,LF](#)