



PSMN038-100HS

N-channel 100 V, 37.6 mOhm, standard level MOSFET in LPAK56D using TrenchMOS technology

26 September 2022

Product data sheet

1. General description

Dual standard level N-channel MOSFET in an LPAK56D (Dual Power-SO8) package using TrenchMOS technology.

2. Features and benefits

- High peak drain current I_{DM}
- Copper clip and flexible Leads
- High operating junction temperature $T_j = 175\text{ °C}$
- Superior reliability
- Low body diode reverse recovery charge Q_r

3. Applications

- Synchronous rectifier
- Forward and flyback converter
- Industrial drive
- Power management system
- Uninterruptible Power Supply (UPS)

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	100	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	-	-	21.4	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	-	53	W
T_j	junction temperature		-55	-	175	°C
Static characteristics FET1 and FET2						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 5\text{ A}$; $T_j = 25\text{ °C}$; Fig. 11	-	30	37.6	mΩ
		$V_{GS} = 10\text{ V}$; $I_D = 5\text{ A}$; $T_j = 175\text{ °C}$; Fig. 11 ; Fig. 12	-	80	104	mΩ
Dynamic characteristics FET1 and FET2						
Q_{GD}	gate-drain charge	$I_D = 5\text{ A}$; $V_{DS} = 80\text{ V}$; $V_{GS} = 10\text{ V}$; $T_j = 25\text{ °C}$; Fig. 13 ; Fig. 14	-	9.7	-	nC
$Q_{G(tot)}$	total gate charge		-	25.9	-	nC
Avalanche Ruggedness FET1 and FET2						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 21.4\text{ A}$; $V_{sup} \leq 100\text{ V}$; $R_{GS} = 50\text{ Ω}$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped; Fig. 4	[1] [2]	-	46	mJ

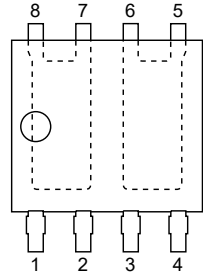
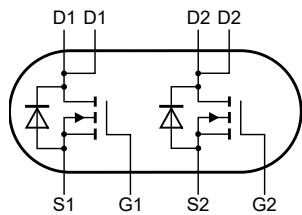
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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode FET1 and FET2						
Q _r	recovered charge	I _S = 5 A; di _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 50 V; T _J = 25 °C	-	44	-	nC

- [1] Refer to application note AN10273 for further information
- [2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	 <p>LPAK56D; Dual LPAK (SOT1205)</p>	 <p>mbk725</p>
2	G1	gate1		
3	S2	source2		
4	G2	gate2		
5	D2	drain2		
6	D2	drain2		
7	D1	drain1		
8	D1	drain1		

6. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
PSMN038-100HS	LPAK56D; Dual LPAK	plastic, single ended surface mounted package (LPAK56D); 8 leads	SOT1205

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN038-100HS	38RS10H

8. Limiting values

Table 5. Limiting values

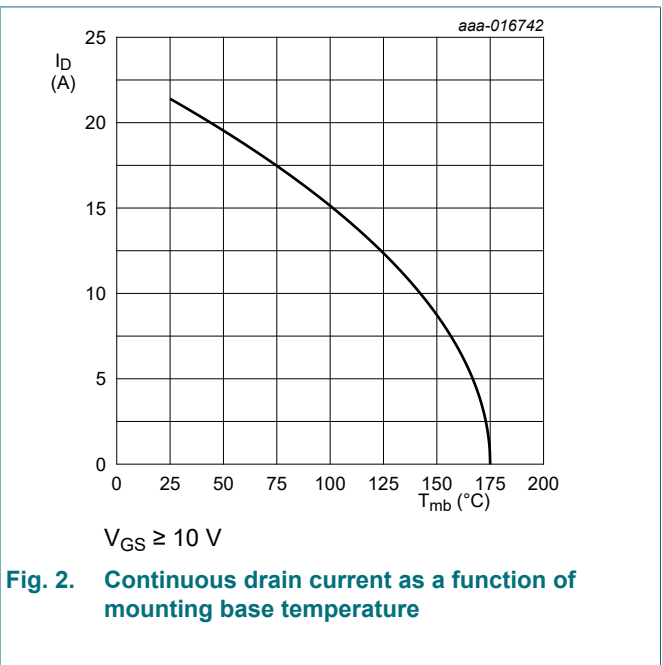
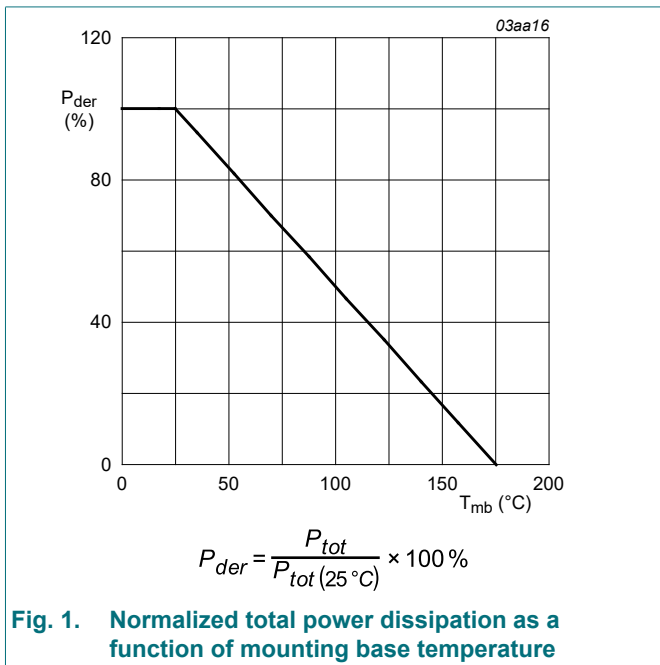
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _J ≤ 175 °C	-	100	V
V _{DGR}	drain-gate voltage	R _{GS} = 20 kΩ	-	100	V
V _{GS}	gate-source voltage	DC; T _J ≤ 175 °C	-20	20	V
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1	-	53	W
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 2	-	21.4	A
		V _{GS} = 10 V; T _{mb} = 100 °C; Fig. 2	-	15	A

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Symbol	Parameter	Conditions	Min	Max	Unit
I_{DM}	peak drain current	pulsed; $t_p \leq 10 \mu\text{s}$; $T_{mb} = 25 \text{ }^\circ\text{C}$; Fig. 3	-	84	A
T_{stg}	storage temperature		-55	175	$^\circ\text{C}$
T_j	junction temperature		-55	175	$^\circ\text{C}$
$T_{sld(M)}$	peak soldering temperature		-	260	$^\circ\text{C}$
Source-drain diode FET1 and FET2					
I_S	source current	$T_{mb} = 25 \text{ }^\circ\text{C}$	-	21.4	A
I_{SM}	peak source current	pulsed; $t_p \leq 10 \mu\text{s}$; $T_{mb} = 25 \text{ }^\circ\text{C}$	-	84	A
Avalanche Ruggedness FET1 and FET2					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 21.4 \text{ A}$; $V_{sup} \leq 100 \text{ V}$; $R_{GS} = 50 \Omega$; $V_{GS} = 10 \text{ V}$; $T_{j(\text{init})} = 25 \text{ }^\circ\text{C}$; unclamped; Fig. 4	[1] [2]	-	46 mJ

- [1] Refer to application note AN10273 for further information
- [2] Single-pulse avalanche rating limited by maximum junction temperature of 175 $^\circ\text{C}$



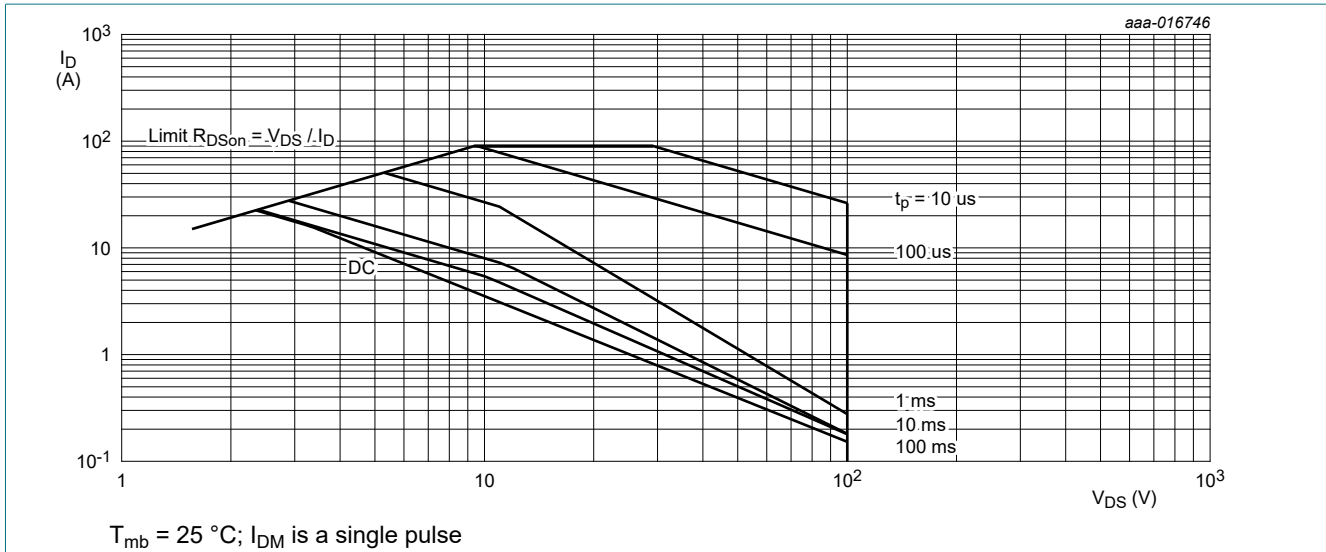


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

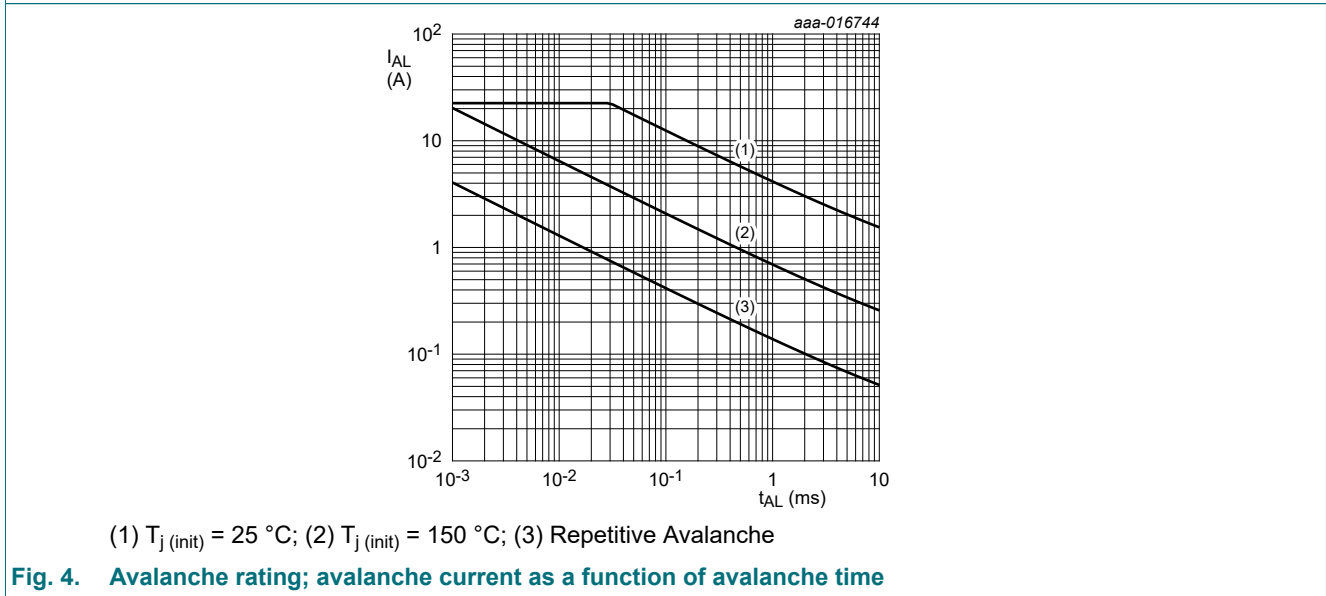


Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	-	2.84	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Minimum footprint; mounted on a printed circuit board	-	95	-	K/W

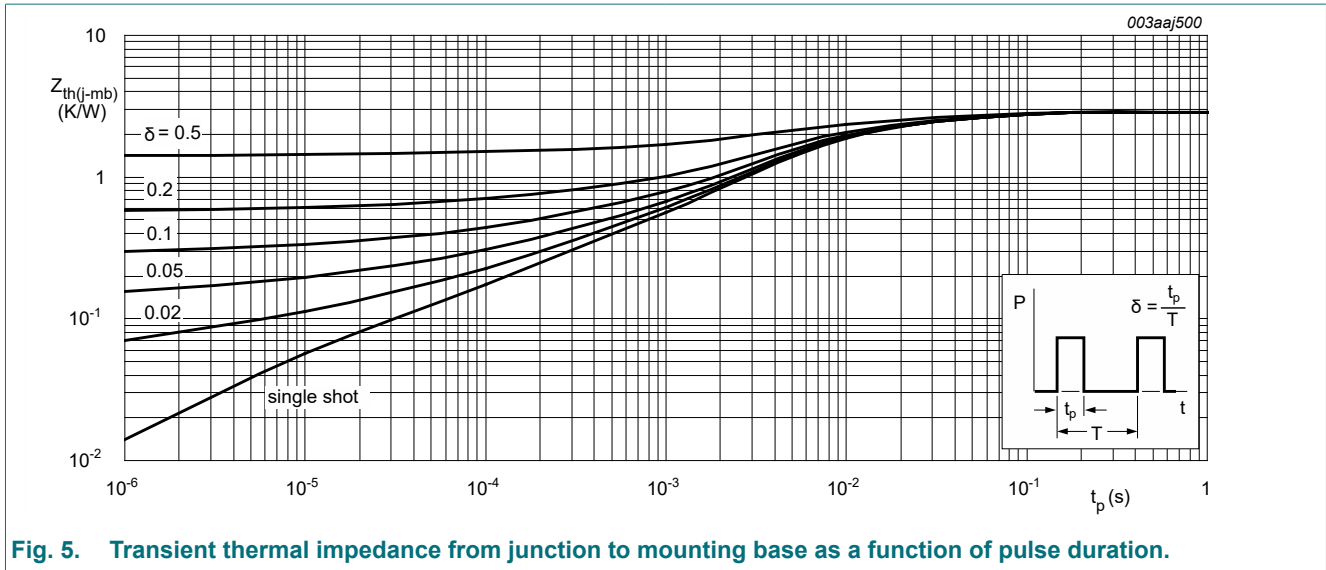


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration.

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics FET1 and FET2						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$ $I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	90	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ C$; Fig. 9 ; Fig. 10 $I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 175 \text{ }^\circ C$; Fig. 10 $I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = -55 \text{ }^\circ C$; Fig. 10	2.4	3	4	V
I_{DSS}	drain leakage current	$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$ $V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ C$	-	0.02	1	μA
I_{GSS}	gate leakage current	$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$ $V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ }^\circ C$; Fig. 11 $V_{GS} = 10 \text{ V}; I_D = 5 \text{ A}; T_j = 175 \text{ }^\circ C$; Fig. 11 ; Fig. 12	-	30	37.6	m Ω
Dynamic characteristics FET1 and FET2						
$Q_{G(tot)}$	total gate charge	$I_D = 5 \text{ A}; V_{DS} = 80 \text{ V}; V_{GS} = 10 \text{ V}; T_j = 25 \text{ }^\circ C$; Fig. 13 ; Fig. 14	-	25.9	-	nC
Q_{GS}	gate-source charge		-	4.3	-	nC
Q_{GD}	gate-drain charge		-	9.7	-	nC
C_{iss}	input capacitance	$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$; Fig. 15	-	1150	1533	pF
C_{oss}	output capacitance		-	122	147	pF
C_{rss}	reverse transfer capacitance		-	84	115	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 80 \text{ V}; R_L = 16 \text{ } \Omega; V_{GS} = 10 \text{ V}; R_{G(ext)} = 5 \text{ } \Omega; T_j = 25 \text{ }^\circ C$	-	6.2	-	ns
t_r	rise time		-	11.2	-	ns
$t_{d(off)}$	turn-off delay time		-	20.3	-	ns
t_f	fall time		-	13.9	-	ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode FET1 and FET2						
V_{SD}	source-drain voltage	$I_S = 5\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 16	-	0.78	1.2	V
t_{rr}	reverse recovery time	$I_S = 5\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$;	-	32.9	-	ns
Q_r	recovered charge	$V_{DS} = 50\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$	-	44	-	nC

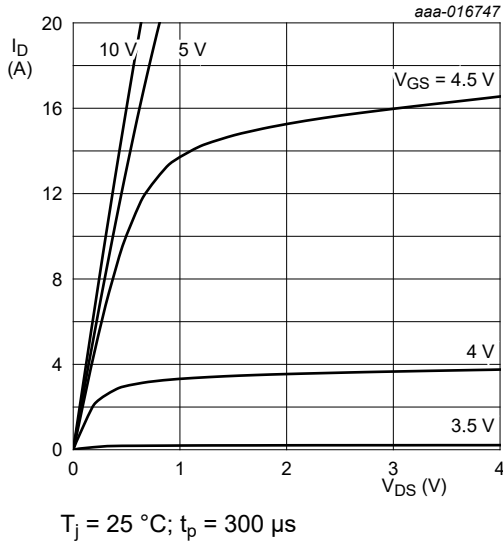


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

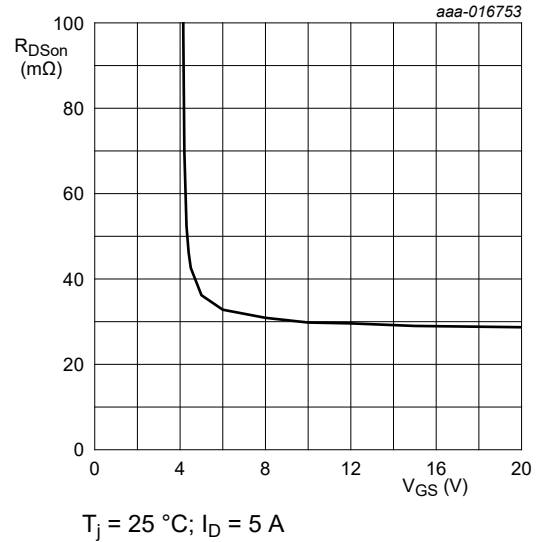


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

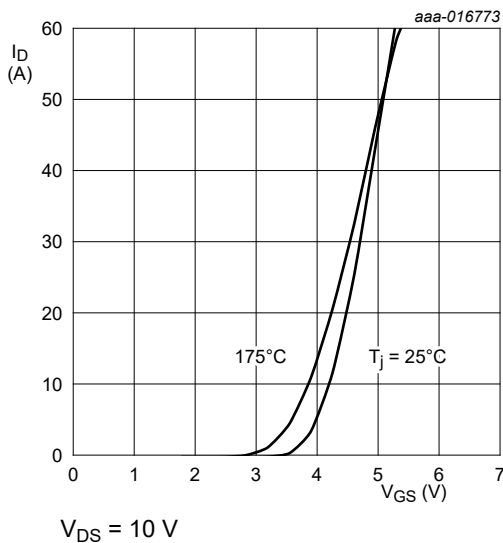


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

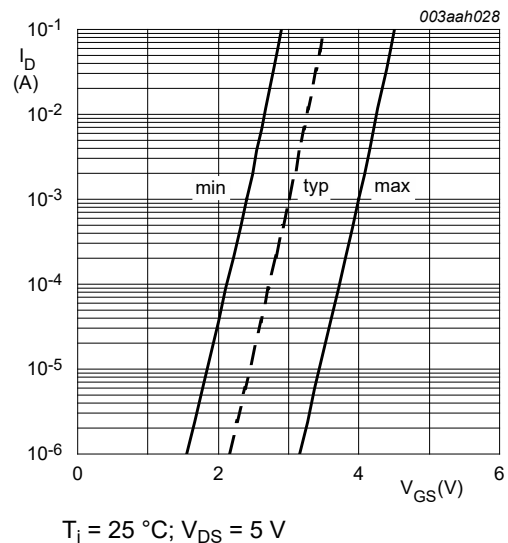


Fig. 9. Sub-threshold drain current as a function of gate-source voltage

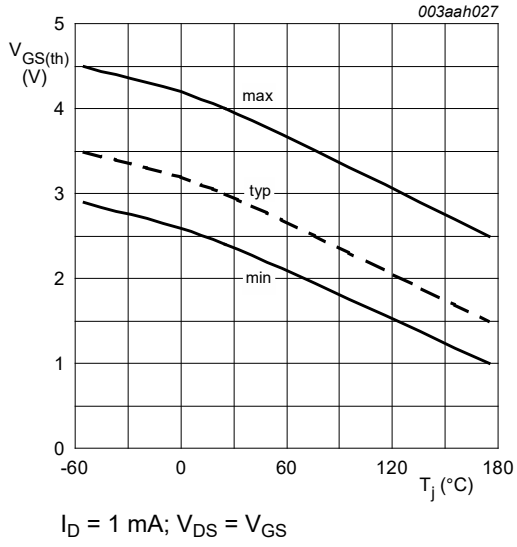


Fig. 10. Gate-source threshold voltage as a function of junction temperature

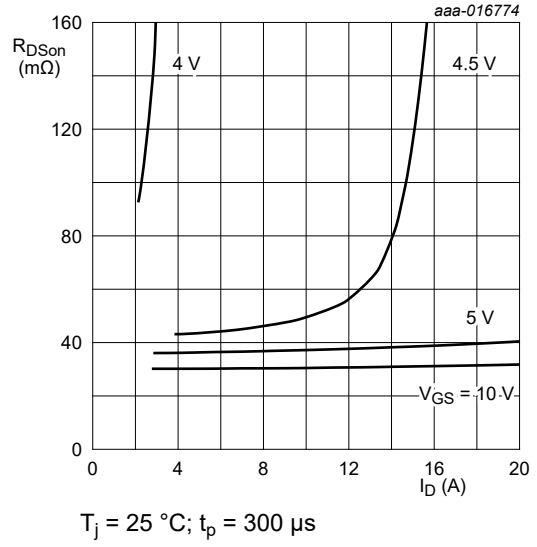


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

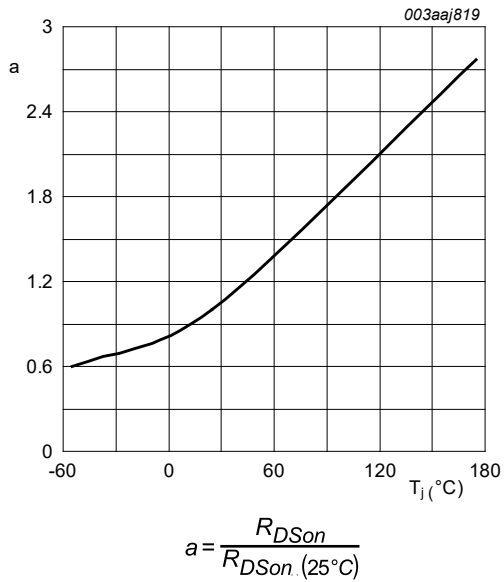


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

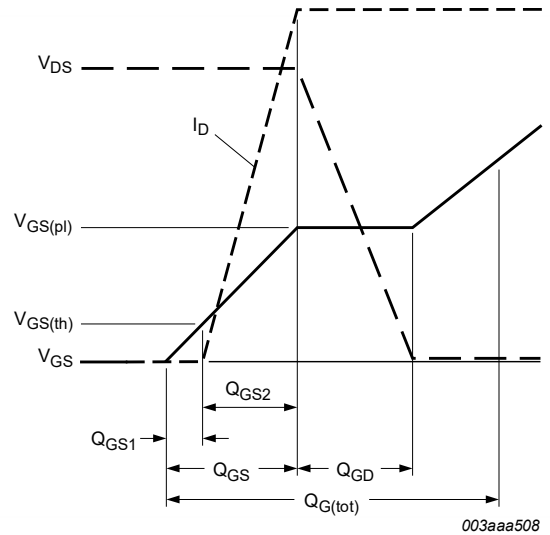


Fig. 13. Gate charge waveform definitions

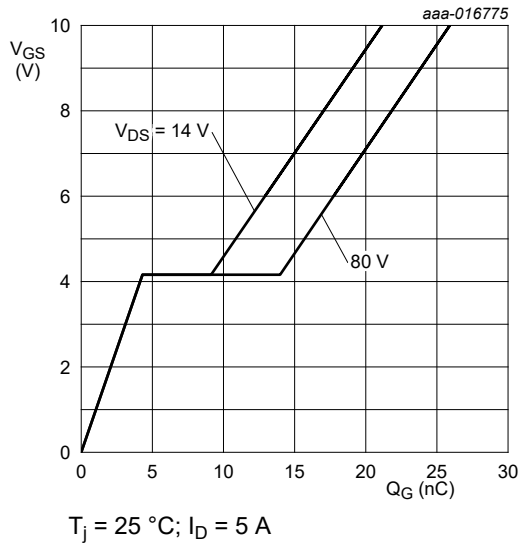


Fig. 14. Gate-source voltage as a function of gate charge; typical values

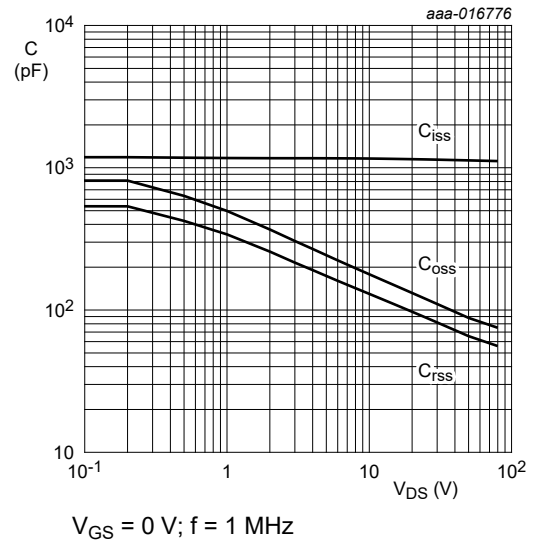


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

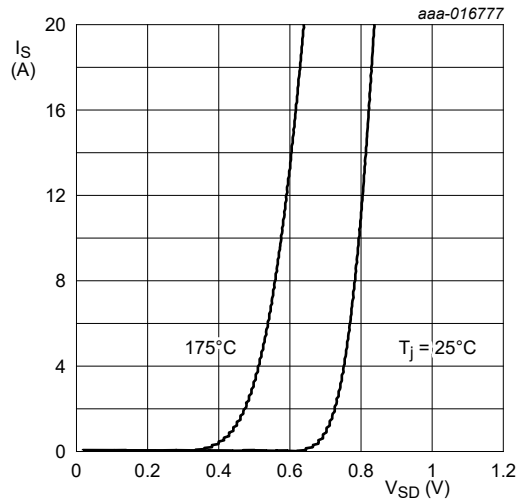


Fig. 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

11. Package outline

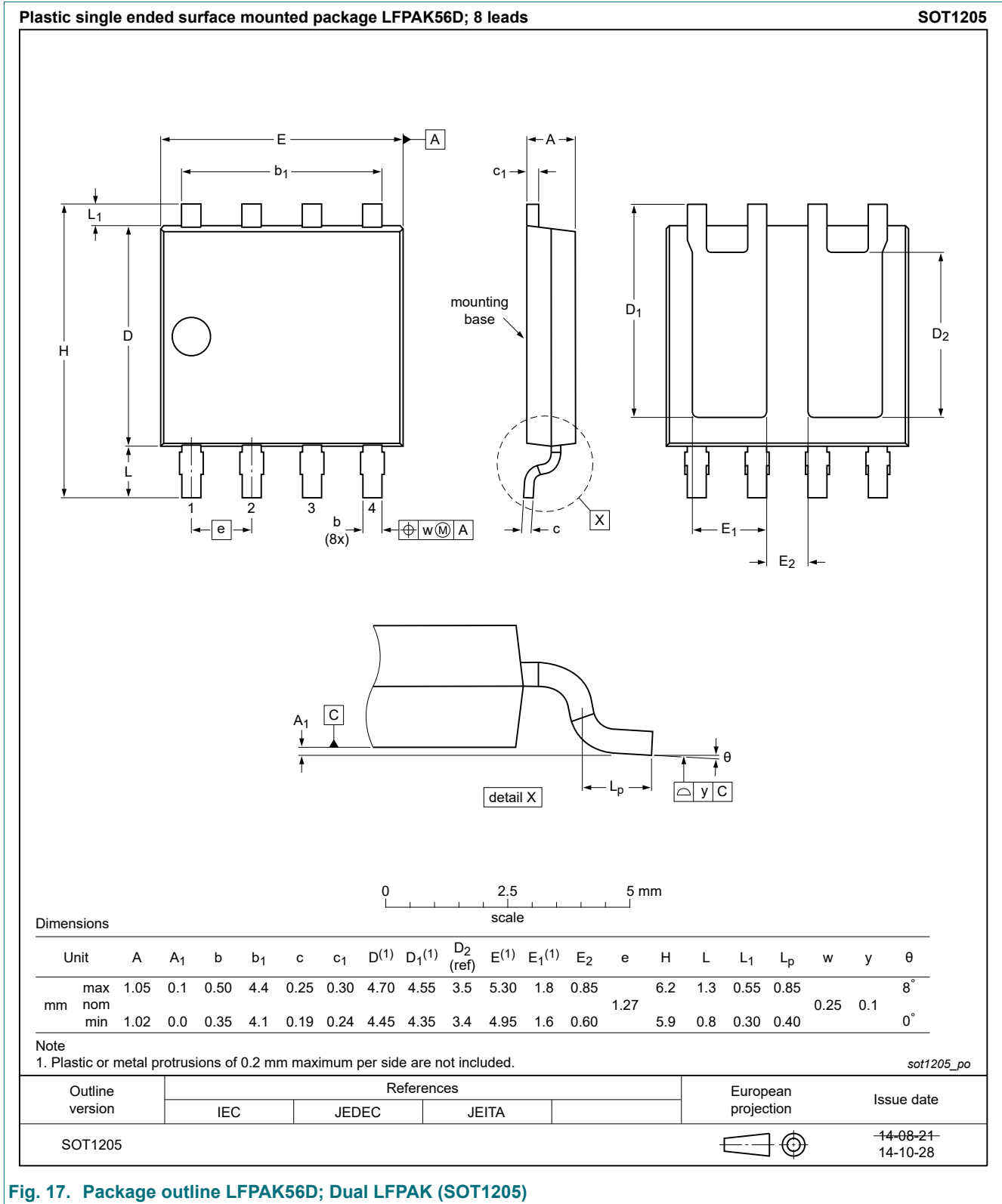


Fig. 17. Package outline LPAK56D; Dual LPAK (SOT1205)

12. Soldering

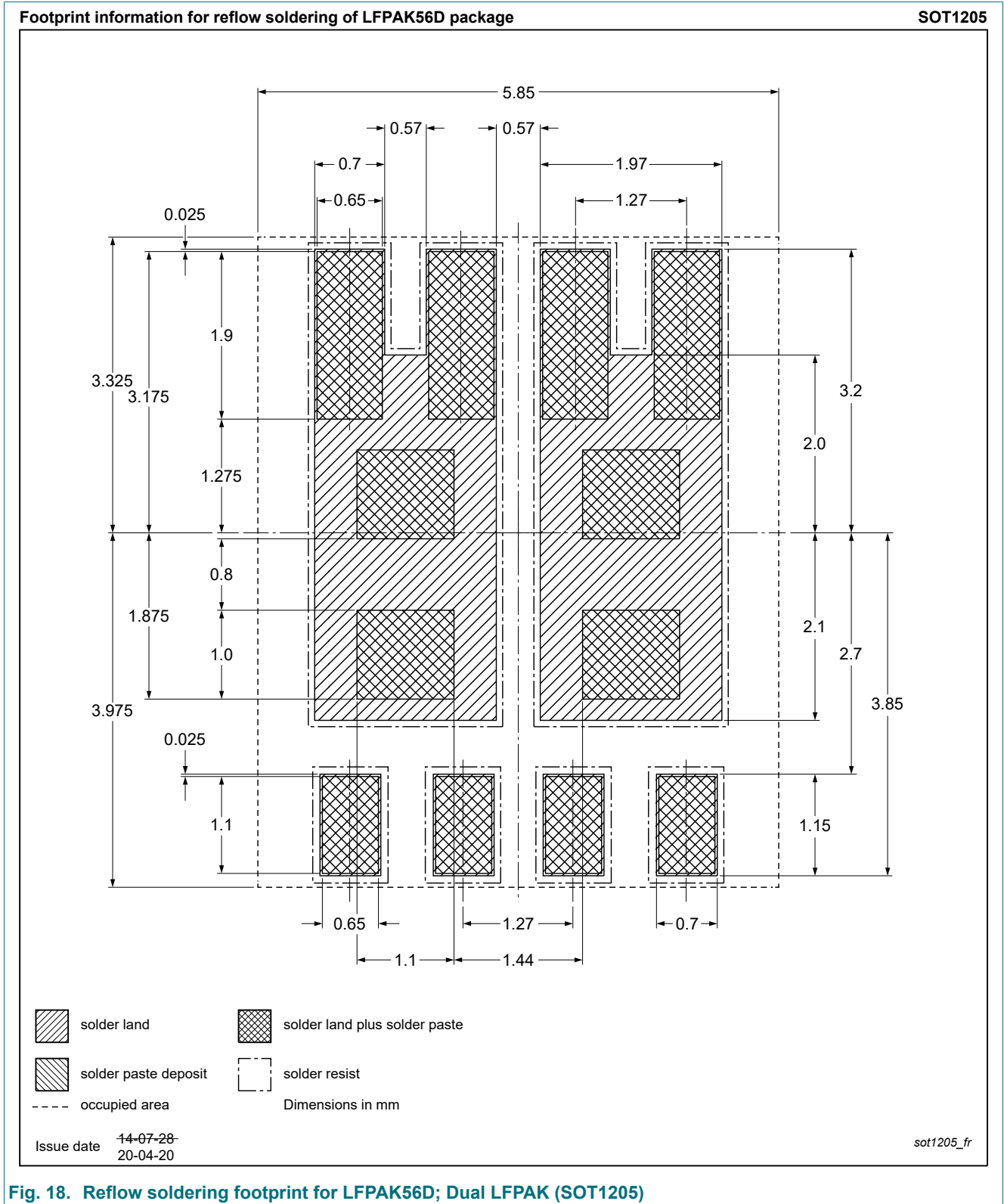


Fig. 18. Reflow soldering footprint for LPAK56D; Dual LPAK (SOT1205)

13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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