



PSMN059-150Y

N-channel TrenchMOS SiliconMAX standard level FET

3 October 2013

Product data sheet

1. General description

SiliconMAX standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

2. Features and benefits

- Higher operating power due to low thermal resistance
- Suitable for high frequency applications due to fast switching characteristics

3. Applications

- Class D amplifier
- DC-to-DC converters
- Motion control
- Switched-mode power supplies

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 150\text{ °C}$	-	-	150	V
I_D	drain current	$T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V};$ Fig. 1 ; Fig. 3	-	-	43	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C};$ Fig. 2	-	-	113	W
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 12\text{ A}; T_j = 25\text{ °C};$ Fig. 9 ; Fig. 10	-	46	59	m Ω
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 10\text{ V}; I_D = 12\text{ A}; V_{DS} = 75\text{ V};$ Fig. 11 ; Fig. 12	-	9.1	-	nC

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>LFLPAK56; Power-SO8 (SOT669)</p>	
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN059-150Y	LFLPAK56; Power-SO8	Plastic single-ended surface-mounted package (LFLPAK56; Power-SO8); 4 leads	SOT669

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN059-150Y	059150

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 150\text{ °C}$	-	150	V
V_{DGR}	drain-gate voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 150\text{ °C}$; $R_{GS} = 20\ \Omega$	-	150	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 1 ; Fig. 3	-	43	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; Fig. 1	-	27.7	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\ \mu\text{s}$; $T_{mb} = 25\text{ °C}$; Fig. 3	-	129	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 2	-	113	W
T_{stg}	storage temperature		-55	150	°C

Symbol	Parameter	Conditions	Min	Max	Unit
T_j	junction temperature		-55	150	°C
Source-drain diode					
I_S	source current	$T_{mb} = 25\text{ °C}$	-	52	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$	-	208	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ °C}$; $I_D = 12.1\text{ A}$; $V_{sup} \leq 150\text{ V}$; unclamped; $t_p = 0.21\text{ ms}$; $R_{GS} = 50\text{ }\Omega$	-	255	mJ

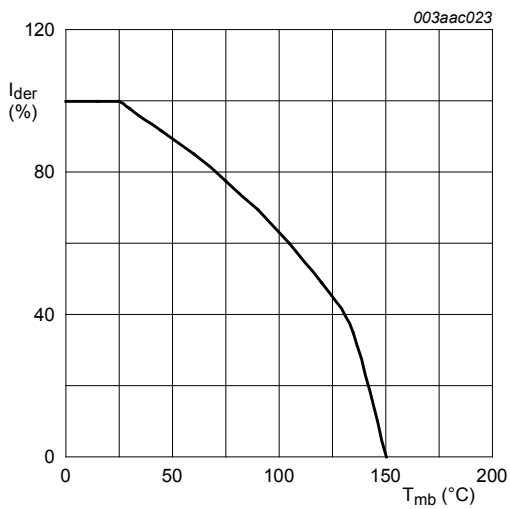


Fig. 1. Normalized continuous drain current as a function of mounting base temperature

$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100\%$$

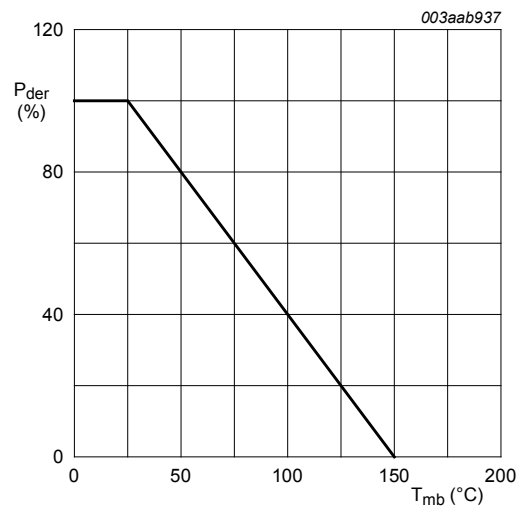
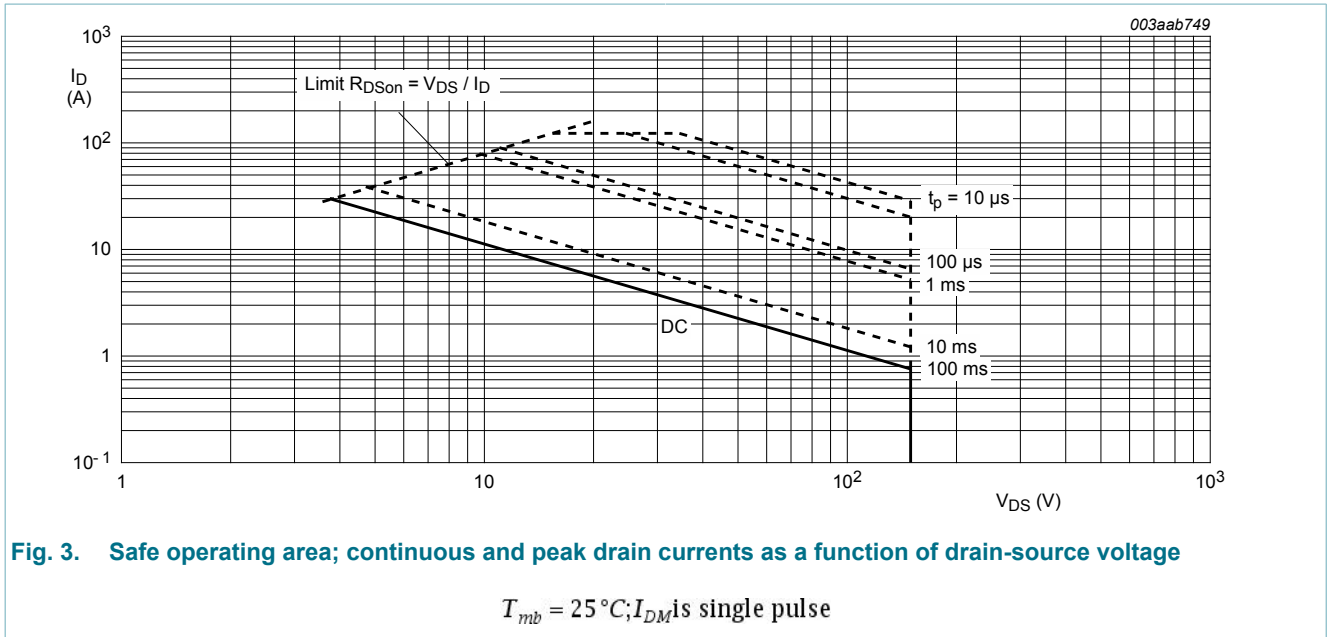


Fig. 2. Normalized total power dissipation as a function of solder point temperature

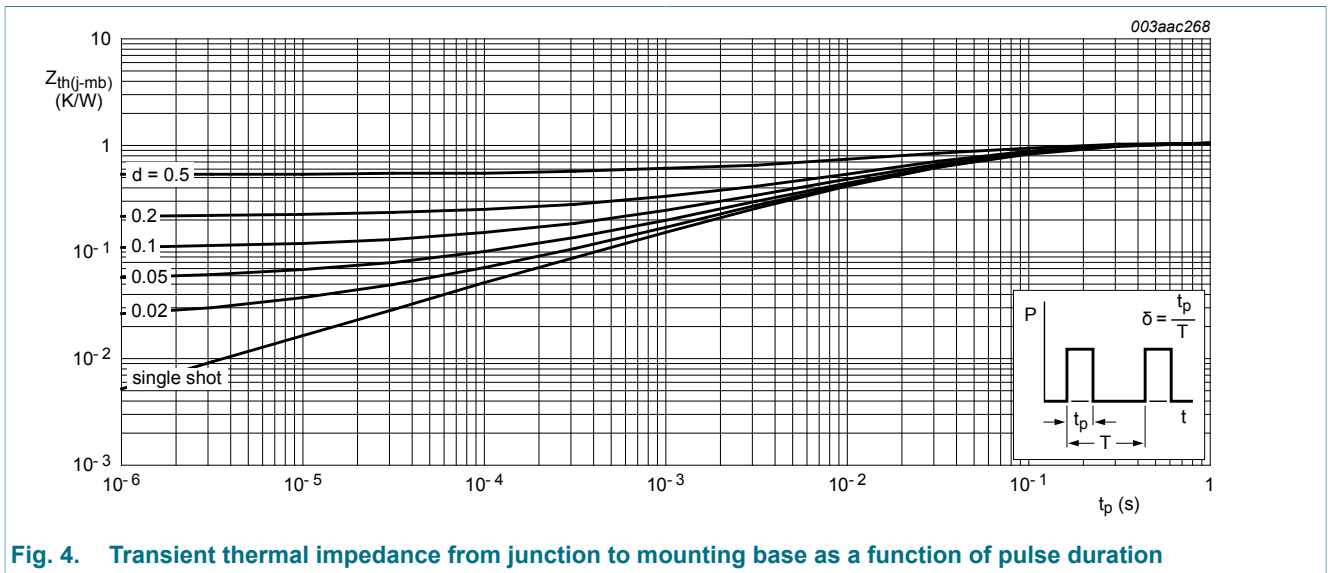
$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$



9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	mounted on a printed-circuit board; vertical in still air; Fig. 4	-	-	1.1	K/W



10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	150	-	-	V
		$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	133	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 7; Fig. 8	2	3	4	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 150 \text{ }^\circ\text{C};$ Fig. 7; Fig. 8	1	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ Fig. 7; Fig. 8	-	-	4.4	V
I_{DSS}	drain leakage current	$V_{DS} = 120 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	1	μA
		$V_{DS} = 120 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ }^\circ\text{C}$	-	-	100	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 12 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 9; Fig. 10	-	46	59	m Ω
		$V_{GS} = 10 \text{ V}; I_D = 12 \text{ A}; T_j = 150 \text{ }^\circ\text{C};$ Fig. 9; Fig. 10	-	101	135	m Ω
R_G	gate resistance	$f = 1 \text{ MHz}$	-	1.1	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 12 \text{ A}; V_{DS} = 75 \text{ V}; V_{GS} = 10 \text{ V};$ Fig. 11; Fig. 12	-	27.9	-	nC
Q_{GS}	gate-source charge		-	6.3	-	nC
Q_{GD}	gate-drain charge		-	9.1	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 12 \text{ A}; V_{DS} = 75 \text{ V};$ Fig. 11; Fig. 12	-	4.8	-	V
C_{iss}	input capacitance	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ Fig. 13	-	1529	-	pF
C_{oss}	output capacitance		-	208	-	pF
C_{rss}	reverse transfer capacitance		-	66	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 75 \text{ V}; R_L = 3 \text{ } \Omega; V_{GS} = 10 \text{ V};$ $R_{G(ext)} = 5.6 \text{ } \Omega$	-	14.2	-	ns
t_r	rise time		-	42	-	ns
$t_{d(off)}$	turn-off delay time		-	54.2	-	ns
t_f	fall time		-	11.1	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 12 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 14	-	0.9	1.2	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{rr}	reverse recovery time	$I_S = 12\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 30\text{ V}$	-	67	-	ns
Q_r	recovered charge	$I_S = 12\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$	-	226	-	nC

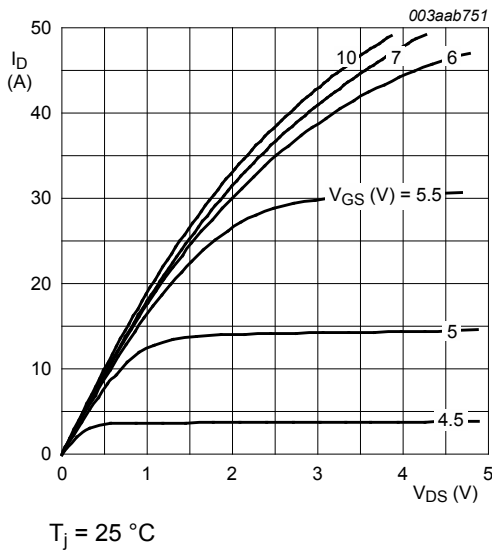


Fig. 5. Output characteristics: drain current as a function of drain-source voltage; typical values

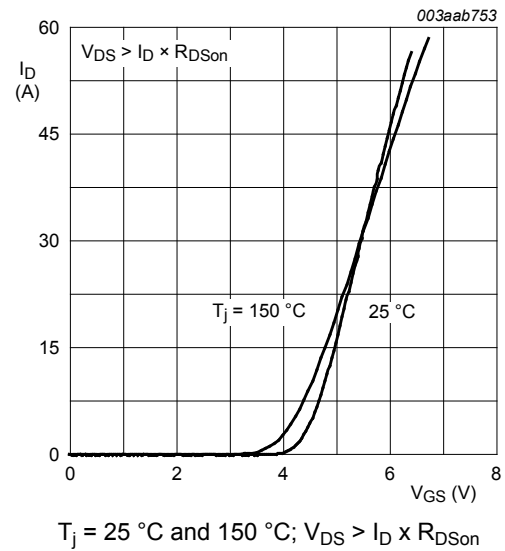


Fig. 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values

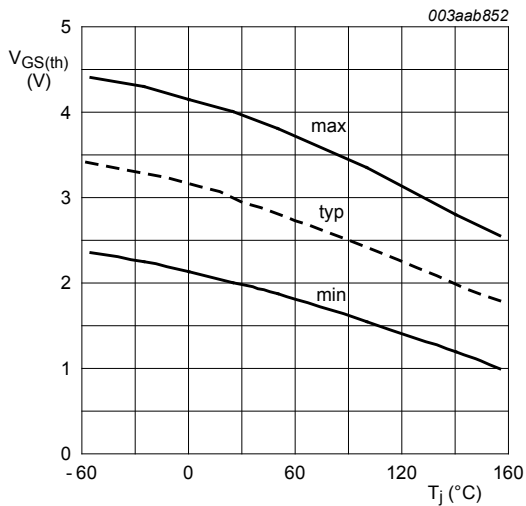


Fig. 7. Gate-source threshold voltage as a function of junction temperature

$$I_D = 1\text{ mA}; V_{DS} = V_{GS}$$

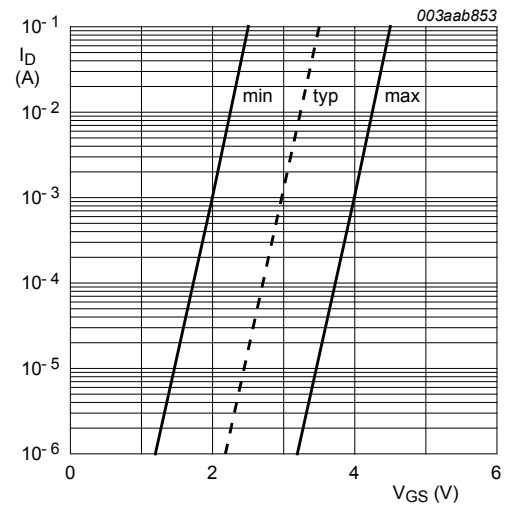


Fig. 8. Sub-threshold drain current as a function of gate-source voltage

$$T_j = 25\text{ °C}; V_{DS} = 5\text{ V}$$

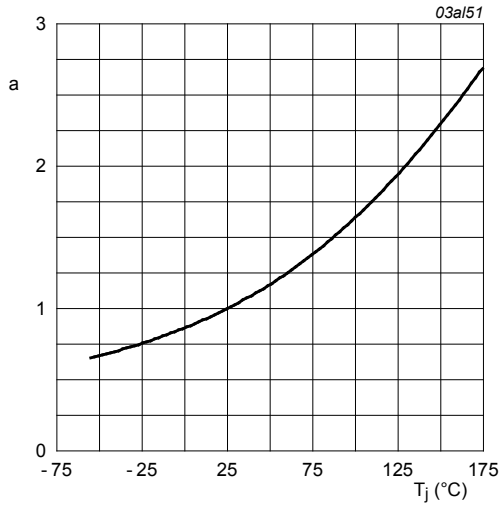


Fig. 9. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon(25^\circ C)}}$$

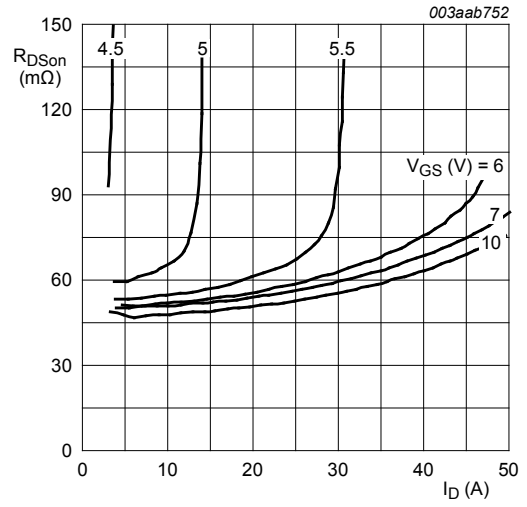


Fig. 10. Drain-source on-state resistance as a function of drain current; typical values

$T_j = 25^\circ C$

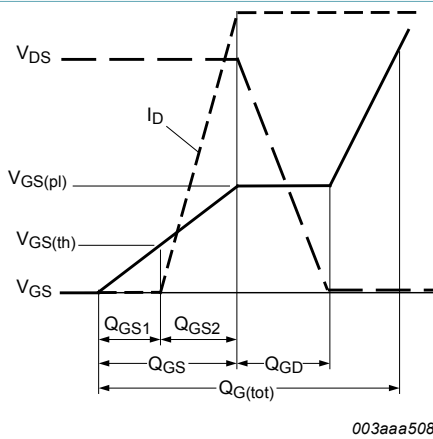


Fig. 11. Gate charge waveform definitions

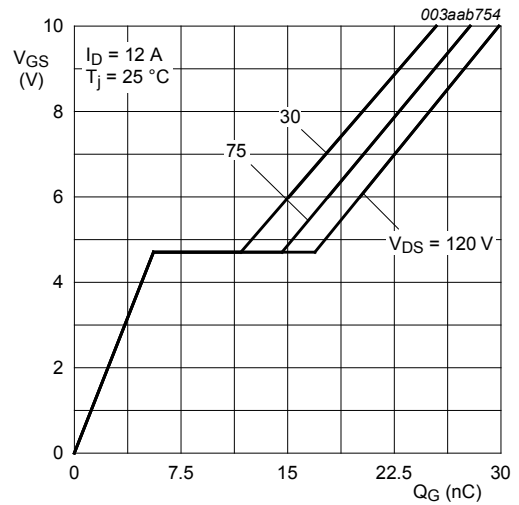


Fig. 12. Gate-source voltage as a function of gate charge; typical values

$I_D = 12 A; V_{DS} = 30, 75 \text{ and } 120 V$

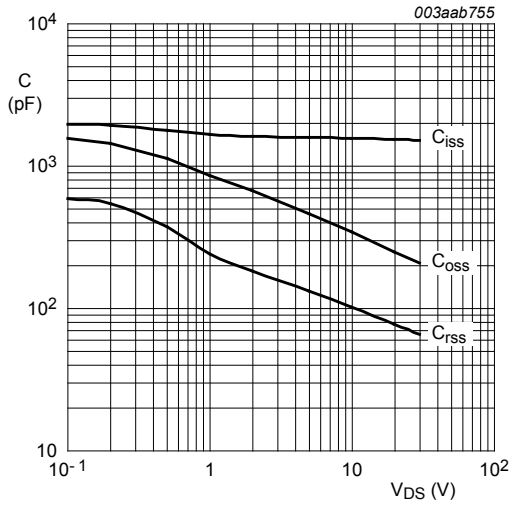


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$$V_{GS} = 0V; f = 1MHz$$

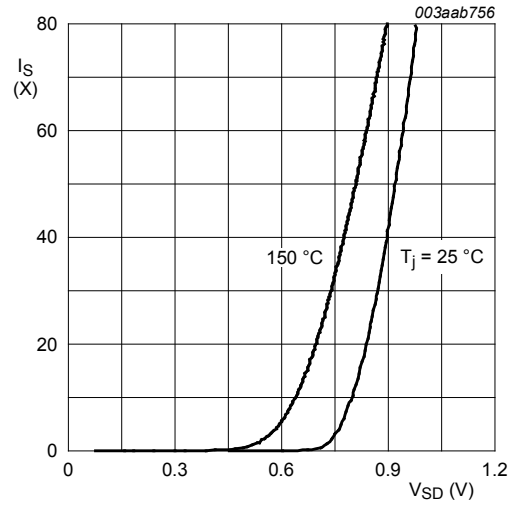
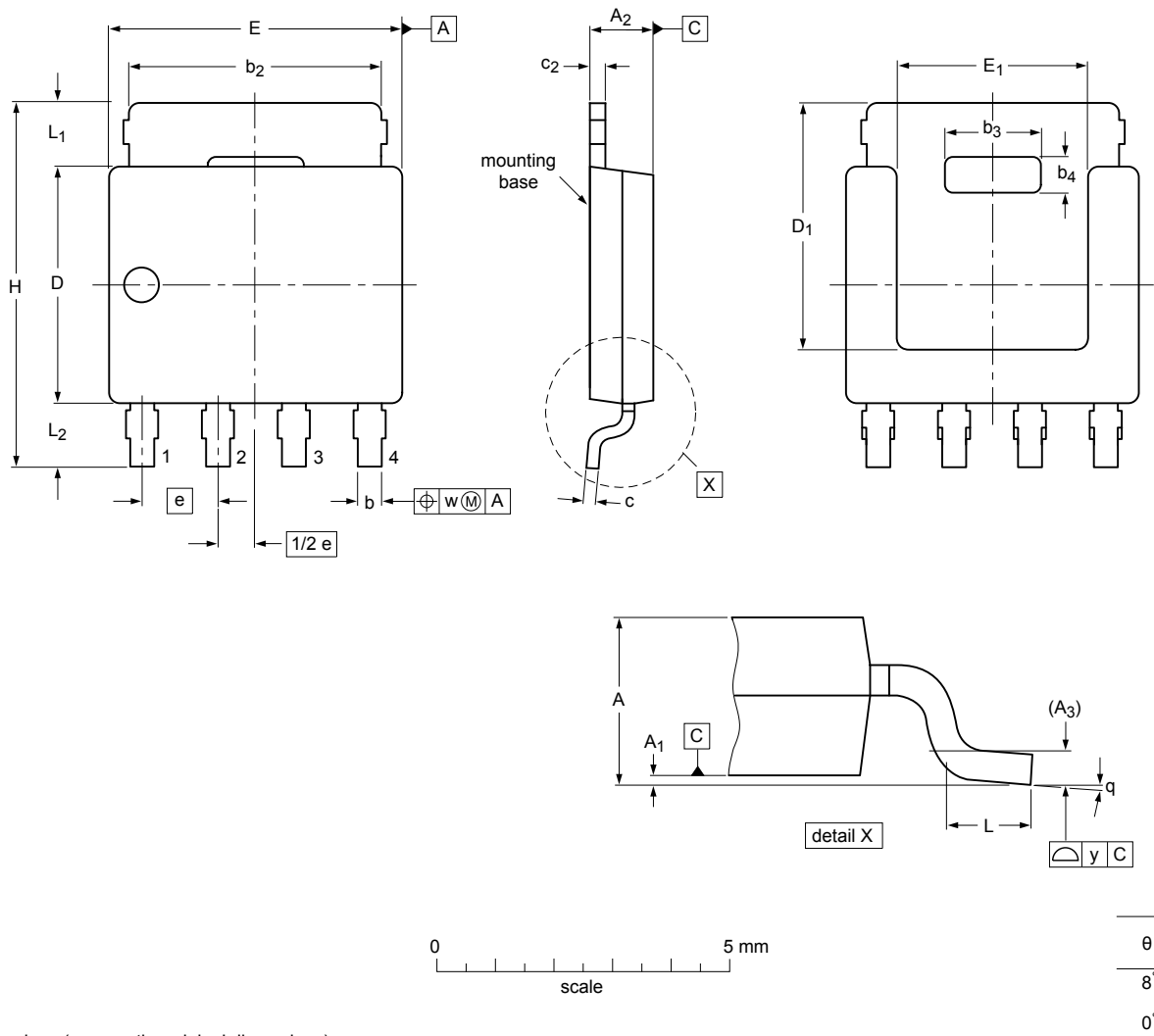


Fig. 14. Source current as a function of source-drain voltage; typical values

$$T_j = 25^\circ C \text{ and } 150^\circ C; V_{GS} = 0V$$

11. Package outline

Plastic single-ended surface-mounted package (LPAK56; Power-SO8); 4 leads SOT669



Dimensions (mm are the original dimensions)

Unit ⁽¹⁾	A	A ₁	A ₂	A ₃	b	b ₂	b ₃	b ₄	c	c ₂	D ⁽¹⁾	D ₁ ⁽¹⁾	E ⁽¹⁾	E ₁ ⁽¹⁾	e	H	L	L ₁	L ₂	w	y
max	1.20	0.15	1.10		0.50	4.41	2.2	0.9	0.25	0.30	4.10	4.20	5.0	3.3	1.27	6.2	0.85	1.3	1.3		
nom				0.25																0.25	0.1
min	1.01	0.00	0.95		0.35	3.62	2.0	0.7	0.19	0.24	3.80		4.8	3.1		5.8	0.40	0.8	0.8		

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

sot669_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT669		MO-235				11-03-25 13-02-27

Fig. 15. Package outline LPAK56; Power-SO8 (SOT669)

12. Legal information

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