



# PSMN0R9-25YLD

N-channel 25 V, 0.85 m $\Omega$ , 300 A logic level MOSFET in LFPAK56 using NextPowerS3 Technology

27 April 2016

Product data sheet

## 1. General description

Logic level gate drive N-channel enhancement mode MOSFET in LFPAK56 package. NextPowerS3 portfolio utilising Nexperia's unique "SchottkyPlus" technology delivers high efficiency, low spiking performance usually associated with MOSFETs with an integrated Schottky or Schottky-like diode but without problematic high leakage current. NextPowerS3 is particularly suited to high efficiency applications at high switching frequencies.

## 2. Features and benefits

- 100% Avalanche tested at  $I_{(AS)} = 190$  A
- Ultra low  $Q_G$ ,  $Q_{GD}$  and  $Q_{OSS}$  for high system efficiency, especially at higher switching frequencies
- Superfast switching with soft-recovery
- Low spiking and ringing for low EMI designs
- Unique "SchottkyPlus" technology; Schottky-like performance with  $< 1$   $\mu$ A leakage at 25 °C
- Optimised for 4.5 V gate drive
- Low parasitic inductance and resistance
- High reliability clip bonded and solder die attach Power SO8 package; no glue, no wire bonds, qualified to 175 °C
- Wave solderable; exposed leads for optimal visual solder inspection

## 3. Applications

- On-board DC:DC solutions for server and telecommunications
- Secondary-side synchronous rectification in telecommunication applications
- Voltage regulator modules (VRM)
- Point-of-Load (POL) modules
- Power delivery for V-core, ASIC, DDR, GPU, VGA and system components
- Brushed and brushless motor control
- Power OR-ing

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$		-	-	25	V
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 2</a>	[1]	-	-	300	A

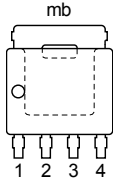
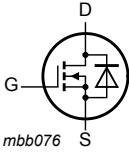
**N-channel 25 V, 0.85 mΩ, 300 A logic level MOSFET in LFAK56 using  
NextPowerS3 Technology**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 1</a>	-	-	238	W
$T_j$	junction temperature		-55	-	175	°C
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 10</a>	-	0.96	1.2	mΩ
		$V_{GS} = 10\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 10</a>	-	0.72	0.85	mΩ
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 25\text{ A}$ ; $V_{DS} = 12\text{ V}$ ; $V_{GS} = 10\text{ V}$ ; <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>	-	89.8	-	nC
		$I_D = 25\text{ A}$ ; $V_{DS} = 12\text{ V}$ ; $V_{GS} = 4.5\text{ V}$ ; <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>	-	41.5	-	nC
		$I_D = 0\text{ A}$ ; $V_{DS} = 0\text{ V}$ ; $V_{GS} = 0\text{ V}$	-	47.2	-	nC
$Q_{GD}$	gate-drain charge	$I_D = 25\text{ A}$ ; $V_{DS} = 12\text{ V}$ ; $V_{GS} = 4.5\text{ V}$ ; <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>	-	9.9	-	nC
<b>Source-drain diode</b>						
S	softness factor	$I_S = 25\text{ A}$ ; $di_S/dt = -100\text{ A}/\mu\text{s}$ ; $V_{GS} = 0\text{ V}$ ; $V_{DS} = 12\text{ V}$ ; <a href="#">Fig. 16</a>	-	0.8	-	

[1] 300A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB thermal design and operating temperature.

## 5. Pinning information

**Table 2. Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p style="text-align: center;"><b>LFAK56; Power-SO8 (SOT669)</b></p>	 <p style="text-align: center;"><i>mbb076</i></p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

## 6. Ordering information

**Table 3. Ordering information**

Type number	Package		
	Name	Description	Version
PSMN0R9-25YLD	LFAK56; Power-SO8	Plastic single-ended surface-mounted package (LFAK56; Power-SO8); 4 leads	SOT669

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN0R9-25YLD	0D925L

## 8. Limiting values

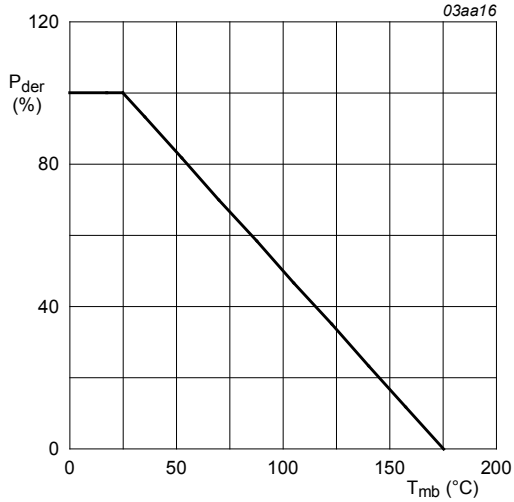
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$		-	25	V
$V_{DGR}$	drain-gate voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$		-	25	V
$V_{GS}$	gate-source voltage			-20	20	V
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 1</a>		-	238	W
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 2</a>	[1]	-	300	A
		$V_{GS} = 10\text{ V}$ ; $T_{mb} = 100\text{ °C}$ ; <a href="#">Fig. 2</a>		-	285	A
$I_{DM}$	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 3</a>		-	1614	A
$T_{stg}$	storage temperature			-55	175	°C
$T_j$	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
$V_{ESD}$	electrostatic discharge voltage	HBM		2000	-	V
<b>Source-drain diode</b>						
$I_S$	source current	$T_{mb} = 25\text{ °C}$		-	198	A
$I_{SM}$	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$		-	1614	A
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 25\text{ A}$ ; $V_{sup} \leq 25\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; $V_{GS} = 10\text{ V}$ ; $T_{j(init)} = 25\text{ °C}$ ; unclamped; $t_p = 8.2\text{ ms}$	[2]	-	3343	mJ
$I_{AS}$	non-repetitive avalanche current	$V_{sup} \leq 25\text{ V}$ ; $V_{GS} = 10\text{ V}$ ; $T_{j(init)} = 25\text{ °C}$ ; $R_{GS} = 50\text{ }\Omega$	[2]	-	190	A

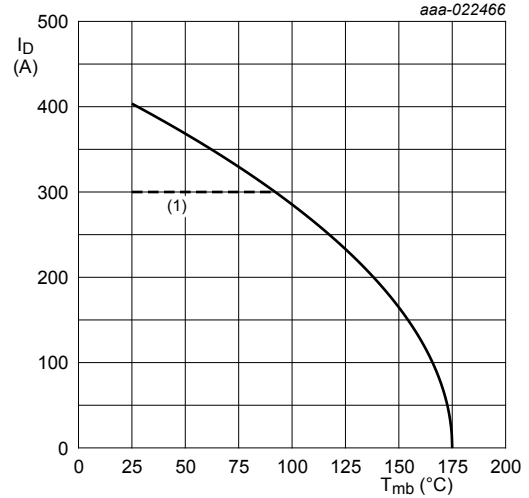
[1] 300A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB thermal design and operating temperature.

[2] Protected by 100% test



**Fig. 1. Normalized total power dissipation as a function of mounting base temperature**

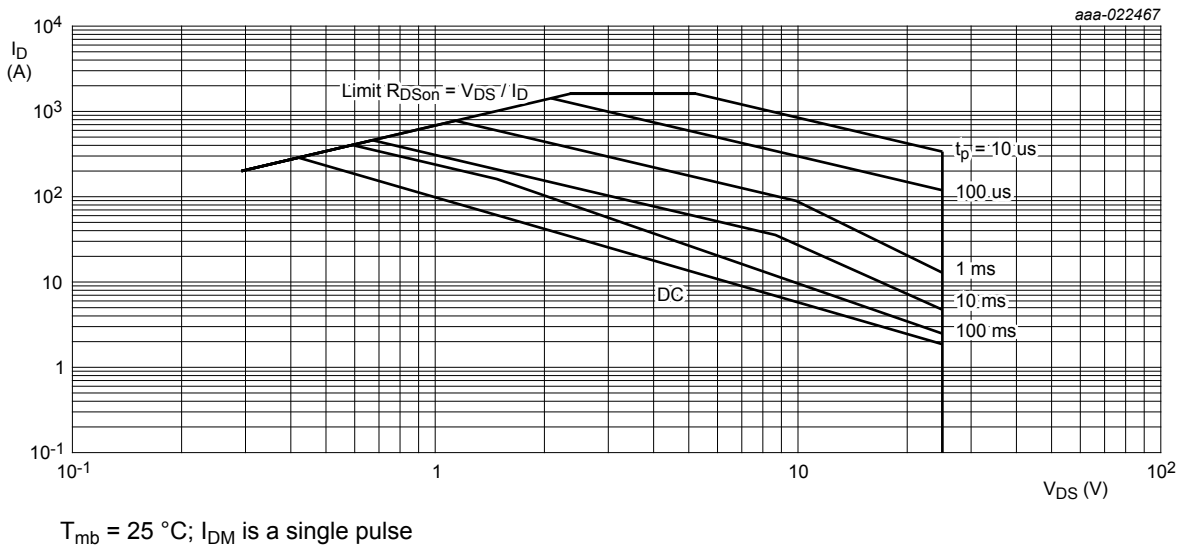
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$



$V_{GS} \geq 10\text{ V}$

(1) 300A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB thermal design and operating temperature.

**Fig. 2. Continuous drain current as a function of mounting base temperature**



**Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**

## 9. Thermal characteristics

**Table 6. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	<a href="#">Fig. 4</a>	-	0.56	0.63	K/W

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	<a href="#">Fig. 5</a>	-	50	-	K/W
		<a href="#">Fig. 6</a>	-	125	-	K/W

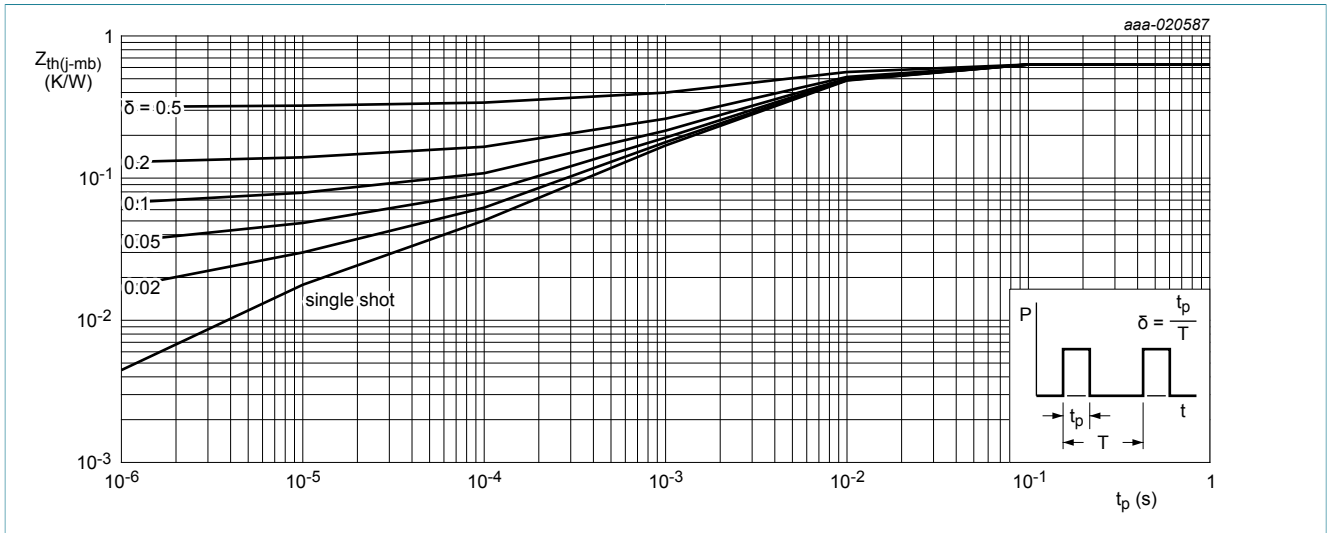


Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

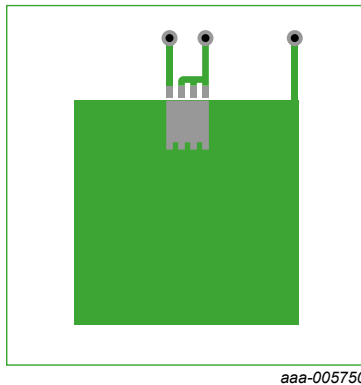


Fig. 5. PCB layout for thermal resistance junction to ambient 1" square pad; FR4 Board; 2oz copper

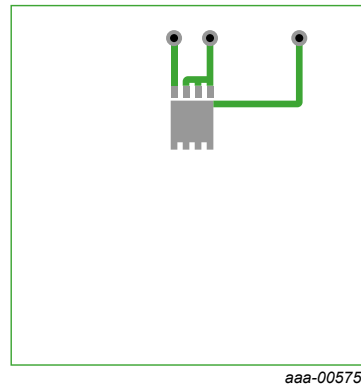


Fig. 6. PCB layout for thermal resistance junction to ambient minimum footprint; FR4 Board; 2oz copper

## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	25	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	22.5	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$	1.2	1.73	2.2	V

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-5.1	-	mV/K
$I_{DSS}$	drain leakage current	$V_{DS} = 20\text{ V}; V_{GS} = 0\text{ V}; T_j = 25\text{ °C}$	-	-	1	μA
		$V_{DS} = 20\text{ V}; V_{GS} = 0\text{ V}; T_j = 125\text{ °C}$	-	30	-	μA
$I_{GSS}$	gate leakage current	$V_{GS} = 20\text{ V}; V_{DS} = 0\text{ V}; T_j = 25\text{ °C}$	-	-	100	nA
		$V_{GS} = -20\text{ V}; V_{DS} = 0\text{ V}; T_j = 25\text{ °C}$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C};$ <a href="#">Fig. 10</a>	-	0.96	1.2	mΩ
		$V_{GS} = 4.5\text{ V}; I_D = 25\text{ A}; T_j = 175\text{ °C};$ <a href="#">Fig. 10; Fig. 11</a>	-	-	2.04	mΩ
		$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C};$ <a href="#">Fig. 10</a>	-	0.72	0.85	mΩ
		$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 175\text{ °C};$ <a href="#">Fig. 10; Fig. 11</a>	-	-	1.45	mΩ
$R_G$	gate resistance	$f = 1\text{ MHz}$	-	1.16	-	Ω
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 25\text{ A}; V_{DS} = 12\text{ V}; V_{GS} = 10\text{ V};$ <a href="#">Fig. 12; Fig. 13</a>	-	89.8	-	nC
		$I_D = 25\text{ A}; V_{DS} = 12\text{ V}; V_{GS} = 4.5\text{ V};$ <a href="#">Fig. 12; Fig. 13</a>	-	41.5	-	nC
		$I_D = 0\text{ A}; V_{DS} = 0\text{ V}; V_{GS} = 0\text{ V}$	-	47.2	-	nC
$Q_{GS}$	gate-source charge	$I_D = 25\text{ A}; V_{DS} = 12\text{ V}; V_{GS} = 4.5\text{ V};$ <a href="#">Fig. 12; Fig. 13</a>	-	15.8	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	9.7	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	6.1	-	nC
$Q_{GD}$	gate-drain charge		-	9.9	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25\text{ A}; V_{DS} = 12\text{ V};$ <a href="#">Fig. 12; Fig. 13</a>	-	2.7	-	V
$C_{iss}$	input capacitance	$V_{DS} = 12\text{ V}; V_{GS} = 0\text{ V}; f = 1\text{ MHz};$ $T_j = 25\text{ °C};$ <a href="#">Fig. 14</a>	-	6721	-	pF
$C_{oss}$	output capacitance		-	2390	-	pF
$C_{rss}$	reverse transfer capacitance		-	418	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 12\text{ V}; R_L = 0.6\text{ Ω}; V_{GS} = 4.5\text{ V};$ $R_{G(ext)} = 5\text{ Ω}$	-	37.9	-	ns
$t_r$	rise time		-	42	-	ns
$t_{d(off)}$	turn-off delay time		-	39.2	-	ns
$t_f$	fall time		-	27.9	-	ns
$Q_{oss}$	output charge	$V_{GS} = 0\text{ V}; V_{DS} = 12\text{ V}; f = 1\text{ MHz}$	-	44	-	nC

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25\text{ A}$ ; $V_{GS} = 0\text{ V}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 15</a>	-	0.78	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 25\text{ A}$ ; $dI_S/dt = -100\text{ A}/\mu\text{s}$ ; $V_{GS} = 0\text{ V}$ ;	-	44	-	ns
$Q_r$	recovered charge	$V_{DS} = 12\text{ V}$ ; <a href="#">Fig. 16</a>	[1]	54.4	-	nC
$t_a$	reverse recovery rise time		-	24.2	-	ns
$t_b$	reverse recovery fall time		-	19.8	-	ns
S	softness factor		-	0.8	-	

[1] includes capacitive recovery

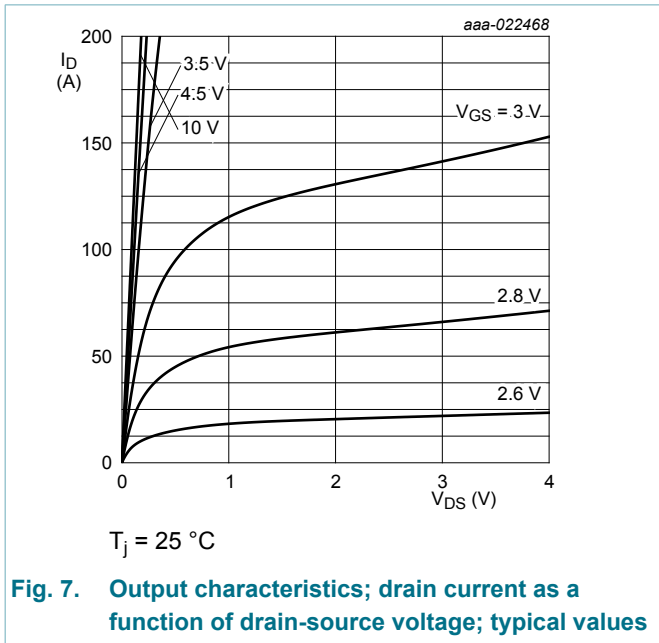


Fig. 7. Output characteristics; drain current as a function of drain-source voltage; typical values

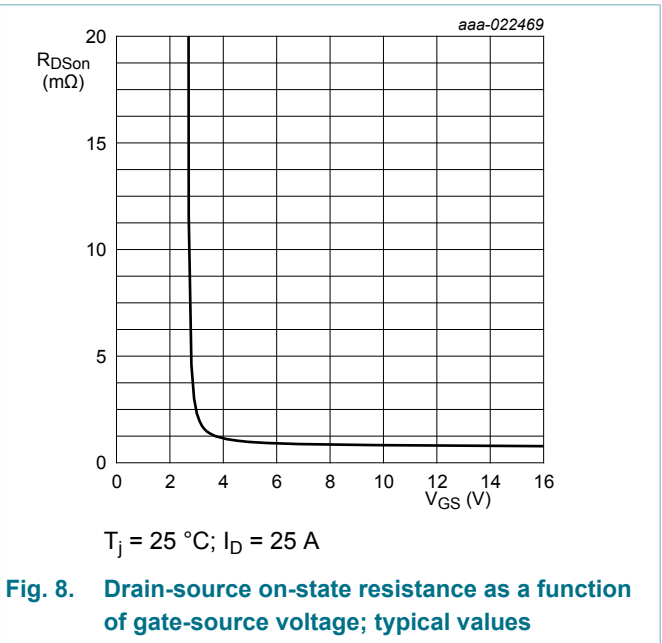


Fig. 8. Drain-source on-state resistance as a function of gate-source voltage; typical values

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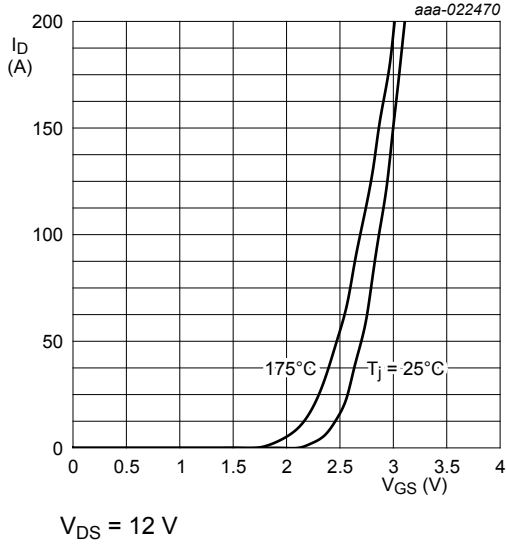


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

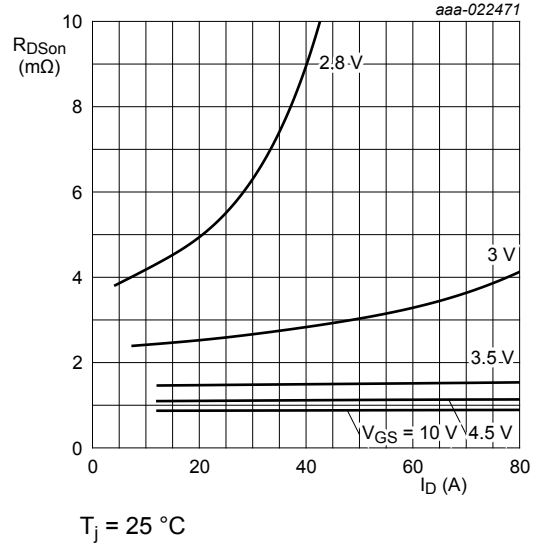


Fig. 10. Drain-source on-state resistance as a function of drain current; typical values

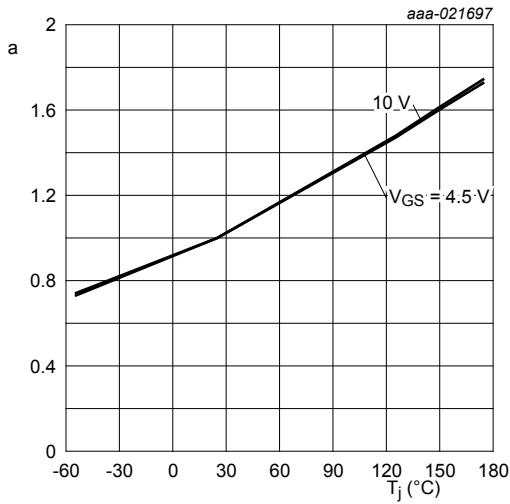


Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

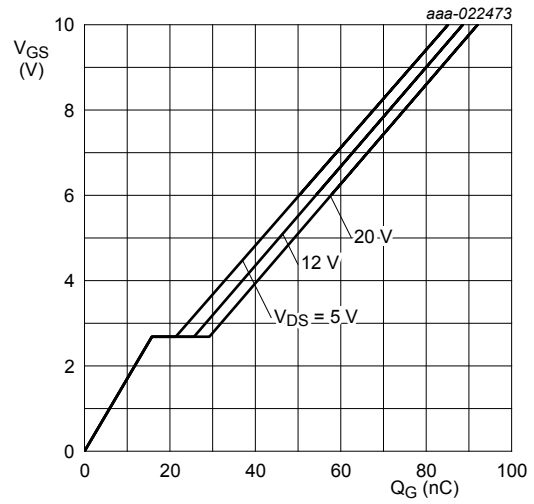


Fig. 12. Gate-source voltage as a function of gate charge; typical values



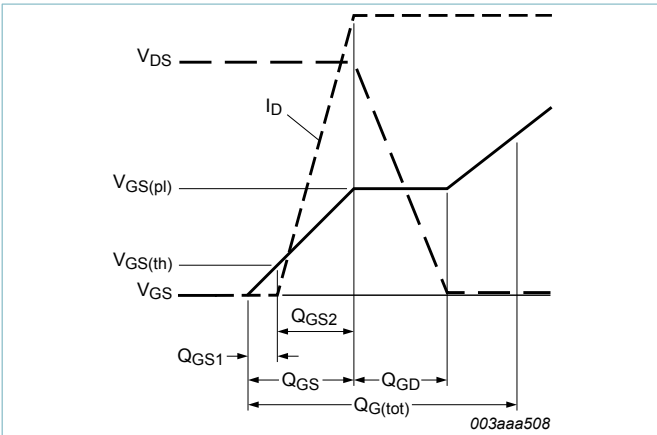
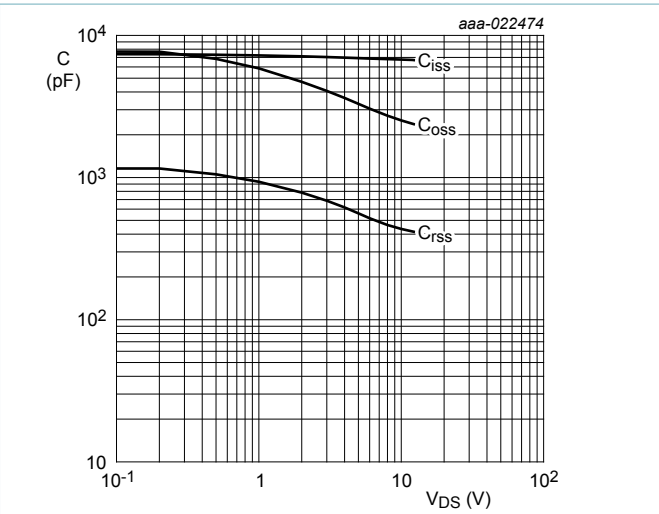
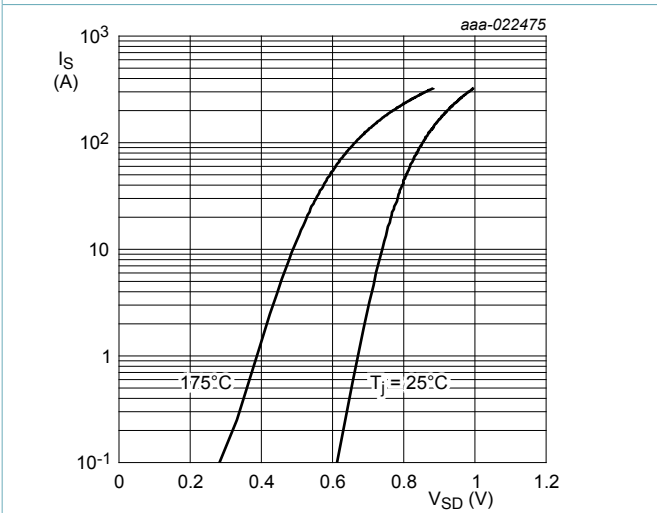


Fig. 13. Gate charge waveform definitions



$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$   
Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0 \text{ V}$   
Fig. 15. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

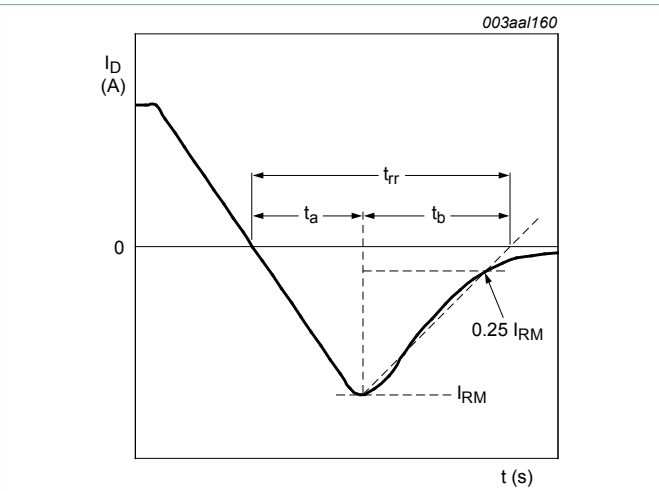


Fig. 16. Reverse recovery timing definition

### 11. Package outline

Plastic single-ended surface-mounted package (LPAK56; Power-SO8); 4 leads SOT669



Dimensions (mm are the original dimensions)

Unit <sup>(1)</sup>	A	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b	b <sub>2</sub>	b <sub>3</sub>	b <sub>4</sub>	c	c <sub>2</sub>	D <sup>(1)</sup>	D <sub>1</sub> <sup>(1)</sup>	E <sup>(1)</sup>	E <sub>1</sub> <sup>(1)</sup>	e	H	L	L <sub>1</sub>	L <sub>2</sub>	w	y
max	1.20	0.15	1.10		0.50	4.41	2.2	0.9	0.25	0.30	4.10	4.20	5.0	3.3		6.2	0.85	1.3	1.3		
nom				0.25											1.27					0.25	0.1
min	1.01	0.00	0.95		0.35	3.62	2.0	0.7	0.19	0.24	3.80		4.8	3.1		5.8	0.40	0.8	0.8		

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

sot669\_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT669		MO-235				-11-03-25- 13-02-27

Fig. 17. Package outline LPAK56; Power-SO8 (SOT669)

## 12. Legal information

### 12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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