

N-channel 30 V 1.3 m Ω logic level MOSFET in LFPAK

Rev. 02 — 25 June 2009

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel MOSFET in LFPAK package qualified to 150 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- Advanced TrenchMOS provides low RDSon and low gate charge
- High efficiency gains in switching power convertors

1.3 Applications

- DC-to-DC converters
- Lithium-ion battery protection
- Load switching

1.4 Quick reference data

Table 1. Quick reference

- Improved mechanical and thermal characteristics
- LFPAK provides maximum power density in a Power SO8 package
- Motor control
- Server power supplies

SymbolParameterConditionsMinTypMax V_{DS} drain-source voltage $T_j \ge 25 ^{\circ}C; T_j \le 150 ^{\circ}C$ 30 I_D drain current $T_{mb} = 25 ^{\circ}C; V_{GS} = 10 V;$ [1]100 P_{tot} total power dissipation $T_{mb} = 25 ^{\circ}C;$ see Figure 2 $T_mb = 25 ^{\circ}C;$ see Figure 2121 T_j junction temperature55-150Avalanche ruggednessV_{GS} = 10 V; $T_{j(init)} = 25 ^{\circ}C;$ $I_D = 100 A; V_{sup} \le 30 V;$ $R_{GS} = 50 \Omega;$ unclampedMaxDynamic characteristics383	
$ I_D \qquad drain current \qquad T_{mb} = 25 \ ^{\circ}C; \ V_{GS} = 10 \ V; \qquad [1] \qquad - \qquad 100 \\ see \ Figure \ 1; \qquad \qquad I_D \qquad see \ Figure \ 1; \qquad \qquad - \qquad 121 \\ T_{i} \qquad total power \\ dissipation \qquad T_{mb} = 25 \ ^{\circ}C; \ see \ Figure \ 2 \\ I_D = 100 \ A; \ V_{sup} \le 30 \ V; \\ avalanche \ energy \qquad R_{GS} = 50 \ \Omega; \ unclamped \qquad \qquad - \qquad - \qquad 383 \\ Dynamic \ characteristics \qquad \qquad - \qquad - \qquad - \qquad 383 \\ Dynamic \ characteristics \qquad \qquad - $	Unit
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	V
$\begin{tabular}{lllllllllllllllllllllllllllllllllll$	A
Avalanche ruggedness $E_{DS(AL)S}$ non-repetitive drain-source avalanche energy $V_{GS} = 10 \text{ V}; \text{ T}_{j(init)} = 25 \text{ °C}; - 383$ $I_D = 100 \text{ A}; \text{ V}_{sup} \le 30 \text{ V};$ avalanche energy $R_{GS} = 50 \Omega;$ unclampedDynamic characteristics	W
	°C
$\begin{array}{ll} \mbox{drain-source} & I_D = 100 \mbox{ A}; \mbox{V}_{sup} \leq 30 \mbox{ V}; \\ \mbox{avalanche energy} & R_{GS} = 50 \Omega; \mbox{ unclamped} \end{array}$	
	mJ
Q_{GD} gate-drain charge V_{GS} = 4.5 V; I_D = 25 A; - 9.3 -	nC
$Q_{G(tot)}$ total gate charge $V_{DS} = 12 V$; see Figure 13; see Figure 14 - 46.6 -	nC

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Table 1.	. Quick reference continued					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static ch	naracteristics					
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I _D = 15 A; T _j = 100 °C; see <u>Figure 12</u>	-	-	1.8	mΩ
		V _{GS} = 10 V; I _D = 15 A; T _j = 25 °C; see <u>Figure 17</u>	-	1.04	1.3	mΩ

[1] Continuous current is limited by package.

2. Pinning information

Table 2.	Pinning	information		
Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		-
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain	SOT1023 (LFPAK2)	mbb076 Ś

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN1R3-30YL	LFPAK2	Plastic single-ende surface-mounted package (LFPAK2); 4 leads	SOT1023

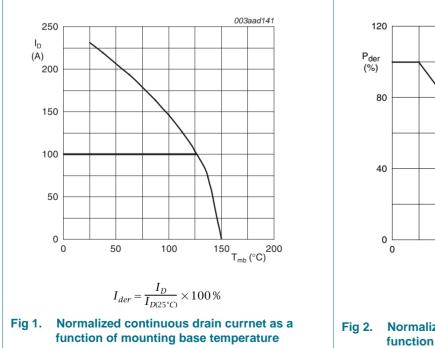
4. Limiting values

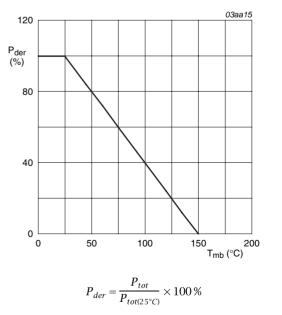
Table 4.Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 150 °C		-	30	V
V _{DGR}	drain-gate voltage	$T_j \ge 25 \text{ °C}; T_j \le 150 \text{ °C}; R_{GS} = 20 \text{ k}\Omega$		-	30	V
V _{GS}	gate-source voltage			-20	20	V
I _D	drain current	V _{GS} = 10 V; T _{mb} = 100 °C; see <u>Figure 1</u>	[1]	-	100	А
		V_{GS} = 10 V; T_{mb} = 25 °C; see <u>Figure 1</u>	[1]	-	100	А
I _{DM}	peak drain current	$t_p \le 10 \ \mu s$; pulsed; $T_{mb} = 25 \ ^{\circ}C$; see Figure 3		-	923	А
P _{tot}	total power dissipation	T _{mb} = 25 °C; see <u>Figure 2</u>		-	121	W
T _{stg}	storage temperature			-55	150	°C
Tj	junction temperature			-55	150	°C
T _{sld(M)}	peak soldering temperature			-	260	°C
Source-dr	ain diode					
I _S	source current	T _{mb} = 25 °C;	[1]	-	100	А
I _{SM}	peak source current	$t_p \le 10 \ \mu s$; pulsed; $T_{mb} = 25 \ ^{\circ}C$		-	923	А
Avalanche	e ruggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_{D} = 100 A; V_{sup} \leq 30 V; R_{GS} = 50 $\Omega;$ unclamped		-	383	mJ

[1] Continuous current is limited by package.

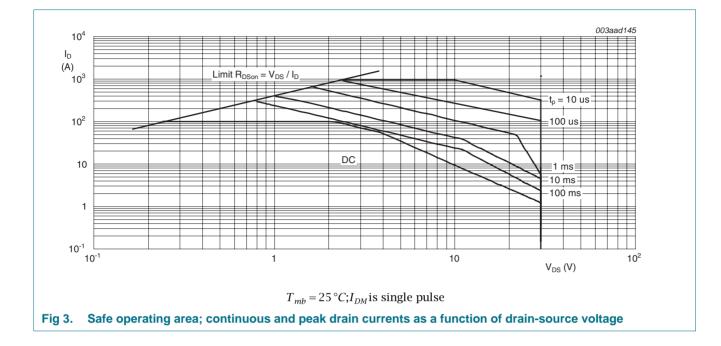






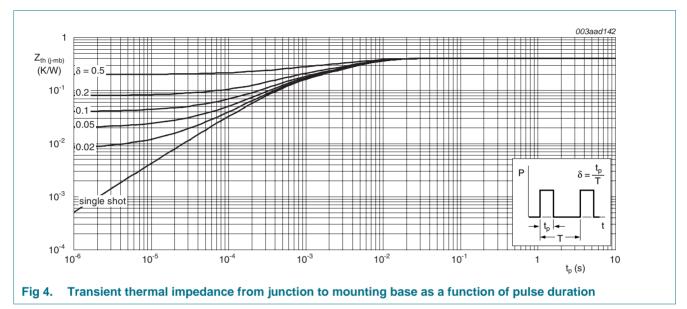
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5. Thermal characteristics

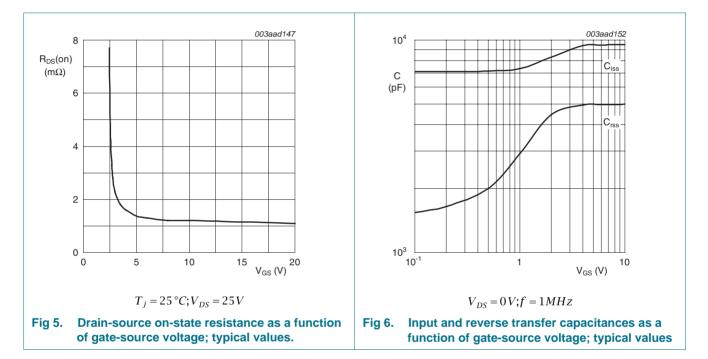
Table 5.	Thermal characteristics					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R _{th(j-mb)}	thermal resistance from junction to mounting base	see <u>Figure 4</u>	-	0.4	1.03	K/W



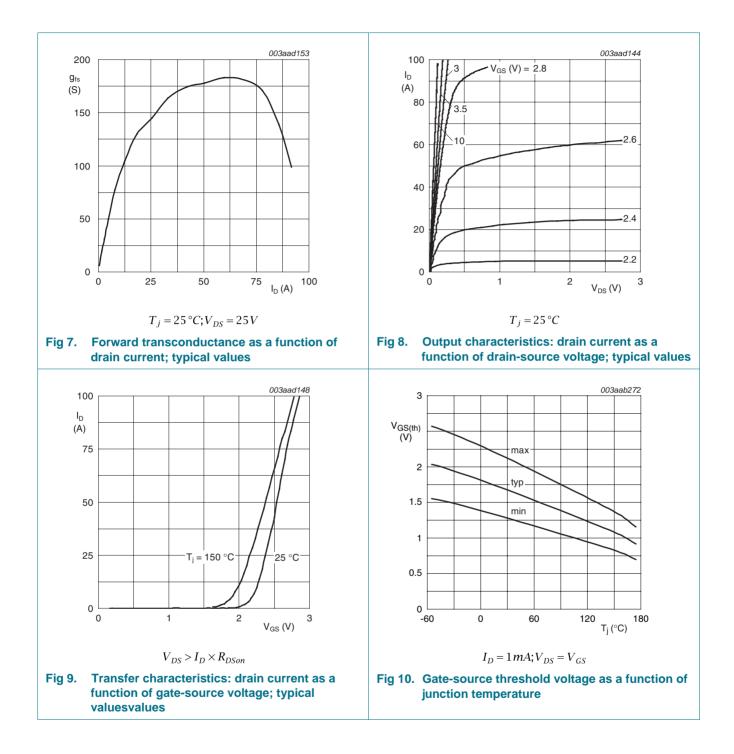
6. Characteristics

Table 6.	Characteristics					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static cha	racteristics					
V _{(BR)DSS}	drain-source	$I_D = 250 \ \mu A; \ V_{GS} = 0 \ V; \ T_j = 25 \ ^\circ C$	30	-	-	V
	breakdown voltage	$I_D = 250 \ \mu A; \ V_{GS} = 0 \ V; \ T_j = -55 \ ^\circ C$	27	-	-	V
V _{GS(th)}	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ °C};$ see <u>Figure 10</u> ; see <u>Figure 11</u>	1.3	1.7	2.15	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 150 \text{ °C};$ see <u>Figure 10</u>	0.65	-	-	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = -55 °C; see <u>Figure 10</u>	-	-	2.45	V
DSS	drain leakage current	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	1	μΑ
		$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ °C}$	-	-	100	μΑ
I _{GSS}	gate leakage current	V_{GS} = 15 V; V_{DS} = 0 V; T_j = 25 °C	-	-	100	nA
		V_{GS} = -15 V; V_{DS} = 0 V; T_j = 25 °C	-	-	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 4.5 V; I _D = 15 A; T _j = 25 °C; see <u>Figure 17</u>	-	1.43	1.95	mΩ
		V _{GS} = 10 V; I _D = 15 A; T _j = 100 °C; see <u>Figure 12</u>	-	-	1.8	mΩ
		V _{GS} = 10 V; I _D = 15 A; T _j = 150 °C; see <u>Figure 12</u>	-	1.9	2.8	mΩ
		V _{GS} = 10 V; I _D = 15 A; T _j = 25 °C; see <u>Figure 17</u>	-	1.04	1.3	mΩ
R _G	gate resistance	f = 1 MHz	-	0.89	-	Ω
Dynamic	characteristics					
Q _{G(tot)}	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 12 \text{ V}; V_{GS} = 10 \text{ V};$ see <u>Figure 13</u> ; see <u>Figure 14</u>	-	100	-	nC
		$I_D = 0 \text{ A}; \text{ V}_{DS} = 0 \text{ V}; \text{ V}_{GS} = 10 \text{ V}$	-	90	-	nC
		$I_D = 25 \text{ A}; V_{DS} = 12 \text{ V}; V_{GS} = 4.5 \text{ V};$ see <u>Figure 13</u> ; see <u>Figure 14</u>	-	46.6	-	nC
Q _{GS}	gate-source charge	$I_D = 25 \text{ A}; V_{DS} = 12 \text{ V}; V_{GS} = 4.5 \text{ V};$ see Figure 13; see Figure 14	-	17.9	-	nC
Q _{GS(th)}	pre-threshold gate-source charge	I_D = 25 A; V_{DS} = 12 V; V_{GS} = 4.5 V; see <u>Figure 13</u>	-	11	-	nC
Q _{GS(th-pl)}	post-threshold gate-source charge		-	6.9	-	nC
Q _{GD}	gate-drain charge	$I_D = 25 \text{ A}; V_{DS} = 12 \text{ V}; V_{GS} = 4.5 \text{ V};$ see <u>Figure 13</u> ; see <u>Figure 14</u>	-	9.3	-	nC
V _{GS(pl)}	gate-source plateau voltage	$V_{DS} = 12 \text{ V}$; see <u>Figure 13</u> ; see <u>Figure 14</u>	-	2.53	-	V
C _{iss}	input capacitance	V_{DS} = 12 V; V_{GS} = 0 V; f = 1 MHz;	-	6227	-	pF
C _{oss}	output capacitance	T _j = 25 °C; see <u>Figure 15</u>	-	1415	-	pF
C _{rss}	reverse transfer capacitance		-	619	-	pF

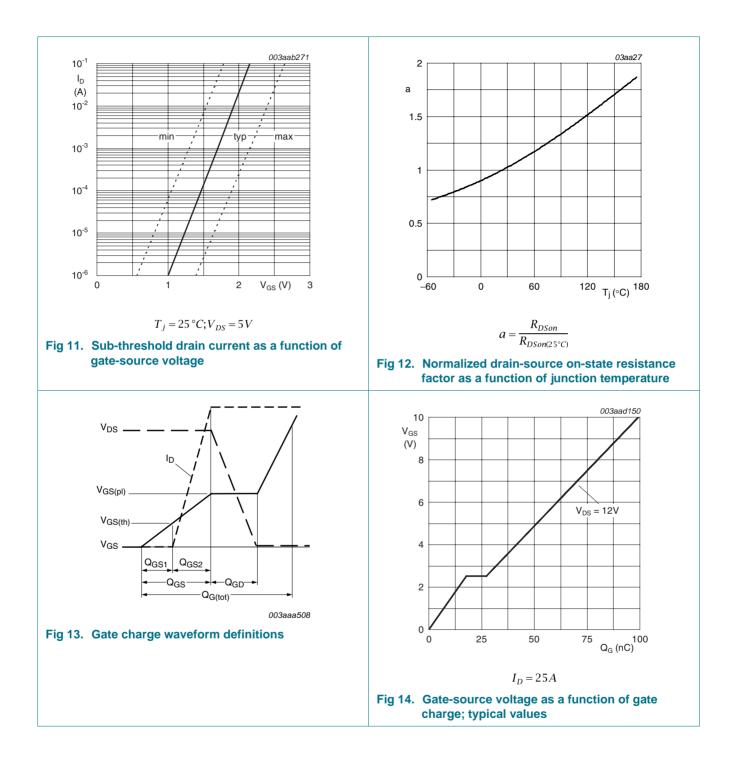
Table 6.	Characteristics continued					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
t _{d(on)}	turn-on delay time	$V_{DS} = 12 \text{ V}; \text{ R}_L = 0.5 \ \Omega; \text{ V}_{GS} = 4.5 \text{ V};$	-	64	-	ns
t _r	rise time	$R_{G(ext)} = 5.6 \Omega$	-	108	-	ns
t _{d(off)}	turn-off delay time		-	106	-	ns
t _f	fall time		-	52	-	ns
Source-d	rain diode					
V_{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; T _j = 25 °C; see <u>Figure 16</u>	-	0.88	1.2	V
t _{rr}	reverse recovery time	$I_{S} = 20 \text{ A}; \text{ d}I_{S}/\text{d}t = -100 \text{ A/s}; \text{ V}_{GS} = 0 \text{ V};$	-	46	-	ns
Qr	recovered charge	$V_{\rm DS} = 20 \ V$	-	53	-	nC

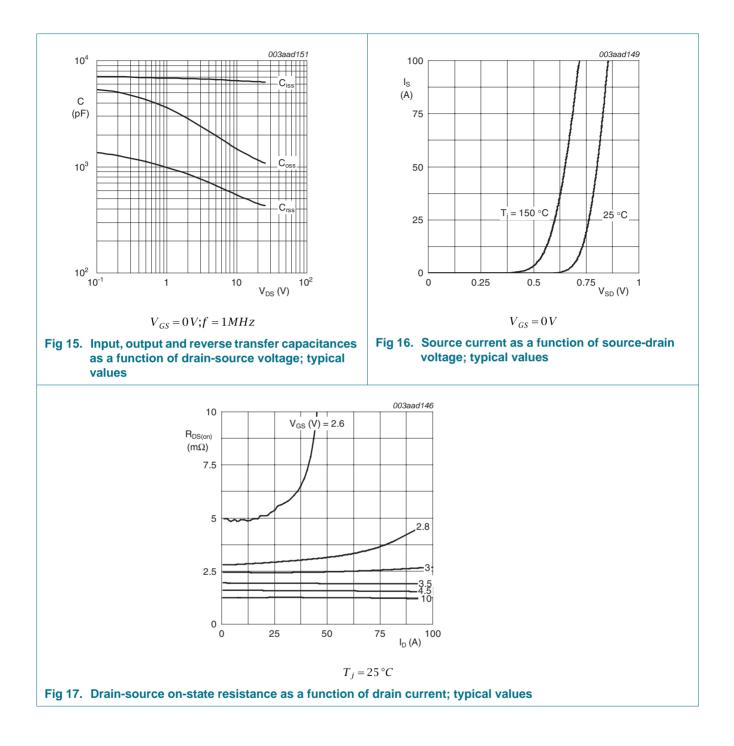


N-channel 30 V 1.3 mΩ logic level MOSFET in LFPAK



PSMN1R3-30YL_2





N-channel 30 V 1.3 m Ω logic level MOSFET in LFPAK

7. Package outline

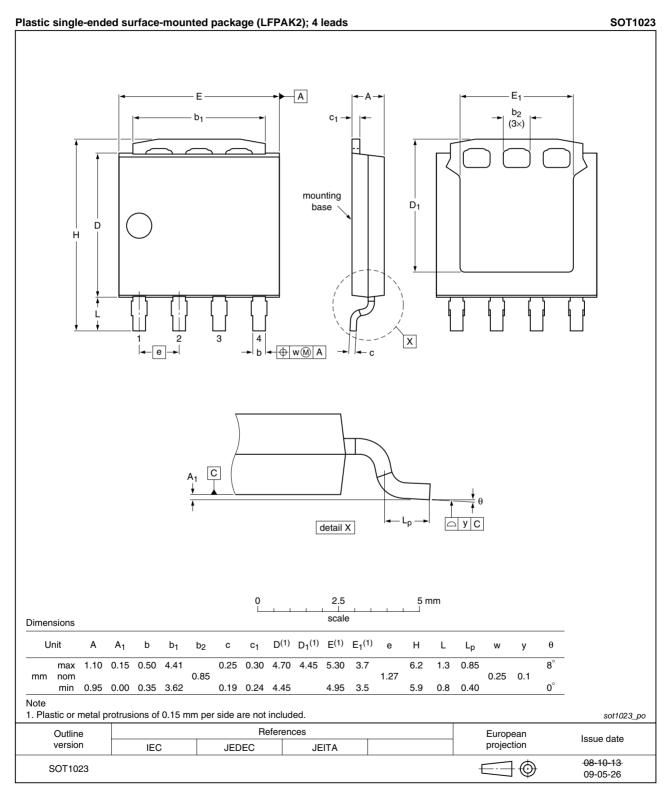


Fig 18. Package outline SOT1023; Package outline

8. Revision history

Table 7.Revision history

	-			
Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN1R3-30YL_2	20090625	Product data sheet	-	PSMN2R3-30YL_1
Modifications:	 Status char 	nged from objective to pr	oduct.	
	 Various cha 	anges to content.		
PSMN1R3-30YL_1	20090528	Objective data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status [1][2]	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions"

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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