



PSMN1R5-30YL

N-channel 30 V 1.5 mΩ logic level MOSFET in LFPAK

Rev. 01 — 9 April 2010

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel MOSFET in LFPAK package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- Advanced TrenchMOS provides low R_{DSon} and low gate charge
- High efficiency gains in switching power convertors
- Improved mechanical and thermal characteristics
- LFPAK provides maximum power density in a Power SO8 package

1.3 Applications

- DC-to-DC converters
- Lithium-ion battery protection
- Load switching
- Motor control
- Server power supplies

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	-	30	V
I_D	drain current	$T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V};$ see [1] Figure 1	-	-	100	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C};$ see Figure 2	-	-	109	W
T_j	junction temperature		-55	-	175	°C
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 15\text{ A};$ $T_j = 100\text{ °C};$ see Figure 14	-	-	2.4	mΩ
		$V_{GS} = 10\text{ V}; I_D = 15\text{ A};$ $T_j = 25\text{ °C}$	-	1.3	1.5	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 4.5\text{ V}; I_D = 10\text{ A};$ $V_{DS} = 12\text{ V};$ see Figure 15 ; see Figure 16	-	8.7	-	nC

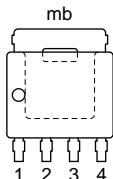
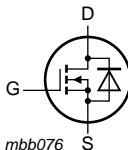
Table 1. Quick reference data ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$Q_{G(\text{tot})}$	total gate charge	$V_{GS} = 4.5 \text{ V}$; $I_D = 10 \text{ A}$; $V_{DS} = 12 \text{ V}$; see Figure 15	-	36.2	-	nC
Avalanche ruggedness						
$E_{DS(\text{AL})S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10 \text{ V}$; $T_{j(\text{init})} = 25 \text{ }^\circ\text{C}$; $I_D = 100 \text{ A}$; $V_{\text{sup}} \leq 30 \text{ V}$; $R_{GS} = 50 \text{ } \Omega$; unclamped	-	-	241	mJ

[1] Continuous current is limited by package.

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

SOT669 (LPAK)

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN1R5-30YL	LPAK	plastic single-ended surface-mounted package (LPAK); 4 leads	SOT669

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

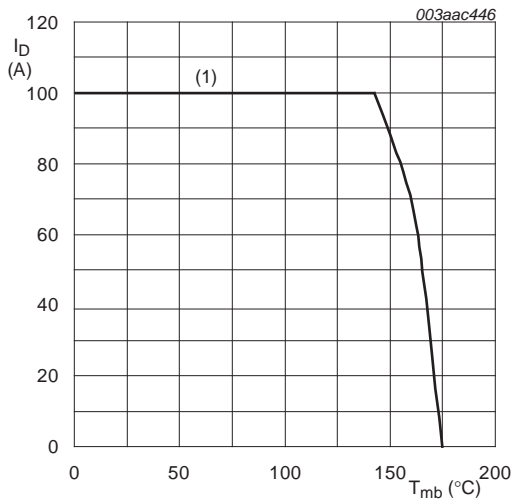
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	-	30	V
V_{DGR}	drain-gate voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	-	30	V
V_{GS}	gate-source voltage		-20	-	20	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; see Figure 1 [1]	-	-	100	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; see Figure 1 [1]	-	-	100	A
I_{DM}	peak drain current	$t_p \leq 10\text{ }\mu\text{s}$; pulsed; $T_{mb} = 25\text{ °C}$; see Figure 4	-	-	790	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	-	109	W
T_{stg}	storage temperature		-55	-	175	°C
T_j	junction temperature		-55	-	175	°C
Source-drain diode						
I_S	source current	$T_{mb} = 25\text{ °C}$ [1]	-	-	100	A
I_{SM}	peak source current	$t_p \leq 10\text{ }\mu\text{s}$; pulsed; $T_{mb} = 25\text{ °C}$	-	-	790	A
Avalanche ruggedness						
$E_{DS(AL)R}$	repetitive drain-source avalanche energy	see Figure 3 [2][3][4]	-	-	-	J
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ °C}$; $I_D = 100\text{ A}$; $V_{sup} \leq 30\text{ V}$; $R_{GS} = 50\text{ }\Omega$; unclamped	-	-	241	mJ

[1] Continuous current is limited by package.

[2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.

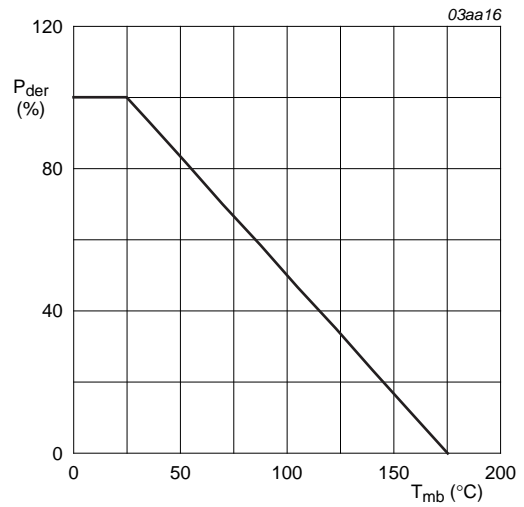
[3] Repetitive avalanche rating limited by average junction temperature of 170 °C.

[4] Refer to application note AN10273 for further information.



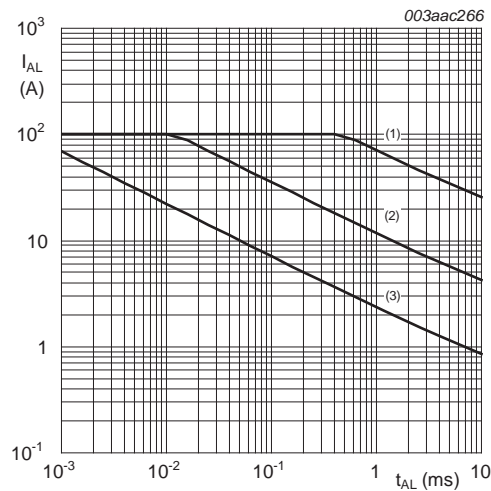
V_{GS} ≥ 10 V; (1) Capped at 100 A due to package

Fig 1. Continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



- (1) Single-pulse; T_j = 25 °C.
- (2) Single-pulse; T_j = 175 °C.
- (3) Repetitive.

Fig 3. Single-pulse and repetitive avalanche rating; avalanche current as a function of avalanche time

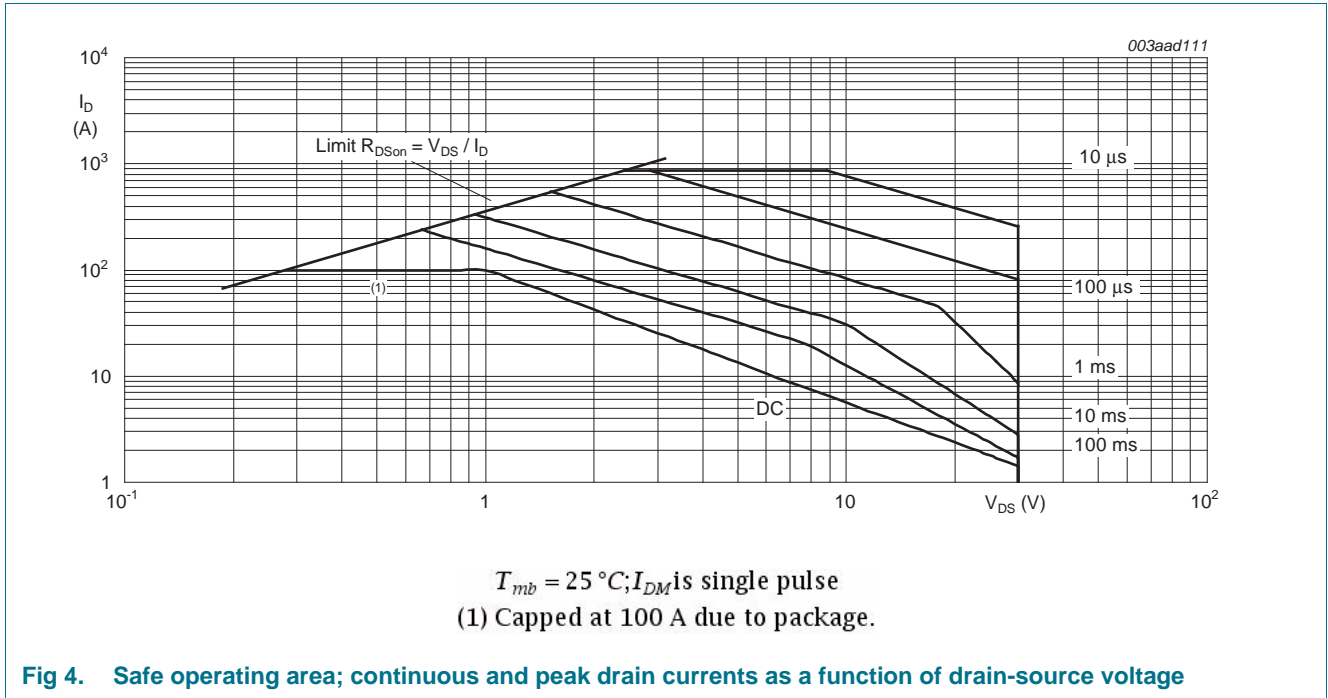


Fig 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 5	-	0.5	1.1	K/W

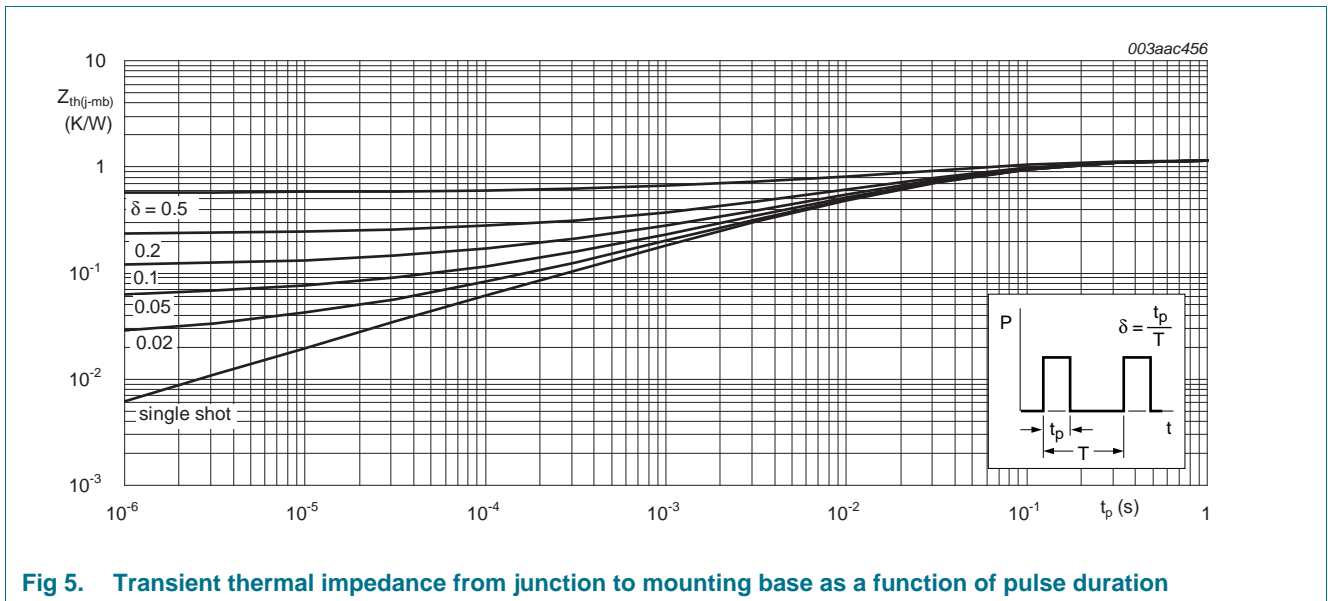


Fig 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 6. Characteristics
Tested to JEDEC standards where applicable.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 20\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ °C}; t_{av} = 100\text{ ns}$	35	-	-	V
		$I_D = 250\text{ }\mu\text{A}; V_{GS} = 0\text{ V}; T_j = 25\text{ °C}$	30	-	-	V
		$I_D = 250\text{ }\mu\text{A}; V_{GS} = 0\text{ V}; T_j = -55\text{ °C}$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}; V_{DS} = V_{GS}; T_j = 25\text{ °C};$ see Figure 12 ; see Figure 13	1.3	1.7	2.15	V
		$I_D = 1\text{ mA}; V_{DS} = V_{GS}; T_j = 150\text{ °C};$ see Figure 13	0.65	-	-	V
		$I_D = 1\text{ mA}; V_{DS} = V_{GS}; T_j = -55\text{ °C};$ see Figure 13	-	-	2.45	V
I_{DSS}	drain leakage current	$V_{DS} = 30\text{ V}; V_{GS} = 0\text{ V}; T_j = 25\text{ °C}$	-	-	1	μA
		$V_{DS} = 30\text{ V}; V_{GS} = 0\text{ V}; T_j = 150\text{ °C}$	-	-	100	μA
I_{GSS}	gate leakage current	$V_{GS} = 16\text{ V}; V_{DS} = 0\text{ V}; T_j = 25\text{ °C}$	-	-	100	nA
		$V_{GS} = -16\text{ V}; V_{DS} = 0\text{ V}; T_j = 25\text{ °C}$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}; I_D = 15\text{ A}; T_j = 25\text{ °C}$	-	1.8	1.9	mΩ
		$V_{GS} = 10\text{ V}; I_D = 15\text{ A}; T_j = 150\text{ °C};$ see Figure 14	-	-	2.8	mΩ
		$V_{GS} = 10\text{ V}; I_D = 15\text{ A}; T_j = 100\text{ °C};$ see Figure 14	-	-	2.4	mΩ
		$V_{GS} = 10\text{ V}; I_D = 15\text{ A}; T_j = 25\text{ °C}$	-	1.3	1.5	mΩ
R_G	gate resistance	$f = 1\text{ MHz}$	-	0.77	1.5	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 10\text{ A}; V_{DS} = 12\text{ V}; V_{GS} = 10\text{ V};$ see Figure 15 ; see Figure 16	-	77.9	-	nC
		$I_D = 0\text{ A}; V_{DS} = 0\text{ V}; V_{GS} = 10\text{ V}$	-	70	-	nC
		$I_D = 10\text{ A}; V_{DS} = 12\text{ V}; V_{GS} = 4.5\text{ V};$ see Figure 15	-	36.2	-	nC
Q_{GS}	gate-source charge	$I_D = 10\text{ A}; V_{DS} = 12\text{ V}; V_{GS} = 4.5\text{ V};$ see Figure 15 ; see Figure 16	-	11.6	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	8	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	3.6	-	nC
Q_{GD}	gate-drain charge		-	8.7	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$V_{DS} = 12\text{ V};$ see Figure 15 ; see Figure 16	-	2.34	-	V
C_{iss}	input capacitance	$V_{DS} = 12\text{ V}; V_{GS} = 0\text{ V}; f = 1\text{ MHz};$ $T_j = 25\text{ °C};$ see Figure 17	-	5057	-	pF
C_{oss}	output capacitance		-	1082	-	pF
C_{rss}	reverse transfer capacitance		-	398	-	pF

Table 6. Characteristics ...continued
 Tested to JEDEC standards where applicable.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	turn-on delay time	$V_{DS} = 12\text{ V}; R_L = 0.5\ \Omega; V_{GS} = 4.5\text{ V};$	-	46	-	ns
t_r	rise time	$R_{G(ext)} = 4.7\ \Omega$	-	72	-	ns
$t_{d(off)}$	turn-off delay time		-	76	-	ns
t_f	fall time		-	34	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C};$ see Figure 18	-	0.78	1.2	V
t_{rr}	reverse recovery time	$I_S = 20\text{ A}; dI_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$	-	45	-	ns
Q_r	recovered charge	$V_{DS} = 20\text{ V}$	-	56	-	nC

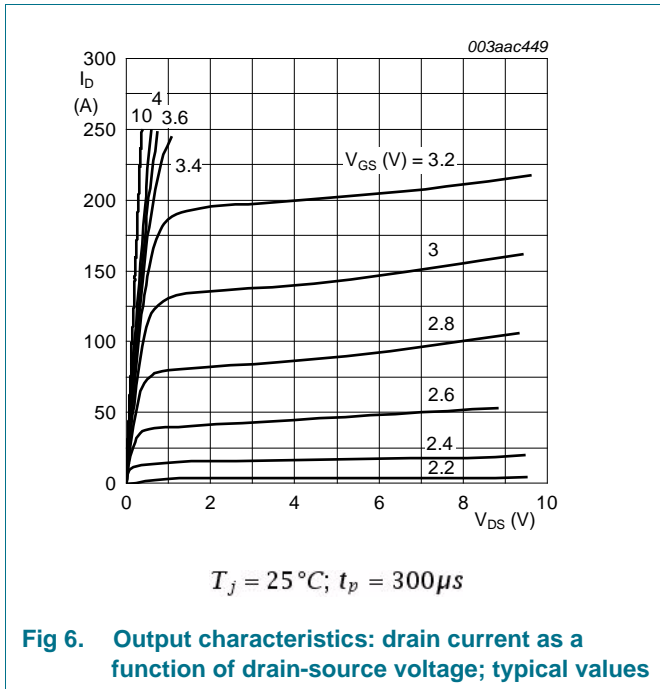


Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values

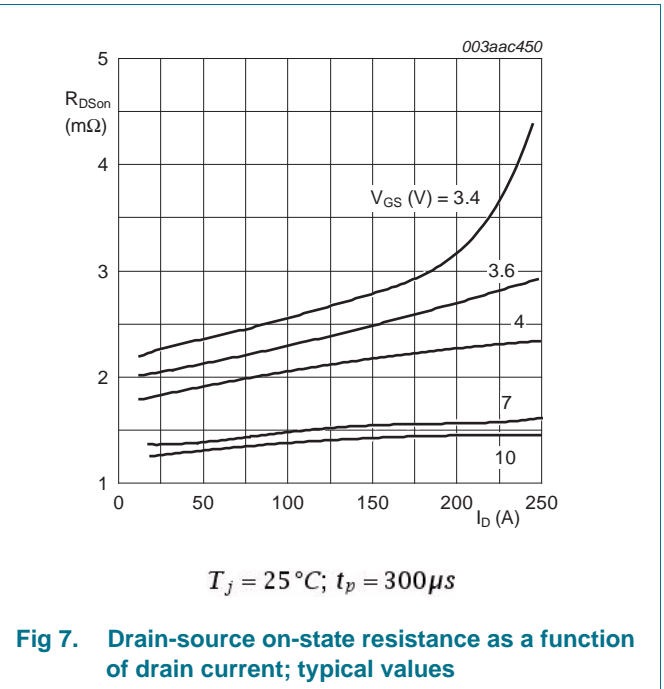
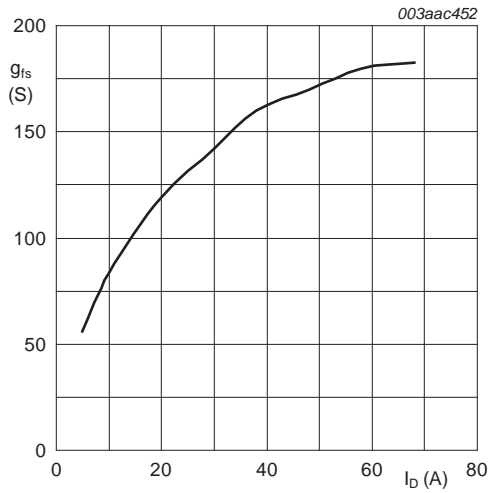
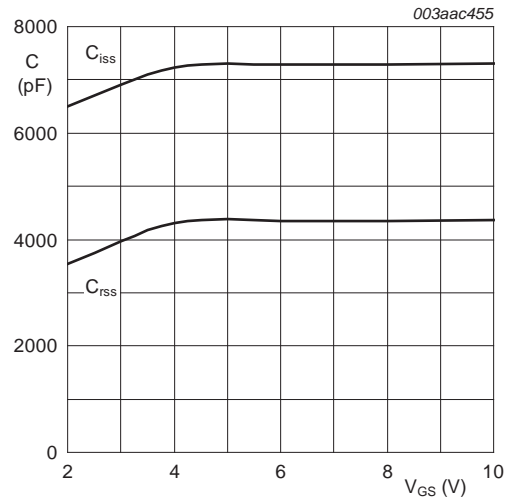


Fig 7. Drain-source on-state resistance as a function of drain current; typical values



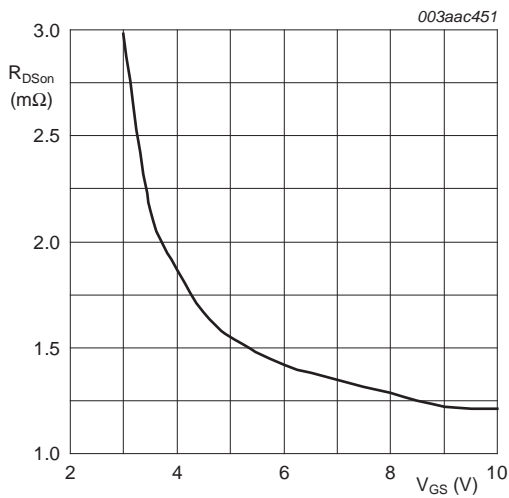
$T_j = 25\text{ }^\circ\text{C}; V_{DS} = 15\text{ V}$

Fig 8. Forward transconductance as a function of drain current; typical values



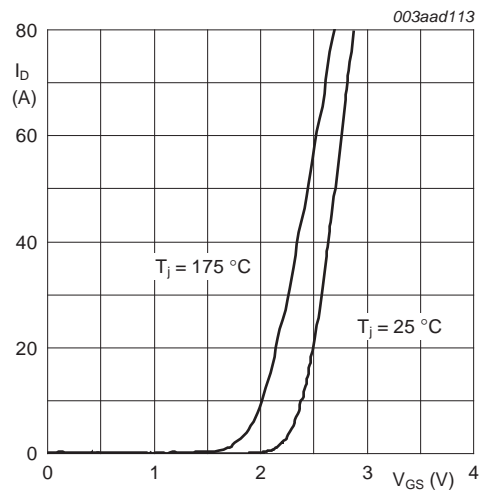
$V_{DS} = 0\text{ V}; f = 1\text{ MHz}$

Fig 9. Input and reverse transfer capacitances as a function of gate-source voltage; typical values



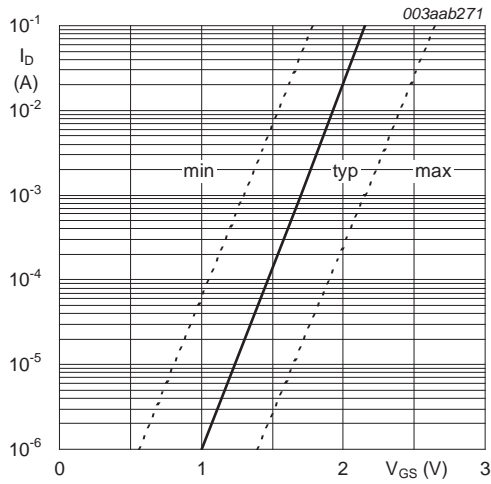
$T_j = 25\text{ }^\circ\text{C}; I_D = 15\text{ A}$

Fig 10. Drain-source on-state resistance as a function of gate-source voltage; typical values



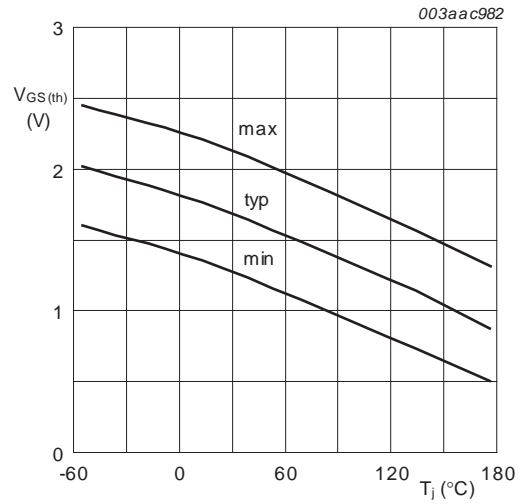
$V_{DS} = 15\text{ V}$

Fig 11. Transfer characteristics: drain current as a function of gate-source voltage; typical values



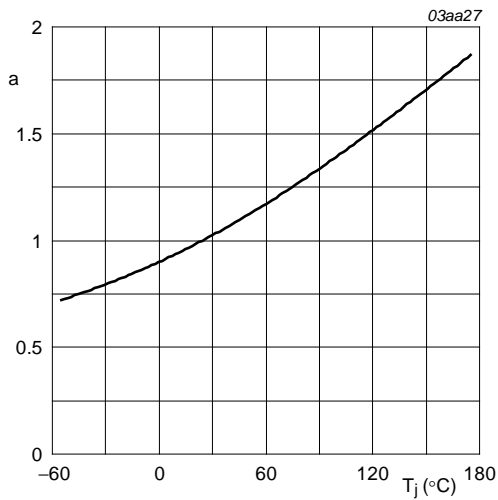
$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$

Fig 12. Sub-threshold drain current as a function of gate-source voltage



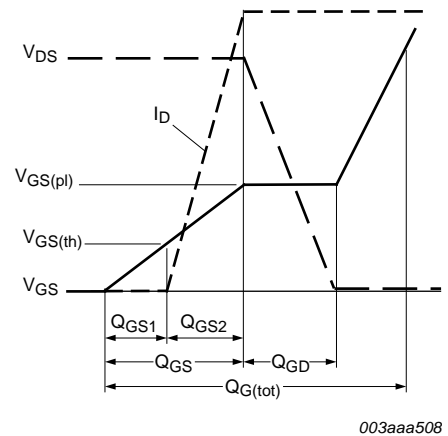
$I_D = 1\text{mA}; V_{DS} = V_{GS}$

Fig 13. Gate-source threshold voltage as a function of junction temperature



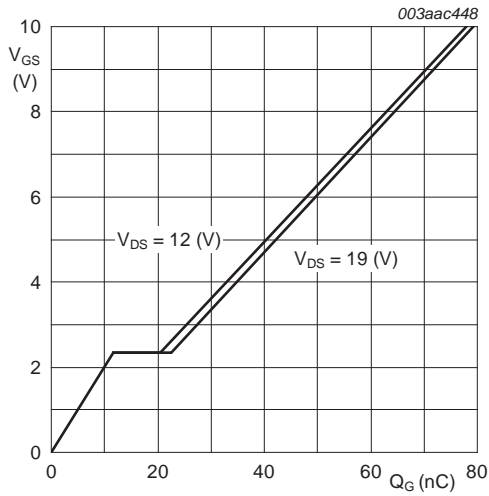
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 14. Normalized drain-source on-state resistance factor as a function of junction temperature



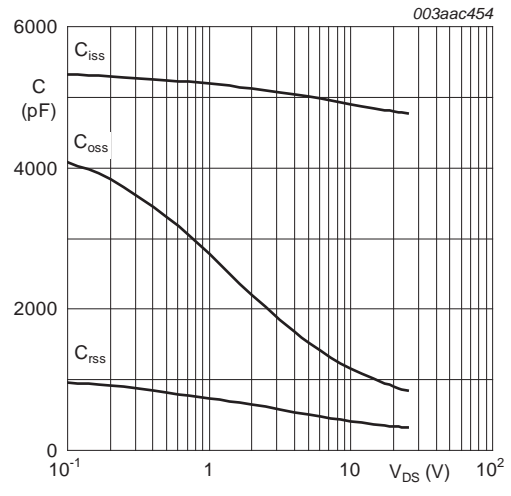
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Fig 15. Gate charge waveform definitions



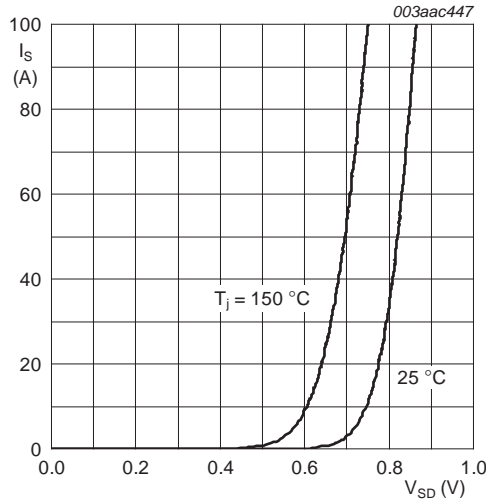
$T_j = 25^\circ\text{C}; I_D = 10\text{A}$

Fig 16. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0\text{V}; f = 1\text{MHz}$

Fig 17. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



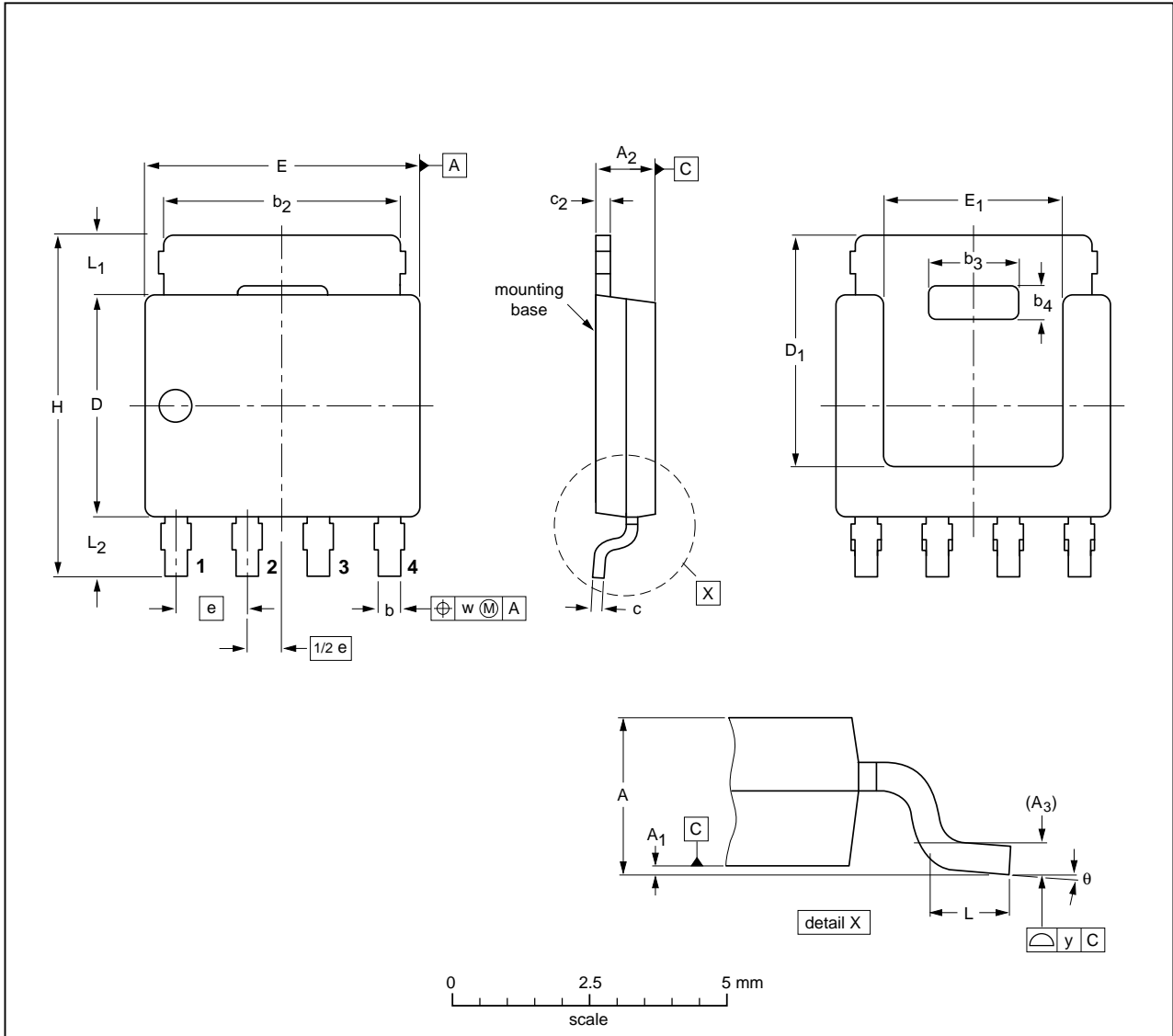
$V_{GS} = 0\text{V}$

Fig 18. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (LPAK); 4 leads

SOT669



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	A ₂	A ₃	b	b ₂	b ₃	b ₄	c	c ₂	D ⁽¹⁾	D ₁ ⁽¹⁾ _{max}	E ⁽¹⁾	E ₁ ⁽¹⁾	e	H	L	L ₁	L ₂	w	y	θ
mm	1.20 1.01	0.15 0.00	1.10 0.95	0.25	0.50 0.35	4.41 3.62	2.2 2.0	0.9 0.7	0.25 0.19	0.30 0.24	4.10 3.80	4.20	5.0 4.8	3.3 3.1	1.27	6.2 5.8	0.85 0.40	1.3 0.8	1.3 0.8	0.25	0.1	8° 0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT669		MO-235				04-10-13 06-03-16

Fig 19. Package outline SOT669 (LPAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN1R5-30YL_1	20100409	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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