

## PSMN3R3-80ES

# N-channel 80 V, 3.3 mΩ standard level MOSFET in I2PAK Rev. 1 — 31 October 2011 Product data

Product data sheet

#### **Product profile** 1.

## 1.1 General description

Standard level N-channel MOSFET in I2PAK package qualified to 175C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

#### 1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for standard level gate drive

## 1.3 Applications

- DC-to-DC converters
- Load switch

- Motor control
- Server power supplies

#### 1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
$V_{DS}$	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C		-	-	80	V
I <sub>D</sub>	drain current	$T_{mb} = 25  ^{\circ}\text{C};  V_{GS} = 10  \text{V};  \text{see}  \frac{\text{Figure 1}}{\text{Constant}}$	[1]	-	-	120	Α
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; see <u>Figure 2</u>		-	-	338	W
T <sub>j</sub>	junction temperature			-55	-	175	°C
Static char	racteristics						
R <sub>DSon</sub>	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 100 °C;$ see Figure 12		-	4.6	5.4	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ °C};$ see <u>Figure 13</u>	[2]	- 2.8	2.8	3.3	mΩ
Dynamic o	haracteristics						
$Q_{GD}$	gate-drain charge	$V_{GS} = 10 \text{ V}; I_D = 75 \text{ A}; V_{DS} = 40 \text{ V};$		-	27	-	nC
Q <sub>G(tot)</sub>	total gate charge	see Figure 14; see Figure 15		-	139	-	nC
Avalanche ruggedness							
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	$V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; $I_D$ = 120 A; $V_{sup}$ ≤ 80 V; $R_{GS}$ = 50 $\Omega$ ; unclamped		-	-	676	mJ

<sup>[1]</sup> Continuous current is limited by package.



<sup>[2]</sup> Measured 3 mm from package.

## 2. Pinning information

Table 2. Pinning information

	•			
Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		_
2	D	drain	mb	D
3	S	source		G (EA)
mb	D	drain		
				mbb076 S
			1 2 3	
			SOT226 (I2PAK)	

## 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN3R3-80ES	I2PAK	plastic single-ended package (I2PAK); TO-262	SOT226

## 4. Limiting values

Table 4. Limiting values

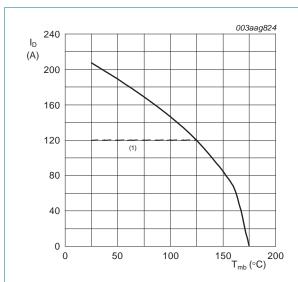
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DS}$	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C		-	80	V
$V_{DGR}$	drain-gate voltage	$T_j \ge 25 \text{ °C}; T_j \le 175 \text{ °C}; R_{GS} = 20 \text{ k}\Omega$		-	80	V
$V_{GS}$	gate-source voltage			-20	20	V
$I_D$	drain current	$V_{GS} = 10 \text{ V}; T_{mb} = 100 \text{ °C}; \text{ see } \frac{\text{Figure 1}}{}$	[1]	-	120	Α
		$V_{GS} = 10 \text{ V}; T_{mb} = 25 \text{ °C}; \text{ see } \underline{\text{Figure 1}}$	[1]	-	120	Α
$I_{DM}$	peak drain current	pulsed; $t_p \le 10 \mu s$ ; $T_{mb} = 25 \text{ °C}$ ; see Figure 3		-	830	Α
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; see <u>Figure 2</u>		-	338	W
T <sub>stg</sub>	storage temperature			-55	175	°C
T <sub>j</sub>	junction temperature			-55	175	°C
T <sub>sld(M)</sub>	peak soldering temperature			-	260	°C
Source-drain	n diode					
Is	source current	T <sub>mb</sub> = 25 °C	[1]	-	120	Α
I <sub>SM</sub>	peak source current	pulsed; $t_p \le 10 \mu s$ ; $T_{mb} = 25 \text{ °C}$		-	830	Α
Avalanche ru	uggedness					
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	$V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; $I_D$ = 120 A; $V_{sup}$ ≤ 80 V; $R_{GS}$ = 50 $\Omega$ ; unclamped		-	676	mJ

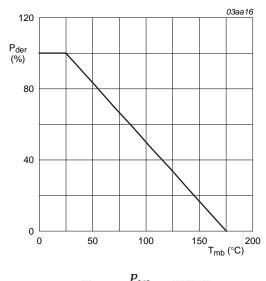
<sup>[1]</sup> Continuous current is limited by package.

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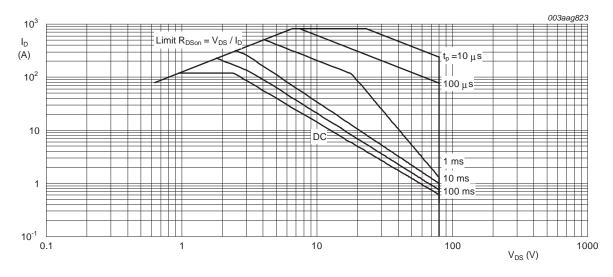
 $V_{GS} \ge 10 V$ ; (1) Capped at 120A due to package



 $P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$ 

Fig 1. Continuous drain current as a function of mounting base temperature

Fig 2. Normalized total power dissipation as a function of mounting base temperature



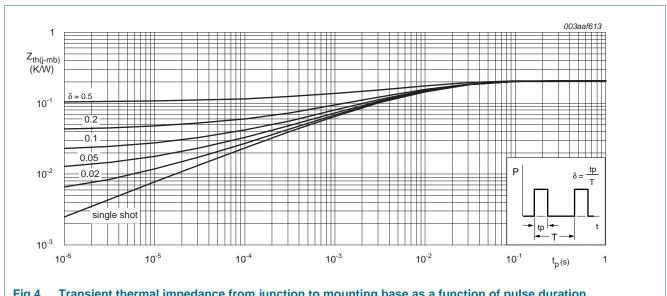
 $T_{mb} = 25$  °C;  $I_{DM}$  is a single pulse; Capped at 120 A due to package

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

## **Thermal characteristics**

Table 5. **Thermal characteristics** 

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	0.22	0.44	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Vertical in free air	-	60	-	K/W



Transient thermal impedance from junction to mounting base as a function of pulse duration

## 6. Characteristics

Table 6. Characteristics

Table 6.	Characteristics					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static cha	aracteristics					
V <sub>(BR)DSS</sub>	drain-source breakdown	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 °C$	73	-	-	V
	voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 °C$	80	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1$ mA; $V_{DS} = V_{GS}$ ; $T_j = 175$ °C; see Figure 10	1	-	-	V
		$I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$ ; $T_j$ = -55 °C; see <u>Figure 10</u>	-	-	4.6	V
		$I_D = 1$ mA; $V_{DS} = V_{GS}$ ; $T_j = 25$ °C; see <u>Figure 10</u> ; see <u>Figure 11</u>	2	3	4	V
I <sub>DSS</sub>	drain leakage current	$V_{DS} = 80 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	0.02	10	μΑ
		$V_{DS} = 80 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ °C}$	-	-	500	μΑ
I <sub>GSS</sub>	gate leakage current	$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	100	nΑ
		$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	100	nΑ
Doon	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 ^{\circ}\text{C};$ see Figure 12	-	6.7	7.9	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 100 \text{ °C};$ see Figure 12	-	4.6	5.4	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ °C};$ see Figure 13	[1] -	2.8	3.3	mΩ
R <sub>G</sub>	internal gate resistance (AC)	f = 1 MHz	-	0.9	-	Ω
Dynamic	characteristics					
Q <sub>G(tot)</sub>	total gate charge	$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$	-	135	-	nC
		$I_D = 75 \text{ A}; V_{DS} = 40 \text{ V}; V_{GS} = 10 \text{ V};$	-	139	-	nC
$Q_{GS}$	gate-source charge	see Figure 14; see Figure 15	-	51	-	nC
Q <sub>GS(th)</sub>	pre-threshold gate-source charge		-	30	-	nC
Q <sub>GS(th-pl)</sub>	post-threshold gate-source charge		-	21	-	nC
Q <sub>GD</sub>	gate-drain charge		-	27	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25 \text{ A}$ ; $V_{DS} = 40 \text{ V}$ ; see <u>Figure 14</u> ; see <u>Figure 15</u>	-	5.8	-	V
C <sub>iss</sub>	input capacitance	$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$	-	9961	-	pF
C <sub>oss</sub>	output capacitance	T <sub>j</sub> = 25 °C; see <u>Figure 16</u>	-	847	-	pF
C <sub>rss</sub>	reverse transfer capacitance		-	401	-	pF
t <sub>d(on)</sub>	turn-on delay time	$V_{DS} = 40 \text{ V}; R_L = 0.53 \Omega; V_{GS} = 10 \text{ V};$	-	41	-	ns
t <sub>r</sub>	rise time	$R_{G(ext)} = 10 \Omega; I_D = 75 A$	-	43	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	109	-	ns
t <sub>f</sub>	fall time		-	44	-	ns

**Product data sheet** 

Table 6. Characteristics ... continued

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Source-drain	n diode					
$V_{SD}$	source-drain voltage	$I_S = 25 \text{ A}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ °C}$ ; see Figure 17	-	0.8	1.2	V
t <sub>rr</sub>	reverse recovery time	$I_S = 25 \text{ A}$ ; $dI_S/dt = 100 \text{ A/}\mu\text{s}$ ;	-	63	-	ns
Q <sub>r</sub>	recovered charge	$V_{GS} = 0 \text{ V}; V_{DS} = 20 \text{ V}$	-	121	-	nC

#### [1] Measured 3 mm from package.

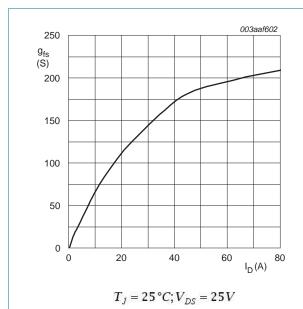


Fig 5. Forward transconductance as a function of drain current; typical values

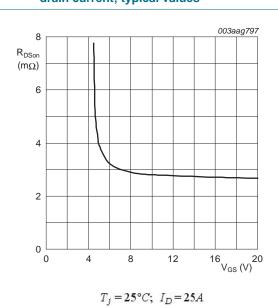
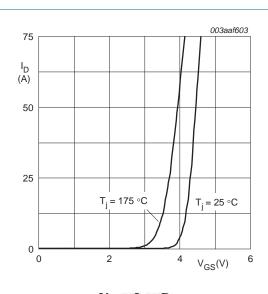
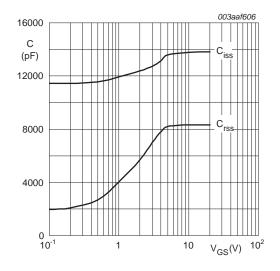


Fig 7. Drain-source on-state resistance as a function of gate-source voltage; typical values



 $V_{DS} > I_D \times R_{DSon}$ 

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values



 $V_{DS} = 0V; f = 1MHz$ 

Fig 8. Input and reverse transfer capacitances as a function of gate-source voltage; typical values

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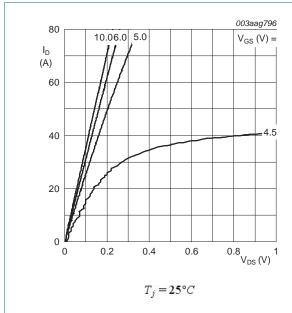


Fig 9. Output characteristics; drain current as a function of drain-source voltage; typical values

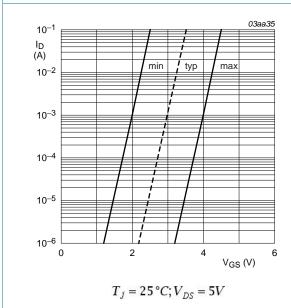
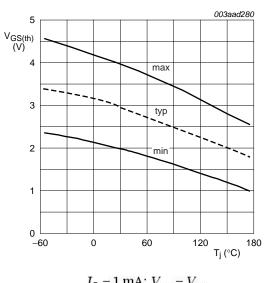


Fig 11. Sub-threshold drain current as a function of gate-source voltage



 $I_D = 1 \text{ mA}; \ V_{DS} = V_{GS}$ 

Fig 10. Gate-source threshold voltage as a function of junction temperature

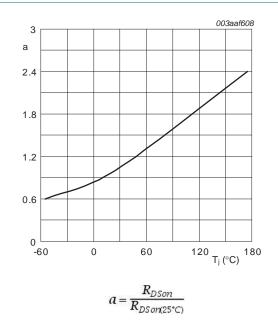


Fig 12. Normailzed drain-source on-state resistance factor as a function of junction temperature

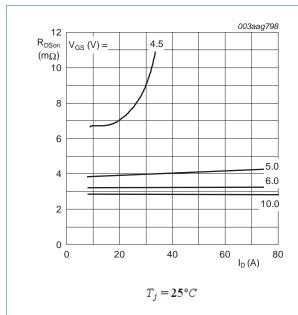
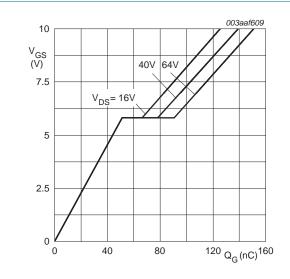
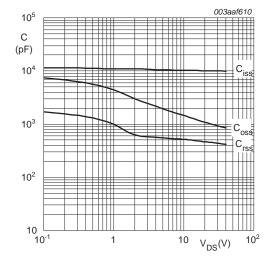


Fig 13. Drain-source on-state resistance as a function of drain current; typical values

Fig 14. Gate charge waveform definitions



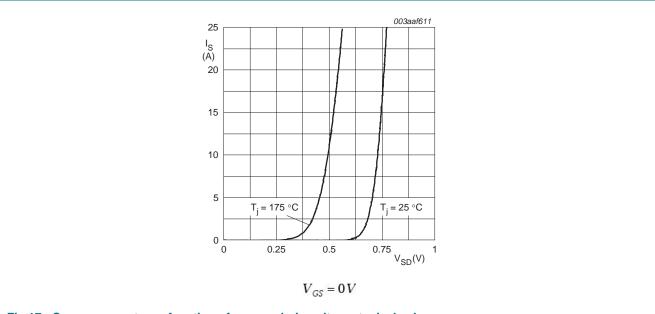


 $T_j = 25$  °C;  $I_D = 75$  A

Fig 16. Input, output and reverse transfer capacitances



 $V_{GS} = 0V; f = 1MHz$ 



## 7. Package outline

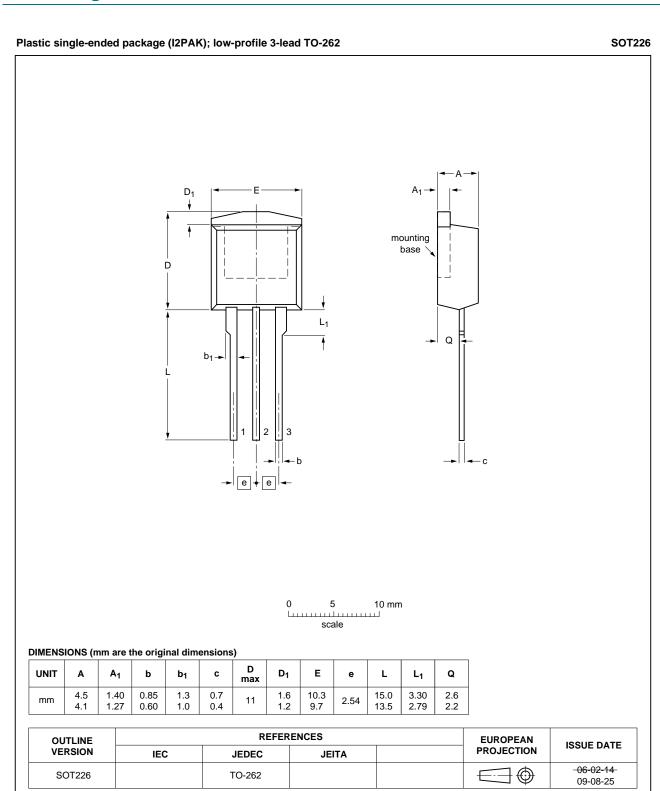


Fig 18. Package outline SOT226 (I2PAK)

## 8. Revision history

### Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN3R3-80ES v.1	20111031	Product data sheet	-	-

## 9. Legal information

#### 9.1 Data sheet status

Document status [1] [2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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# **PSMN3R3-80ES**

## **Nexperia**

N-channel 80 V, 3.3 m $\Omega$  standard level MOSFET in I2PAK

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