



# PSMN3R5-25MLD

N-channel 25 V, 3.72 mΩ logic level MOSFET in LFPAK33 using NextPowerS3 Technology

6 April 2016

Product data sheet

## 1. General description

Logic level gate drive N-channel enhancement mode MOSFET in LFPAK33 package. NextPowerS3 portfolio utilising Nexperia's unique "SchottkyPlus" technology delivers high efficiency, low spiking performance usually associated with MOSFETS with an integrated Schottky or Schottky-like diode but without problematic high leakage current. NextPowerS3 is particularly suited to high efficiency applications at high switching frequencies.

## 2. Features and benefits

- Ultra low  $Q_G$ ,  $Q_{GD}$  and  $Q_{OSS}$  for high system efficiency, especially at higher switching frequencies
- Superfast switching with soft-recovery; s-factor > 1
- Low spiking and ringing for low EMI designs
- Unique "SchottkyPlus" technology; Schottky-like performance with < 1  $\mu\text{A}$  leakage at 25 °C
- Optimised for 4.5 V gate drive
- Low parasitic inductance and resistance
- High reliability clip bonded and solder die attach Mini Power SO8 package; no glue, no wire bonds, qualified to 175 °C
- Exposed leads for optimal visual solder inspection

## 3. Applications

- On-board DC:DC solutions for server and telecommunications
- Secondary-side synchronous rectification in telecommunication applications
- Voltage regulator modules (VRM)
- Point-of-Load (POL) modules
- Power delivery for V-core, ASIC, DDR, GPU, VGA and system components
- Brushed and brushless motor control

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$		-	-	25	V
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 2</a>	[1]	-	-	70	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 1</a>		-	-	65	W

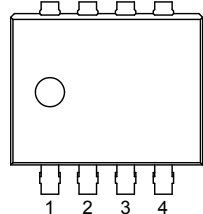
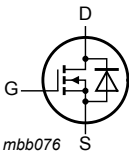
N-channel 25 V, 3.72 mΩ logic level MOSFET in LFAK33 using NextPowerS3 Technology

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T <sub>j</sub>	junction temperature		-55	-	175	°C
<b>Static characteristics</b>						
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 20 A; T <sub>j</sub> = 25 °C; <a href="#">Fig. 10</a>	-	4.46	5.41	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C; <a href="#">Fig. 10</a>	-	3.26	3.72	mΩ
<b>Dynamic characteristics</b>						
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 12 V; V <sub>GS</sub> = 10 V; <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>	-	18.9	-	nC
		I <sub>D</sub> = 25 A; V <sub>DS</sub> = 12 V; V <sub>GS</sub> = 4.5 V; <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>	-	8.7	-	nC
		I <sub>D</sub> = 0 A; V <sub>DS</sub> = 0 V; V <sub>GS</sub> = 10 V	-	10.7	-	nC
Q <sub>GD</sub>	gate-drain charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 12 V; V <sub>GS</sub> = 4.5 V; <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>	-	2.1	-	nC
<b>Source-drain diode</b>						
S	softness factor	I <sub>S</sub> = 25 A; di/dt = -100 A/μs; V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 12 V; <a href="#">Fig. 16</a>	-	1.1	-	

[1] Continuous current is limited by package

### 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>LFAK33 (SOT1210)</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

### 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN3R5-25MLD	LFAK33	Plastic single ended surface mounted package (LFAK33); 8 leads	SOT1210

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN3R5-25MLD	3D525L

## 8. Limiting values

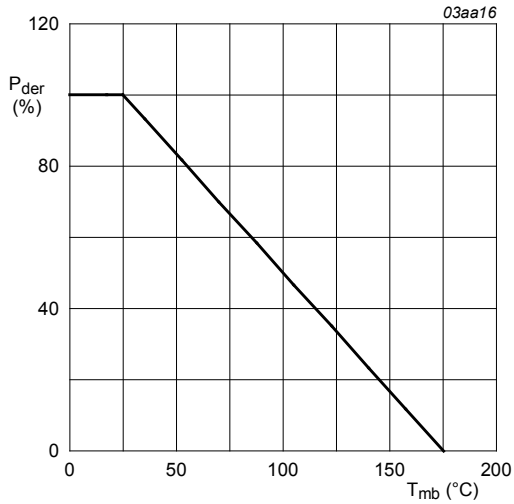
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$		-	25	V
$V_{DGR}$	drain-gate voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$		-	25	V
$V_{GS}$	gate-source voltage			-20	20	V
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 1</a>		-	65	W
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 2</a>	[1]	-	70	A
		$V_{GS} = 10\text{ V}$ ; $T_{mb} = 100\text{ °C}$ ; <a href="#">Fig. 2</a>		-	70	A
$I_{DM}$	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 3</a>		-	405	A
$T_{stg}$	storage temperature			-55	175	°C
$T_j$	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
$V_{ESD}$	electrostatic discharge voltage	HBM (JEDEC)		400	-	V
<b>Source-drain diode</b>						
$I_S$	source current	$T_{mb} = 25\text{ °C}$		-	54	A
$I_{SM}$	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$		-	405	A
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 25\text{ A}$ ; $V_{sup} \leq 25\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; $V_{GS} = 10\text{ V}$ ; $T_{j(init)} = 25\text{ °C}$ ; unclamped; $t_p = 262\text{ }\mu\text{s}$	[2]	-	106.6	mJ

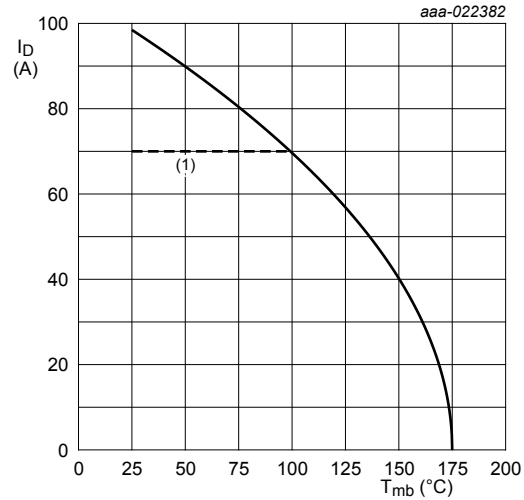
[1] Continuous current is limited by package

[2] Protected by 100% test



**Fig. 1. Normalized total power dissipation as a function of mounting base temperature**

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

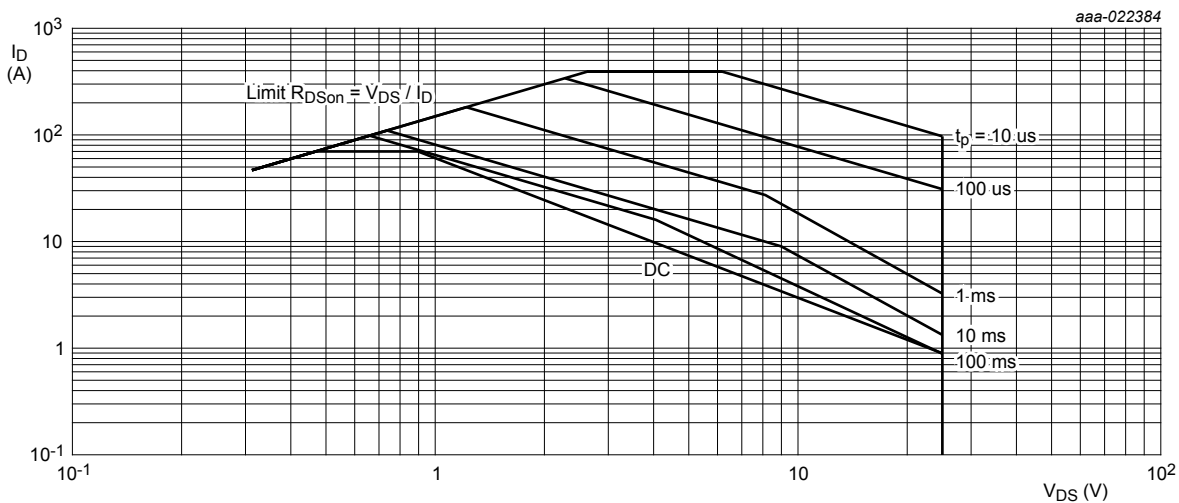


$V_{GS} \geq 10\text{ V}$

(1) Capped at 70A due to package

**Fig. 2. Continuous drain current as a function of mounting base temperature**

$$I_D = 98\text{ A} \times \sqrt{\frac{175^{\circ}\text{C} - T_{mb}}{150^{\circ}\text{C}}} \text{ for } T_{mb} \geq 25^{\circ}\text{C}$$



$T_{mb} = 25^{\circ}\text{C}$ ;  $I_{DM}$  is a single pulse

**Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**

## 9. Thermal characteristics

**Table 6. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4	-	2.08	2.31	K/W

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	<a href="#">Fig. 5</a>	-	57	-	K/W
		<a href="#">Fig. 6</a>	-	178	-	K/W

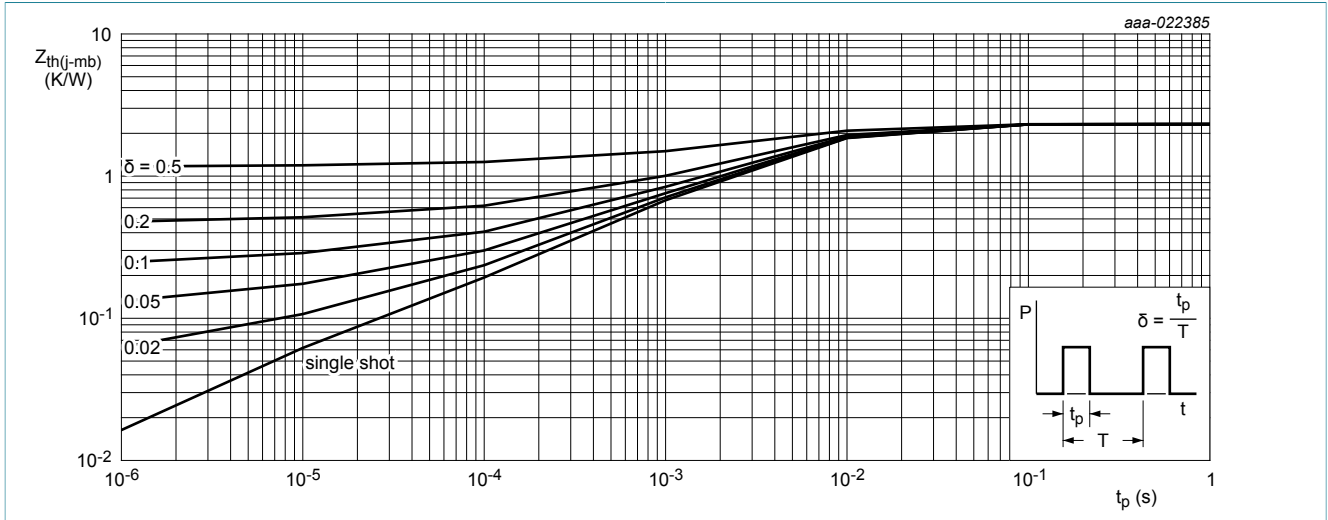


Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

aaa-008476

aaa-008477

**Fig. 5. PCB layout for thermal resistance junction to ambient 1" square pad; FR4 Board; 2oz copper**

**Fig. 6. PCB layout for thermal resistance junction to ambient minimum footprint; FR4 Board; 2oz copper**

## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	25	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	22.5	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$	1.2	1.73	2.2	V

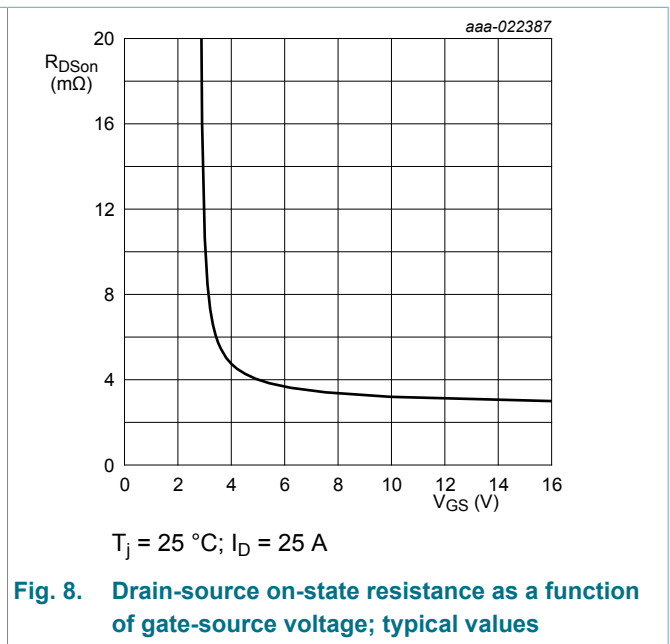
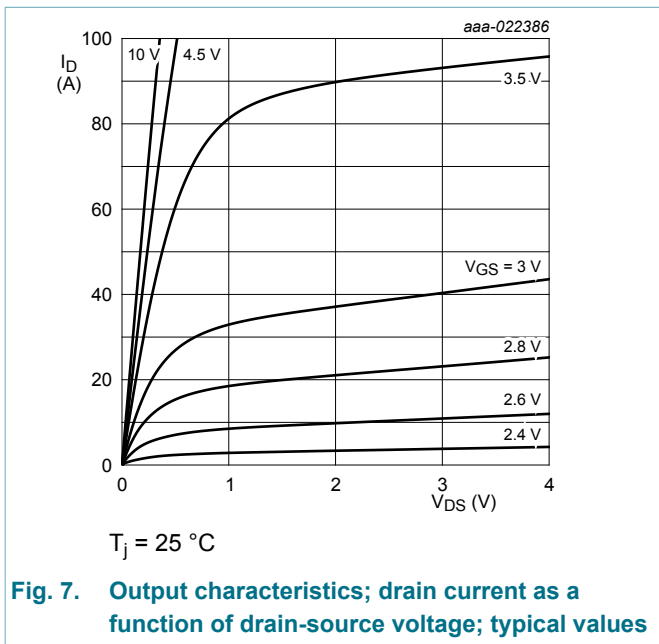
## N-channel 25 V, 3.72 mΩ logic level MOSFET in LPAK33 using NextPowerS3 Technology

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25\text{ }^{\circ}\text{C} \leq T_j \leq 175\text{ }^{\circ}\text{C}$	-	-4.3	-	mV/K
$I_{DSS}$	drain leakage current	$V_{DS} = 20\text{ V}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^{\circ}\text{C}$	-	-	1	$\mu\text{A}$
		$V_{GS} = 20\text{ V}; T_j = 125\text{ }^{\circ}\text{C}$	-	2.66	-	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = 20\text{ V}; V_{DS} = 0\text{ V}; T_j = 25\text{ }^{\circ}\text{C}$	-	-	100	nA
		$V_{GS} = -20\text{ V}; V_{DS} = 0\text{ V}; T_j = 25\text{ }^{\circ}\text{C}$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}; I_D = 20\text{ A}; T_j = 25\text{ }^{\circ}\text{C};$ <a href="#">Fig. 10</a>	-	4.46	5.41	mΩ
		$V_{GS} = 4.5\text{ V}; I_D = 20\text{ A}; T_j = 175\text{ }^{\circ}\text{C};$ <a href="#">Fig. 11; Fig. 10</a>	-	-	9.2	mΩ
		$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ }^{\circ}\text{C};$ <a href="#">Fig. 10</a>	-	3.26	3.72	mΩ
		$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 175\text{ }^{\circ}\text{C};$ <a href="#">Fig. 11; Fig. 10</a>	-	-	6.4	mΩ
$R_G$	gate resistance	$f = 1\text{ MHz}$	-	0.73	-	Ω
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 25\text{ A}; V_{DS} = 12\text{ V}; V_{GS} = 10\text{ V};$ <a href="#">Fig. 12; Fig. 13</a>	-	18.9	-	nC
		$I_D = 25\text{ A}; V_{DS} = 12\text{ V}; V_{GS} = 4.5\text{ V};$ <a href="#">Fig. 12; Fig. 13</a>	-	8.7	-	nC
		$I_D = 0\text{ A}; V_{DS} = 0\text{ V}; V_{GS} = 10\text{ V}$	-	10.7	-	nC
$Q_{GS}$	gate-source charge	$I_D = 25\text{ A}; V_{DS} = 12\text{ V}; V_{GS} = 4.5\text{ V};$ <a href="#">Fig. 12; Fig. 13</a>	-	3.9	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	2.1	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	1.8	-	nC
$Q_{GD}$	gate-drain charge		-	2.1	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25\text{ A}; V_{DS} = 12\text{ V};$ <a href="#">Fig. 12; Fig. 13</a>	-	3	-	V
$C_{iss}$	input capacitance	$V_{DS} = 12\text{ V}; V_{GS} = 0\text{ V}; f = 1\text{ MHz};$ $T_j = 25\text{ }^{\circ}\text{C};$ <a href="#">Fig. 14</a>	-	1334	-	pF
$C_{oss}$	output capacitance		-	863	-	pF
$C_{rss}$	reverse transfer capacitance		-	89	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 12\text{ V}; R_L = 0.6\text{ }^{\Omega}; V_{GS} = 4.5\text{ V};$ $R_{G(ext)} = 5\text{ }^{\Omega}$	-	10.8	-	ns
$t_r$	rise time		-	12.9	-	ns
$t_{d(off)}$	turn-off delay time		-	11.7	-	ns
$t_f$	fall time		-	7	-	ns

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$Q_{oss}$	output charge	$V_{GS} = 0\text{ V}; V_{DS} = 12\text{ V}; f = 1\text{ MHz}; T_j = 25\text{ °C}$	-	13.9	-	nC
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ °C}; \text{Fig. 15}$	-	0.82	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 25\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V}; V_{DS} = 12\text{ V}; \text{Fig. 16}$	-	24.4	-	ns
$Q_r$	recovered charge		[1]	13.5	-	nC
$t_a$	reverse recovery rise time		-	11.8	-	ns
$t_b$	reverse recovery fall time		-	12.7	-	ns
S	softness factor		-	1.1	-	

[1] includes capacitive recovery



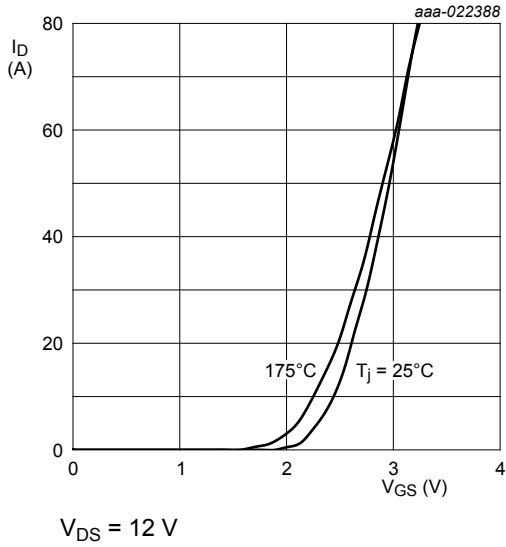


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

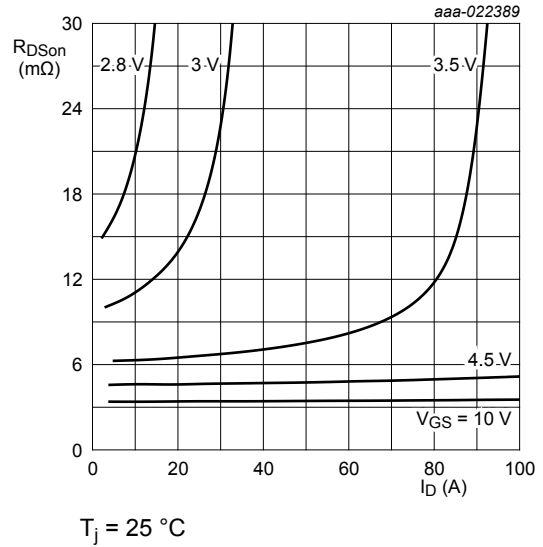


Fig. 10. Drain-source on-state resistance as a function of drain current; typical values

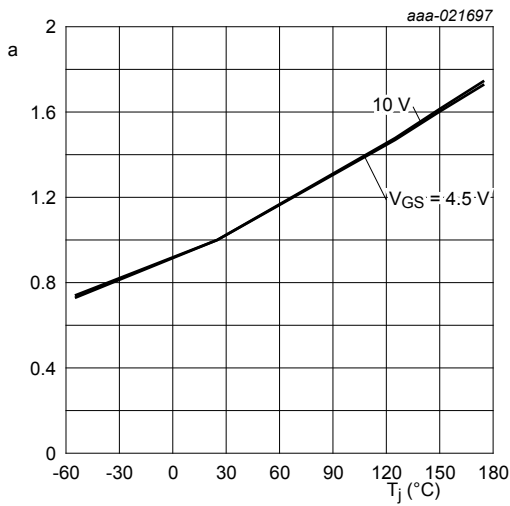


Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

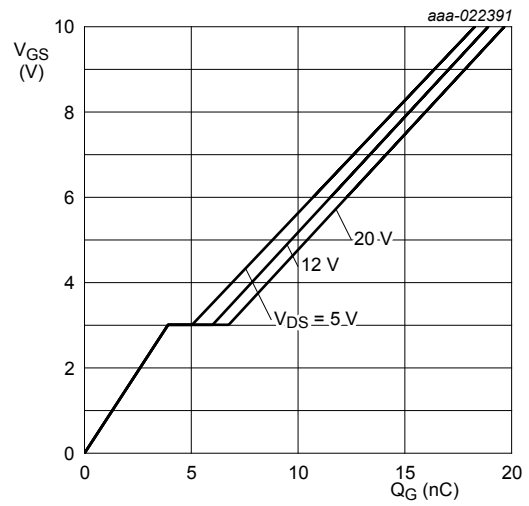


Fig. 12. Gate-source voltage as a function of gate charge; typical values



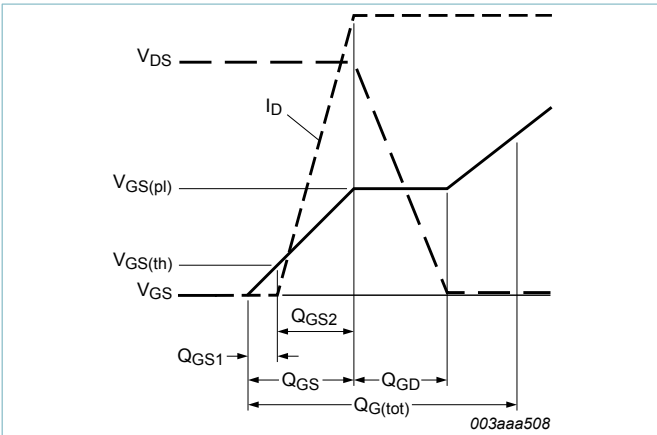
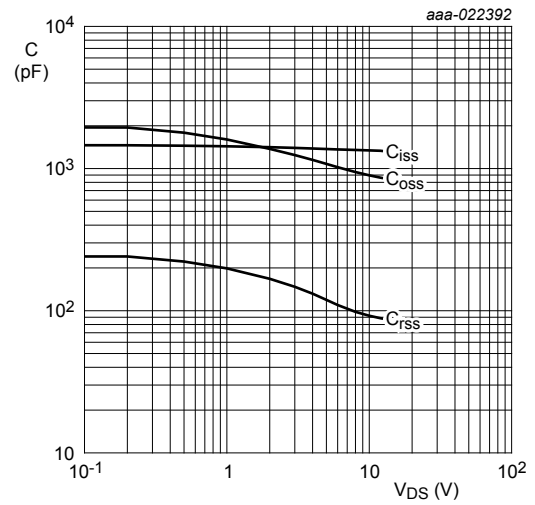
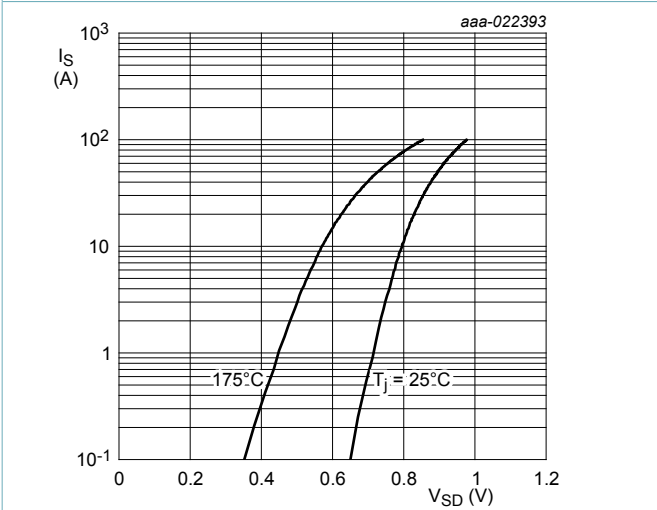


Fig. 13. Gate charge waveform definitions



$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0 \text{ V}$

Fig. 15. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

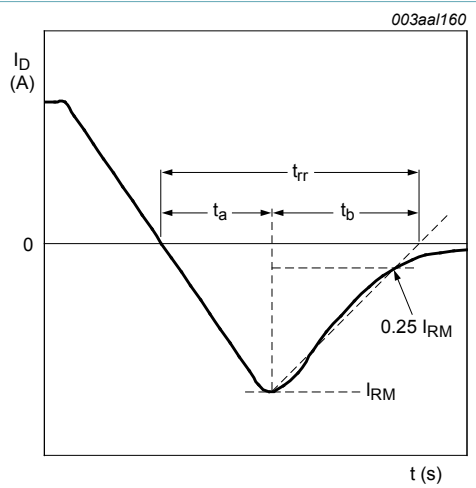


Fig. 16. Reverse recovery timing definition

### 11. Package outline

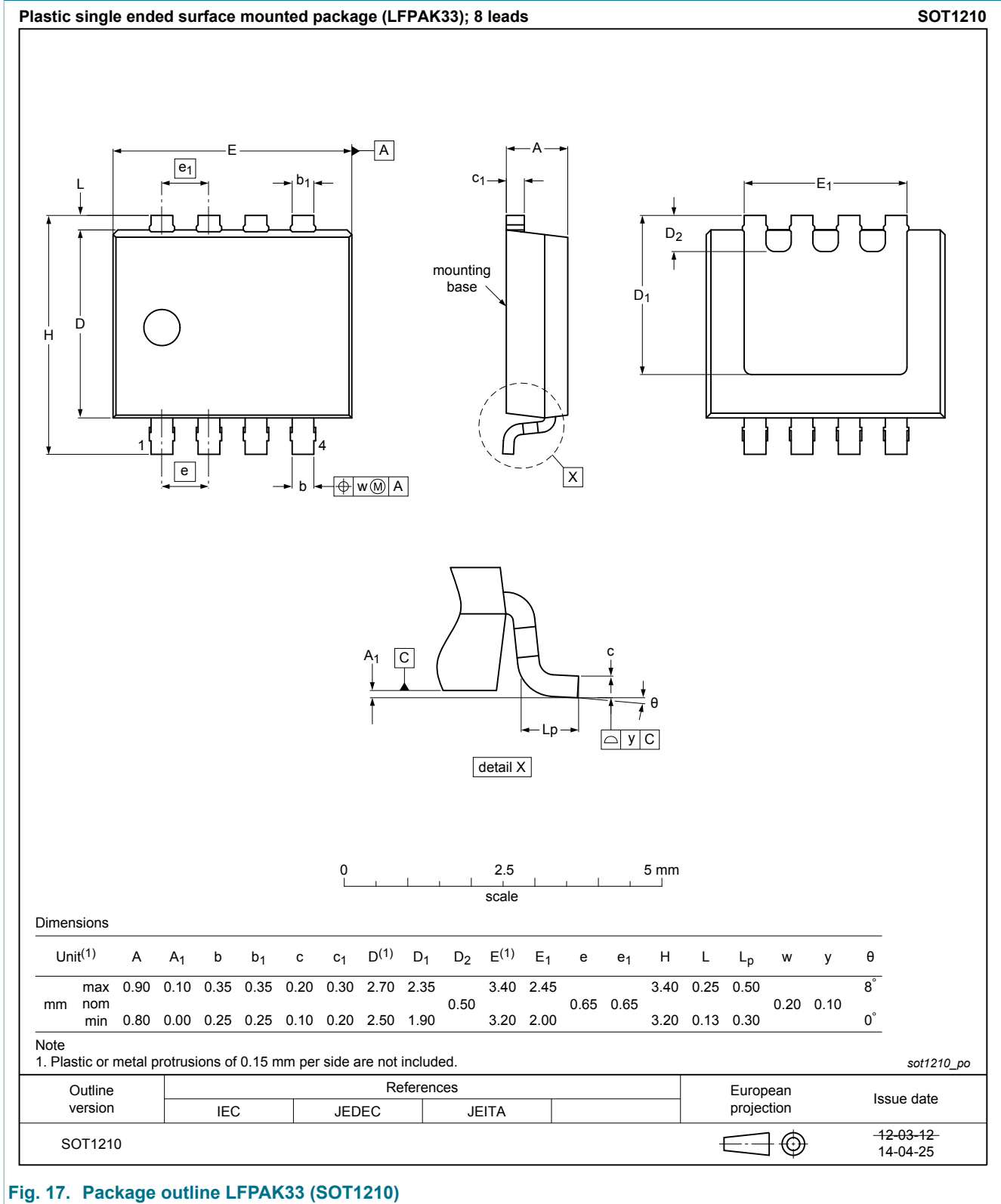


Fig. 17. Package outline LPAK33 (SOT1210)

## 12. Legal information

### 12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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## 13. Contents

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