



# PSMN4R4-80BS

N-channel 80 V, 4.5 mΩ standard level MOSFET in D2PAK

Rev. 1 — 22 March 2012

Product data sheet

## 1. Product profile

### 1.1 General description

Standard level N-channel MOSFET in SOT404 package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

### 1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for standard level gate drive sources

### 1.3 Applications

- DC - DC converters
- Motor control
- Load switching
- Server power supplies

### 1.4 Quick reference data

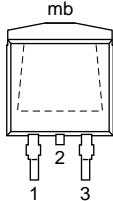
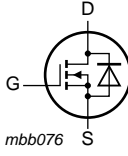
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	-	80	V
$I_D$	drain current	$T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V};$ see <a href="#">Figure 1</a>	[1]	-	100	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C};$ see <a href="#">Figure 2</a>	-	-	306	W
$T_j$	junction temperature		-55	-	175	°C
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 100\text{ °C};$ see <a href="#">Figure 13</a> ; see <a href="#">Figure 6</a>	-	6.27	7.4	mΩ
		$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C};$ see <a href="#">Figure 6</a>	-	3.8	4.5	mΩ
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; V_{DS} = 40\text{ V};$ see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>	-	25	-	nC
$Q_{G(tot)}$	total gate charge		-	125	-	nC
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}; T_{j(init)} = 25\text{ °C};$ $I_D = 100\text{ A}; V_{sup} \leq 80\text{ V};$ $R_{GS} = 50\text{ Ω};$ unclamped	-	-	591	mJ

[1] Continuous current is limited by package

## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain <sup>[1]</sup>		
3	S	source		
mb	D	drain		

**SOT404 (D2PAK)**

[1] It is not possible to make connection to pin 2

## 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN4R4-80BS	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

## 4. Marking

Table 4. Marking codes

Type number	Marking code
PSMN4R4-80BS	PSMN4R4-80BS

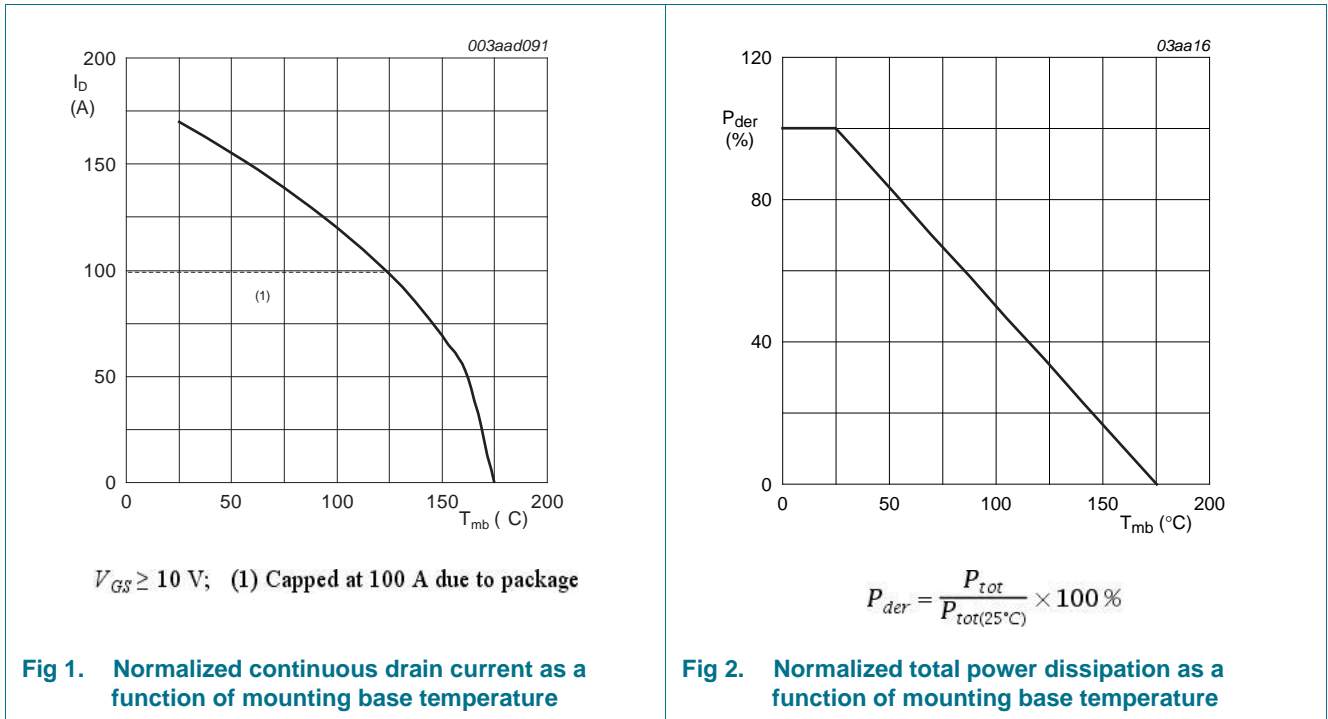
5. Limiting values

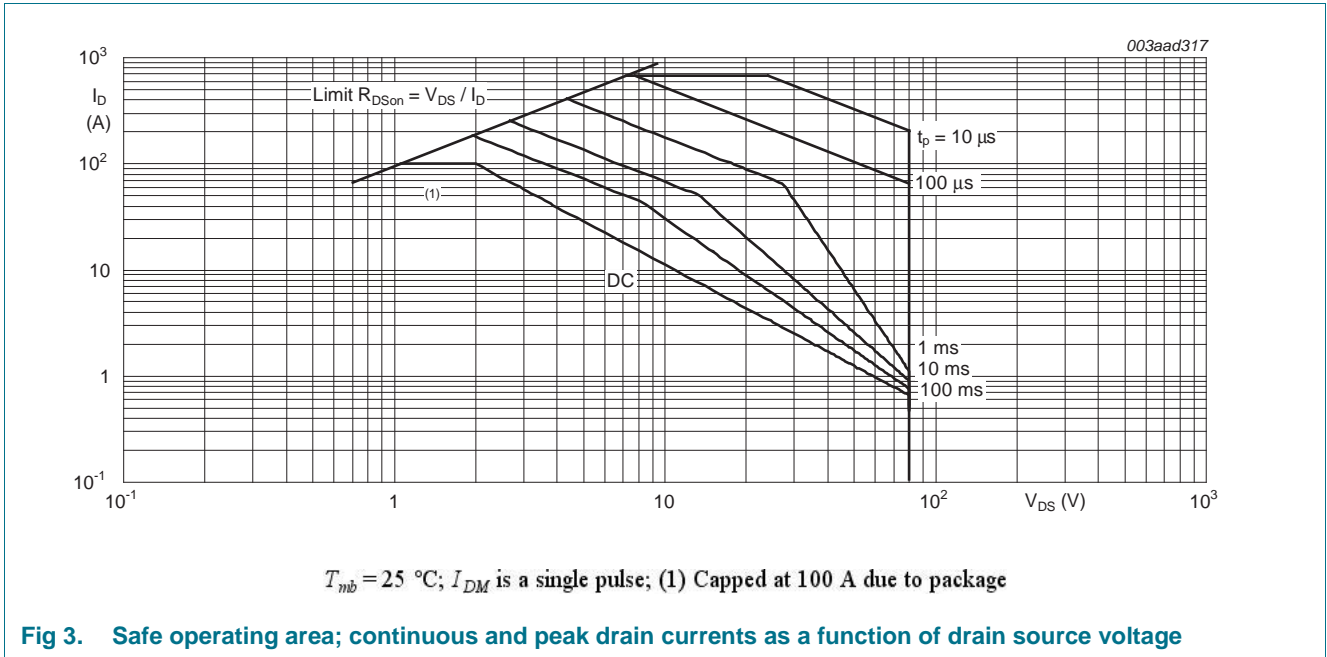
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C	-	80	V
V <sub>DGR</sub>	drain-gate voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C; R <sub>GS</sub> = 20 kΩ	-	80	V
V <sub>GS</sub>	gate-source voltage		-20	20	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 100 °C; see Figure 1 [1]	-	100	A
		V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 25 °C; see Figure 1 [1]	-	100	A
I <sub>DM</sub>	peak drain current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C; see Figure 3	-	680	A
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; see Figure 2	-	306	W
T <sub>stg</sub>	storage temperature		-55	175	°C
T <sub>j</sub>	junction temperature		-55	175	°C
T <sub>sld(M)</sub>	peak soldering temperature		-	260	°C
<b>Source-drain diode</b>					
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C	[1]	100	A
I <sub>SM</sub>	peak source current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C	-	680	A
<b>Avalanche ruggedness</b>					
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; I <sub>D</sub> = 100 A; V <sub>sup</sub> ≤ 80 V; R <sub>GS</sub> = 50 Ω; unclamped	-	591	mJ

[1] Continuous current is limited by package

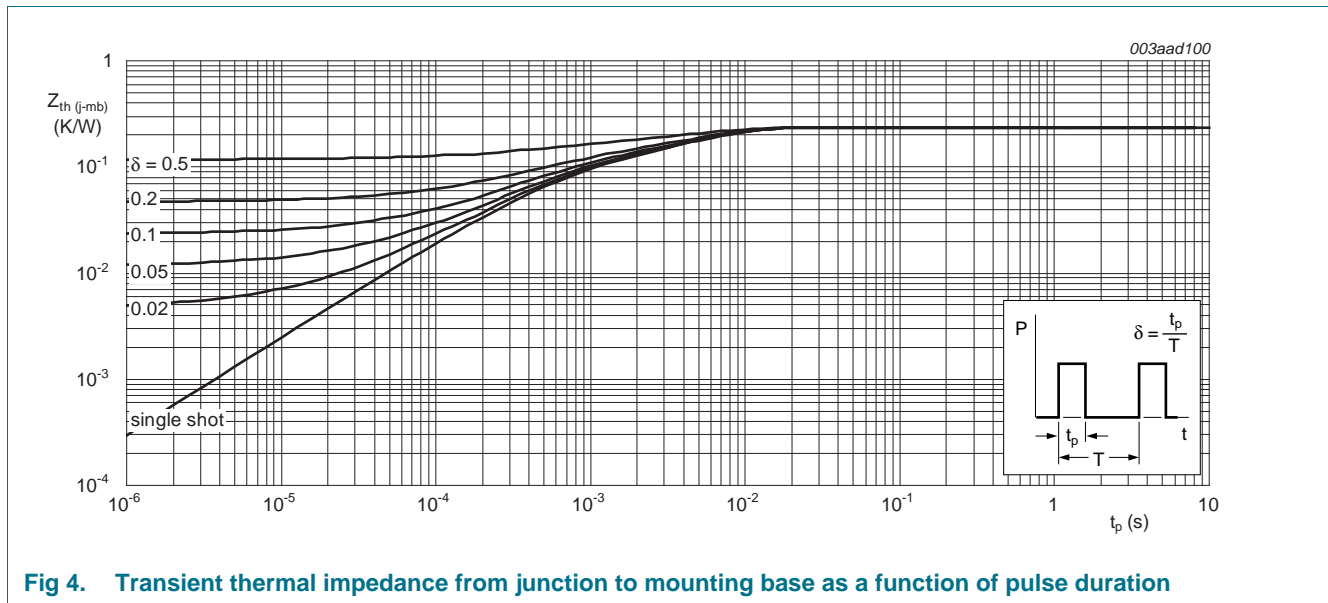




## 6. Thermal characteristics

**Table 6. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 4</a>	-	0.23	0.49	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Minimum footprint; mounted on a printed circuit board	-	50	-	K/W



**Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration**

## 7. Characteristics

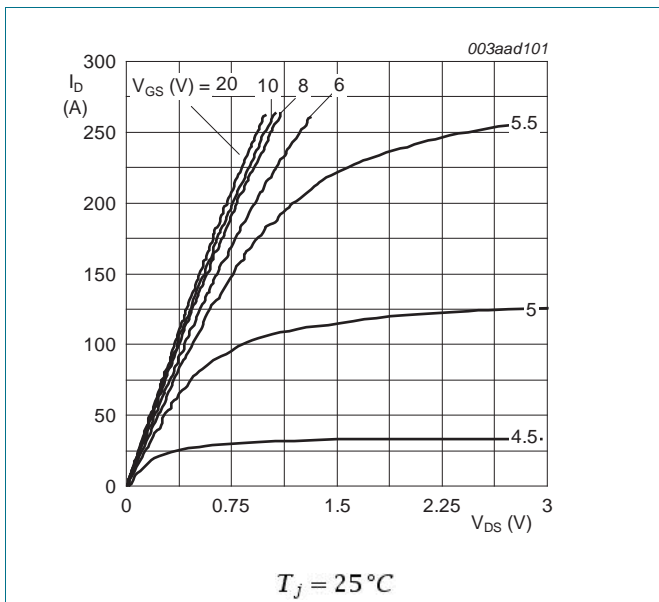
**Table 7. Characteristics**

Tested to JEDEC standards where applicable.

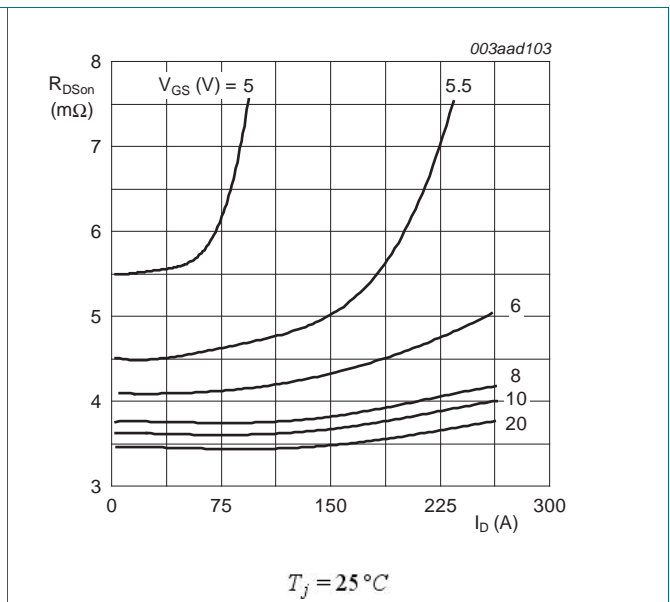
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	73	-	-	V
		$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	80	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ\text{C};$ see <a href="#">Figure 11</a>	1	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ see <a href="#">Figure 11</a>	-	-	4.6	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 11</a> ; see <a href="#">Figure 12</a>	2	3	4	V
$I_{DSS}$	drain leakage current	$V_{DS} = 80 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.02	10	$\mu\text{A}$
		$V_{DS} = 80 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ\text{C}$	-	-	200	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	10	100	nA
		$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ\text{C};$ see <a href="#">Figure 13</a> ; see <a href="#">Figure 6</a>	-	9.12	10.7	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 100 \text{ }^\circ\text{C};$ see <a href="#">Figure 13</a> ; see <a href="#">Figure 6</a>	-	6.27	7.4	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 6</a>	-	3.8	4.5	mΩ
$R_G$	internal gate resistance (AC)	$f = 1 \text{ MHz}$	-	1	-	Ω
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$	-	112	-	nC
		$I_D = 25 \text{ A}; V_{DS} = 40 \text{ V}; V_{GS} = 10 \text{ V};$ see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>	-	125	-	nC
$Q_{GS}$	gate-source charge		-	39	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	24	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	15	-	nC
$Q_{GD}$	gate-drain charge		-	25	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25 \text{ A}; V_{DS} = 40 \text{ V};$ see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>	-	4.65	-	V
$C_{iss}$	input capacitance	$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 16</a>	-	8400	-	pF
$C_{oss}$	output capacitance		-	700	-	pF
$C_{rss}$	reverse transfer capacitance		-	336	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 40 \text{ V}; R_L = 0.5 \text{ } \Omega; V_{GS} = 10 \text{ V};$ $R_{G(ext)} = 1.5 \text{ } \Omega$	-	34.7	-	ns
$t_r$	rise time		-	38.1	-	ns
$t_{d(off)}$	turn-off delay time		-	66	-	ns
$t_f$	fall time		-	18.4	-	ns

**Table 7. Characteristics ...continued**  
Tested to JEDEC standards where applicable.

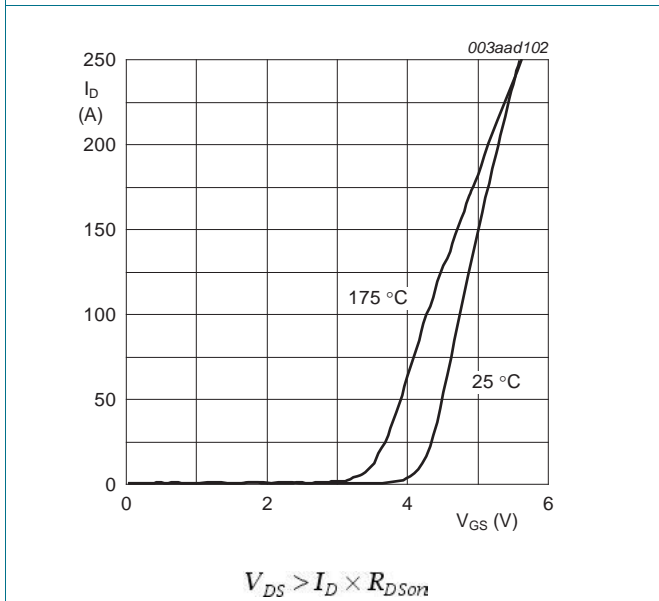
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25\text{ A}$ ; $V_{GS} = 0\text{ V}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 17</a>	-	0.8	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 25\text{ A}$ ; $dI_S/dt = 100\text{ A}/\mu\text{s}$ ; $V_{GS} = 0\text{ V}$ ; $V_{DS} = 20\text{ V}$	-	59	-	ns
$Q_r$	recovered charge		-	130	-	nC



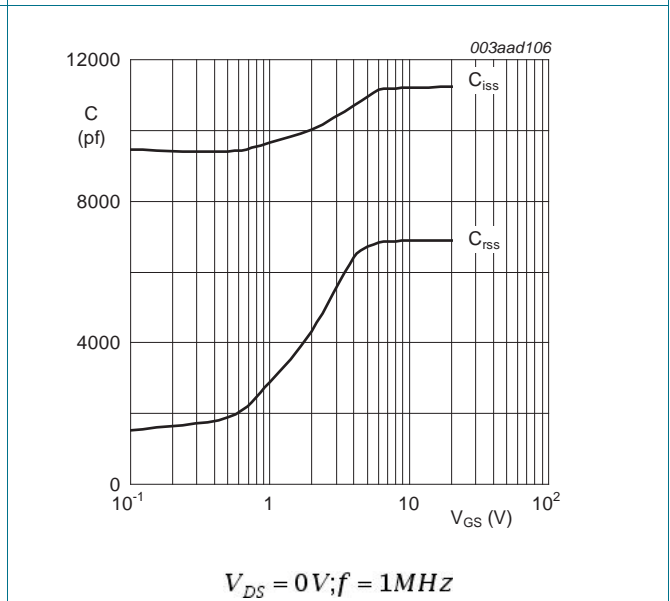
**Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values**



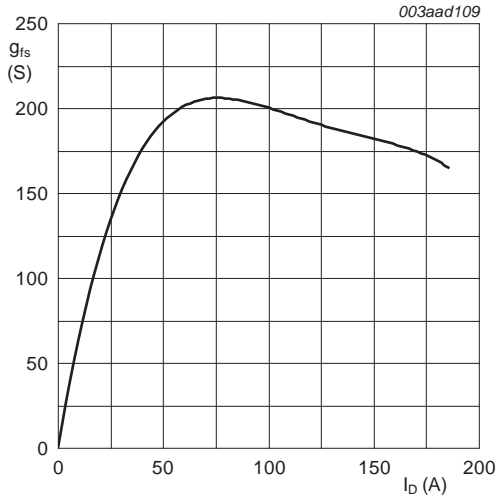
**Fig 6. Drain-source on-state resistance as a function of drain current; typical values**



**Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values**

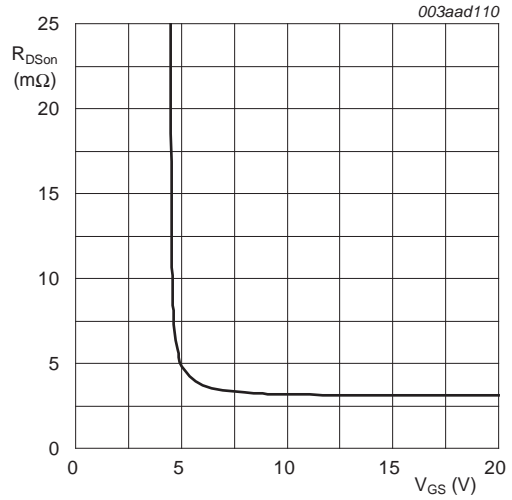


**Fig 8. Input and reverse transfer capacitances as a function of gate-source voltage; typical values**



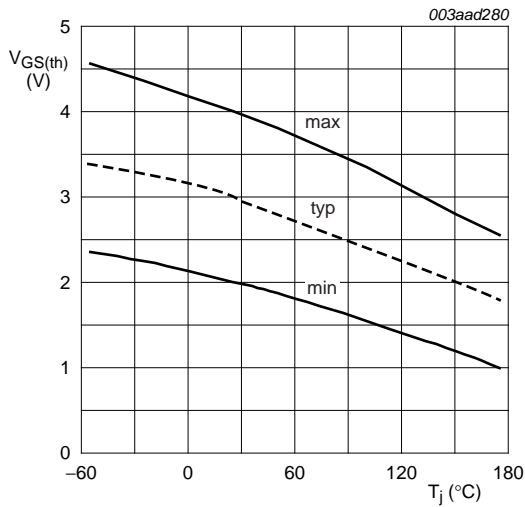
$T_j = 25\text{ }^\circ\text{C}; V_{DS} = 25\text{ V}$

Fig 9. Forward transconductance as a function of drain current; typical values



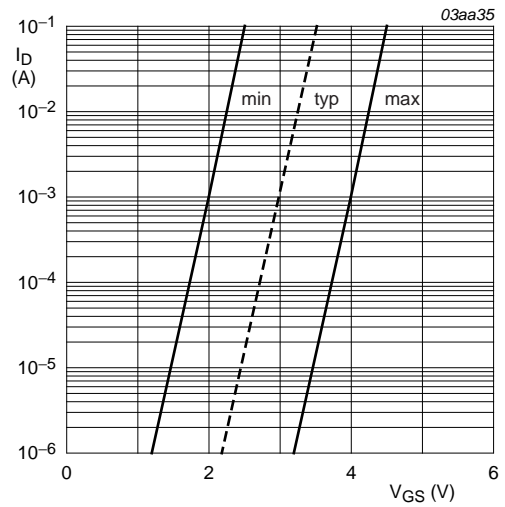
$T_j = 25\text{ }^\circ\text{C}; I_D = 15\text{ A}$

Fig 10. Drain-source on-state resistance as a function of gate-source voltage; typical values



$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

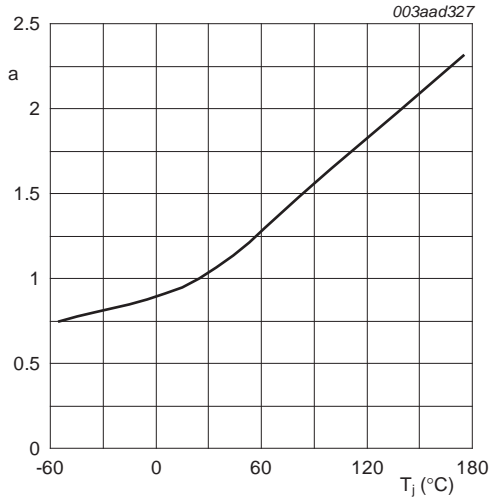
Fig 11. Gate-source threshold voltage as a function of junction temperature



$T_j = 25\text{ }^\circ\text{C}; V_{DS} = 5\text{ V}$

Fig 12. Sub-threshold drain current as a function of gate-source voltage





$$a = \frac{R_{DS(on)}}{R_{DS(on)25^{\circ}\text{C}}}$$

Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature

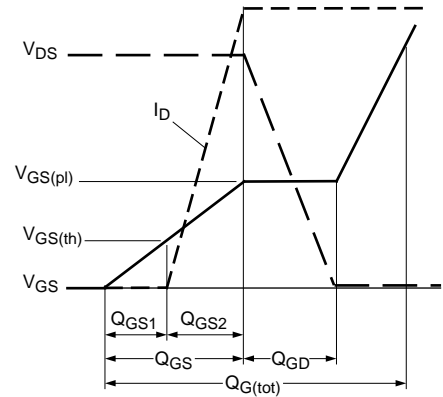
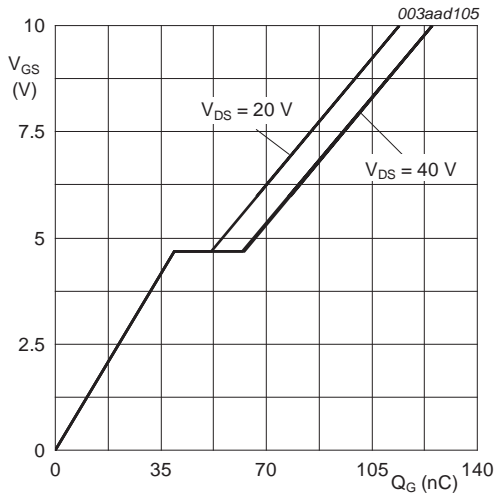
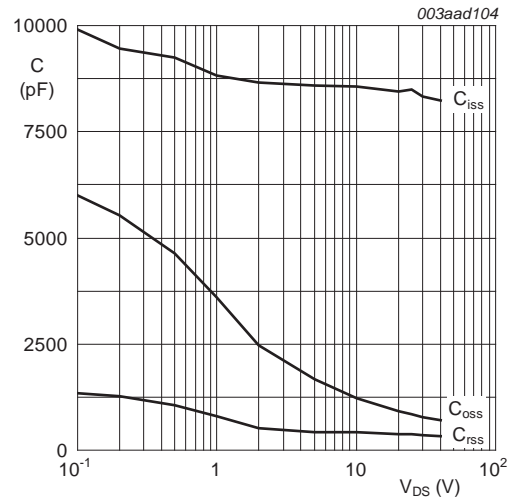


Fig 14. Gate charge waveform definitions



$T_j = 25^{\circ}\text{C}; I_D = 25\text{ A}$

Fig 15. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

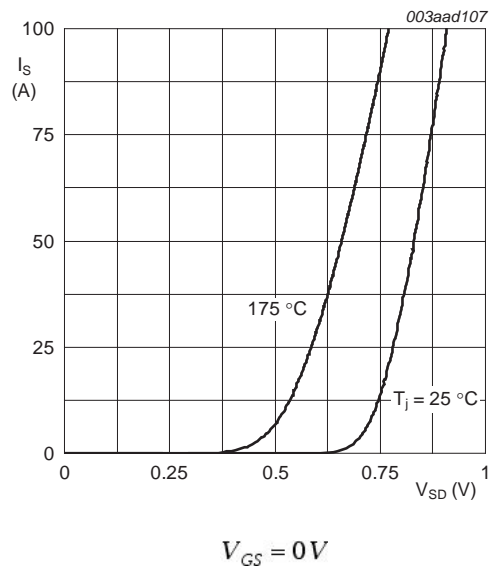


Fig 17. Source current as a function of source-drain voltage; typical values

8. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

SOT404

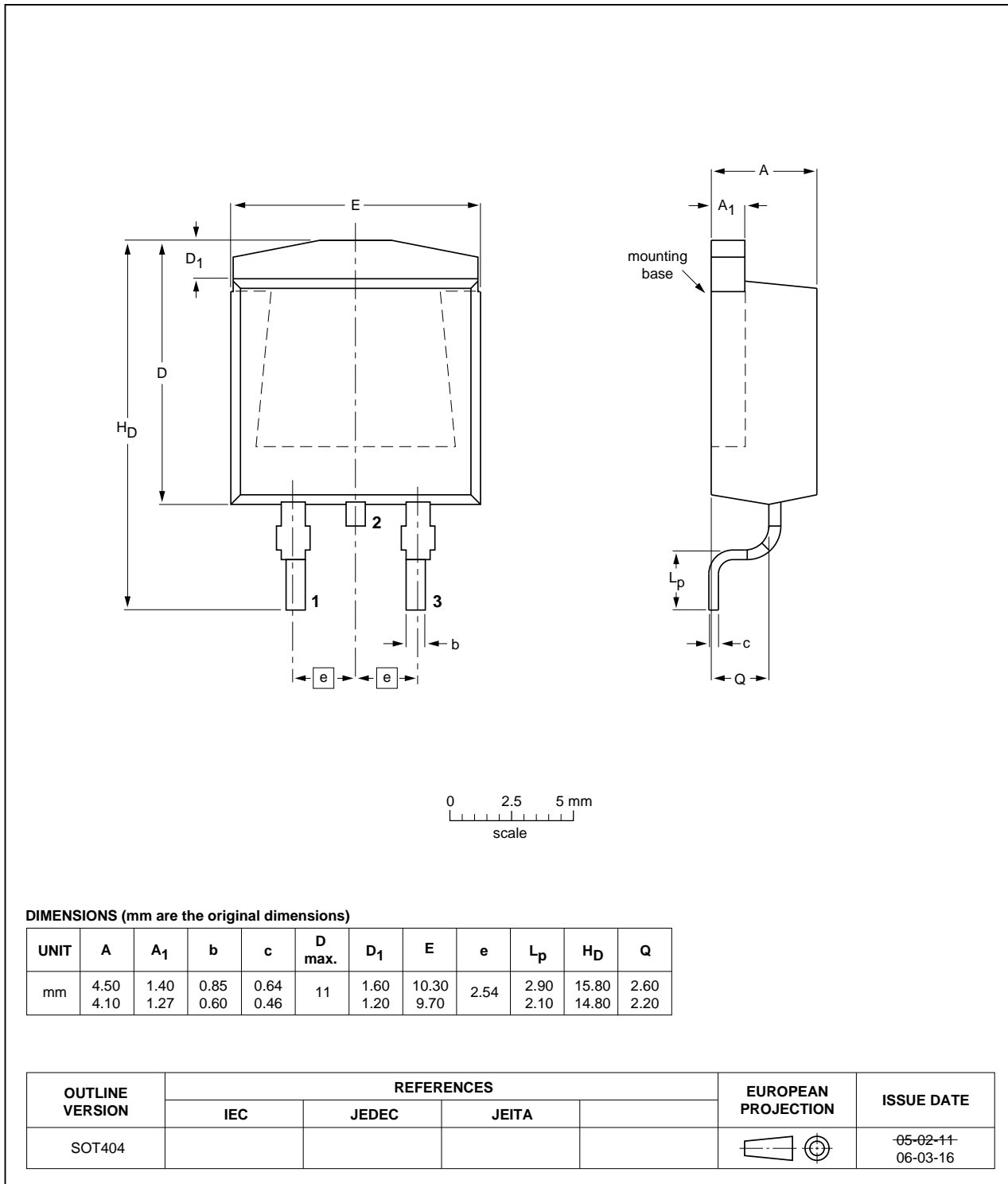


Fig 18. Package outline SOT404 (D2PAK)

## 9. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN4R4-80BS v.1	20120322	Product data sheet	-	-

## 10. Legal information

### 10.1 Data sheet status

Document status <sup>[1]</sup> <sup>[2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[TPCC8103,L1Q\(CM](#) [MIC4420CM-TR](#) [VN1206L](#) [614234A](#) [715780A](#) [NTNS3166NZT5G](#) [SSM6J414TU,LF\(T](#) [751625C](#)  
[IPS70R2K0CEAKMA1](#) [BUK954R8-60E](#) [DMN3404LQ-7](#) [NTE6400](#) [SQJ402EP-T1-GE3](#) [2SK2614\(TE16L1,Q\)](#) [2N7002KW-FAI](#)  
[DMN1017UCP3-7](#) [EFC2J004NUZTDG](#) [ECH8691-TL-W](#) [FCAB21350L1](#) [P85W28HP2F-7071](#) [DMN1053UCP4-7](#) [NTE221](#) [NTE2384](#)  
[NTE2903](#) [NTE2941](#) [NTE2945](#) [NTE2946](#) [NTE2960](#) [NTE2967](#) [NTE2969](#) [NTE2976](#) [NTE455](#) [NTE6400A](#) [NTE2910](#) [NTE2916](#) [NTE2956](#)  
[NTE2911](#) [US6M2GTR](#) [TK10A80W,S4X\(S](#) [SSM6P69NU,LF](#)