



# PSMN4R8-100BSE

N-channel 100 V 4.8 mΩ standard level MOSFET in D2PAK

12 April 2013

Product data sheet

## 1. General description

Standard level N-channel MOSFET in a D2PAK package qualified to 175 °C. Part of Nexperia's "NextPower Live" portfolio, the PSMN4R8-100BSE complements the latest "hot-swap" controllers - robust enough to withstand substantial inrush currents during turn on, whilst offering a low  $R_{DS(on)}$  characteristic to keep temperatures down and efficiency up in continued use. Ideal for telecommunication systems based on a 48 V backplane / supply rail.

## 2. Features and benefits

- Enhanced forward biased safe operating area for superior linear mode operation
- Very low  $R_{DS(on)}$  for low conduction losses

## 3. Applications

- Electronic fuse
- Hot swap
- Load switch
- Soft start

## 4. Quick reference data

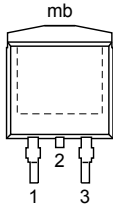
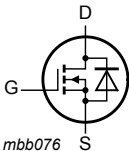
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	-	100	V
$I_{DM}$	peak drain current	pulsed; $T_{mb} = 25\text{ °C}; t_p \leq 10\text{ }\mu\text{s}$ ; <a href="#">Fig. 4</a>	-	-	707	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 2</a>	-	-	405	W
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C}$ ; <a href="#">Fig. 12</a>	-	4.1	4.8	mΩ
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; V_{DS} = 50\text{ V}$ ; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>	-	59	83	nC
$Q_{G(tot)}$	total gate charge		-	196	278	nC

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Avalanche Ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$ ; $T_{j(\text{init})} = 25\text{ °C}$ ; $I_D = 120\text{ A}$ ; $V_{\text{sup}} \leq 100\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; unclamped; <a href="#">Fig. 3</a>	-	-	542	mJ

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p style="text-align: center;"><b>D2PAK (SOT404)</b></p>	 <p style="text-align: center;"><i>mbb076</i></p>
2	D	drain <sup>[1]</sup>		
3	S	source		
mb	D	mounting base; connected to drain		

[1] It is not possible to make connection to pin 2

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN4R8-100BSE	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN4R8-100BSE	PSMN4R8-100BSE

## 8. Limiting values

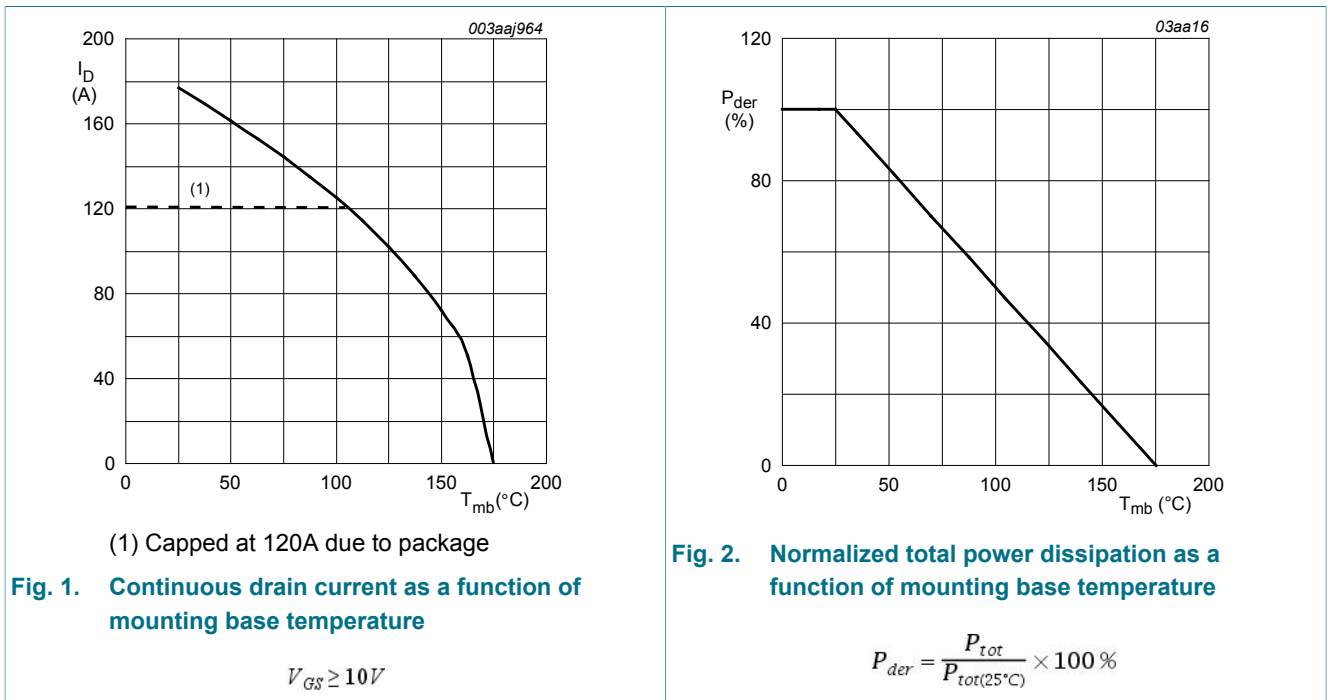
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$	-	100	V
$V_{DGR}$	drain-gate voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$	-	100	V
$V_{GS}$	gate-source voltage		-20	20	V

Symbol	Parameter	Conditions		Min	Max	Unit
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 1</a>	[1]	-	120	A
		V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 100 °C; <a href="#">Fig. 1</a>	[1]	-	120	A
I <sub>DM</sub>	peak drain current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C; <a href="#">Fig. 4</a>		-	707	A
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <a href="#">Fig. 2</a>		-	405	W
T <sub>stg</sub>	storage temperature			-55	175	°C
T <sub>j</sub>	junction temperature			-55	175	°C
T <sub>sld(M)</sub>	peak soldering temperature			-	260	°C
<b>Source-drain diode</b>						
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C	[1]	-	120	A
I <sub>SM</sub>	peak source current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C		-	707	A
<b>Avalanche Ruggedness</b>						
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; I <sub>D</sub> = 120 A; V <sub>sup</sub> ≤ 100 V; R <sub>GS</sub> = 50 Ω; unclamped; <a href="#">Fig. 3</a>		-	542	mJ

[1] Continuous current limited by package.



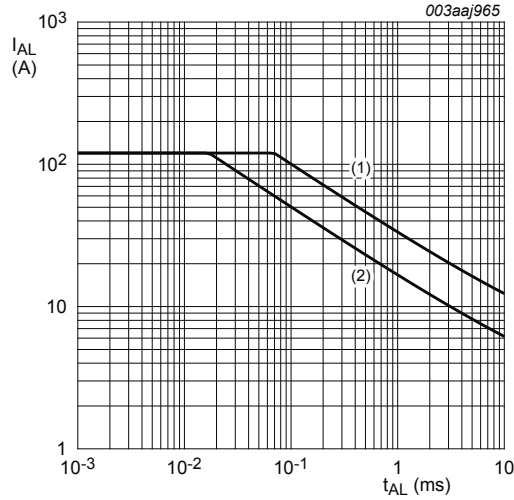


Fig. 3. Single pulse avalanche rating; avalanche current as a function of avalanche time

(1)  $T_{j (int)} = 25^{\circ}C$ ; (2)  $T_{j (int)} = 100^{\circ}C$

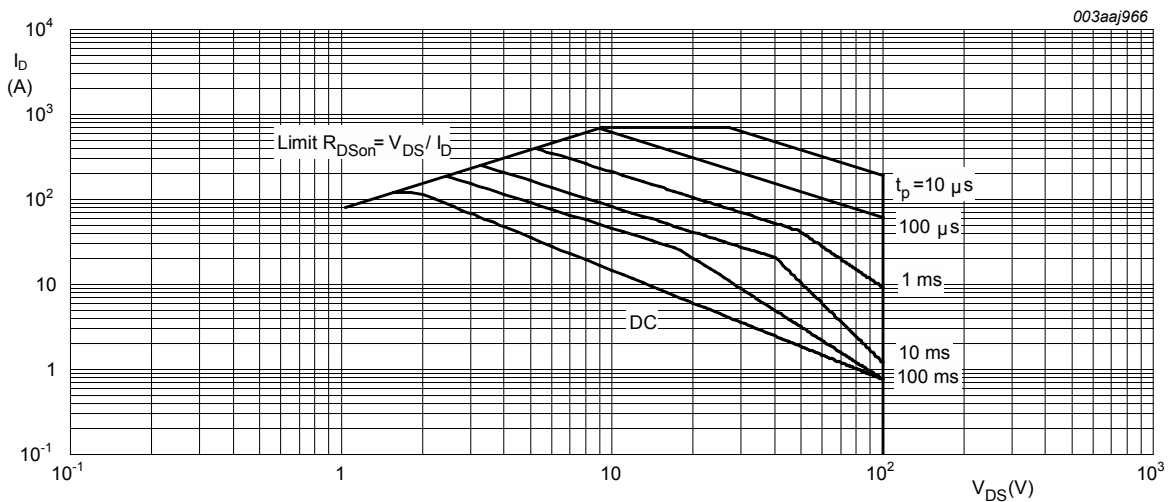


Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^{\circ}C$ ;  $I_{DM}$  is a single pulse; Capped at 120 A due to package

## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	<a href="#">Fig. 5</a>	-	0.3	0.37	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Minimum footprint; mounted on a printed circuit board	-	50	-	K/W

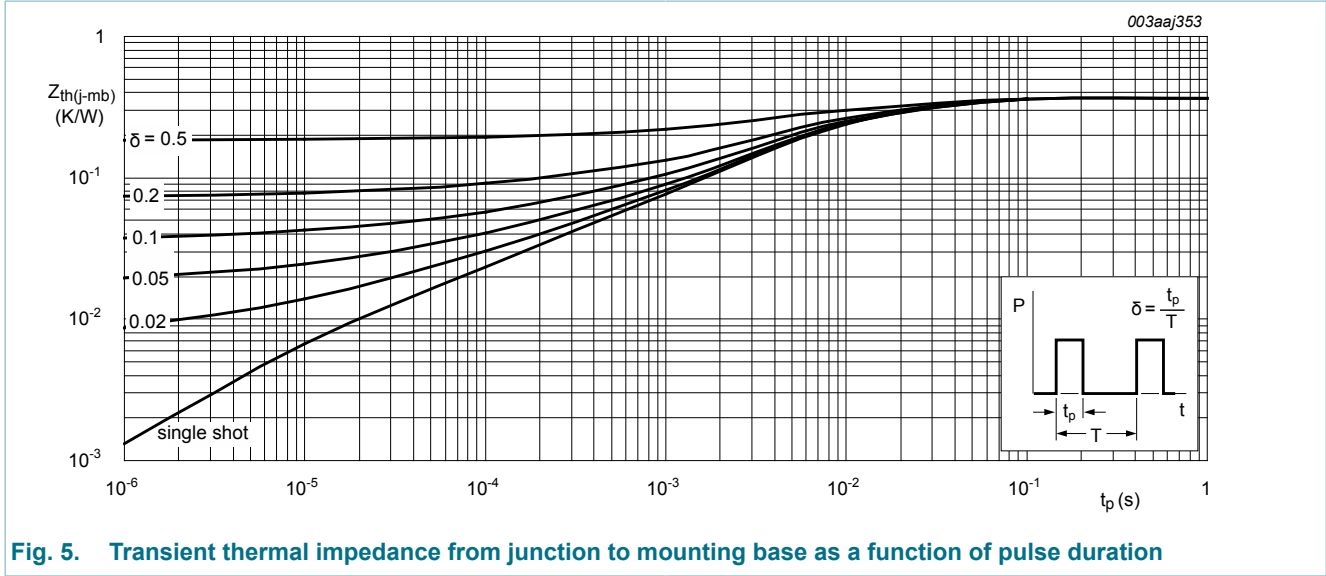


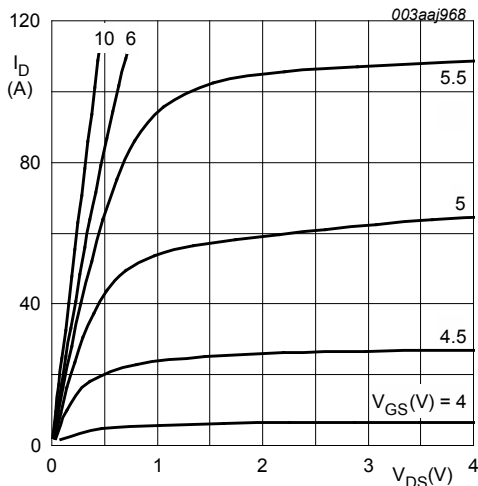
Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

## 10. Characteristics

Table 7. Characteristics

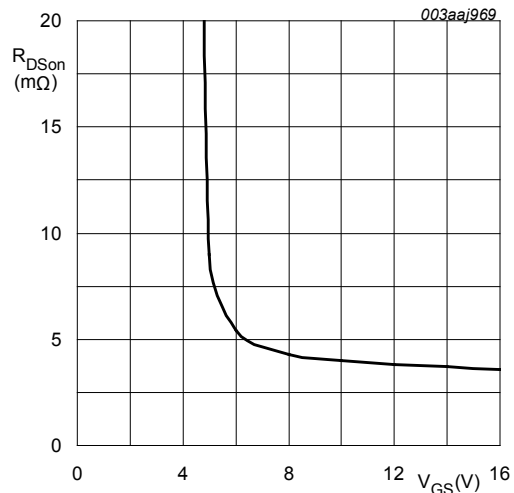
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	100	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	90	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 10; Fig. 11</a>	2	3	4	V
$V_{GSth}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C;$ <a href="#">Fig. 11</a>	1	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C;$ <a href="#">Fig. 11</a>	-	-	4.6	V
$I_{DSS}$	drain leakage current	$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.16	10	$\mu A$
		$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ C$	-	-	500	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	10	100	nA
		$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	10	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 12</a>	-	4.1	4.8	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 100 \text{ }^\circ C;$ <a href="#">Fig. 13; Fig. 12</a>	-	-	8.7	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ C;$ <a href="#">Fig. 12; Fig. 13</a>	-	-	13	mΩ
$R_G$	gate resistance	$f = 1 \text{ MHz}$	0.43	0.85	1.7	Ω

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Dynamic characteristics</b>						
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 50 V; V <sub>GS</sub> = 10 V; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>	-	196	278	nC
		I <sub>D</sub> = 0 A; V <sub>DS</sub> = 0 V; V <sub>GS</sub> = 10 V	-	166.9	234	nC
Q <sub>GS</sub>	gate-source charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 50 V; V <sub>GS</sub> = 10 V; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>	-	40	56	nC
Q <sub>GD</sub>	gate-drain charge		-	59	83	nC
V <sub>GS(pl)</sub>	gate-source plateau voltage	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 50 V; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>	-	4.3	-	V
C <sub>iss</sub>	input capacitance	V <sub>DS</sub> = 50 V; V <sub>GS</sub> = 0 V; f = 1 MHz;	-	10665	14400	pF
C <sub>oss</sub>	output capacitance	T <sub>j</sub> = 25 °C; <a href="#">Fig. 16</a>	-	674	910	pF
C <sub>rss</sub>	reverse transfer capacitance		-	459	643	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = 50 V; R <sub>L</sub> = 2 Ω; V <sub>GS</sub> = 10 V;	-	41	61.5	ns
t <sub>r</sub>	rise time	R <sub>G(ext)</sub> = 4.7 Ω	-	65	97.5	ns
t <sub>d(off)</sub>	turn-off delay time		-	127	190.5	ns
t <sub>f</sub>	fall time		-	69	103.5	ns
<b>Source-drain diode</b>						
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 25 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 17</a>	-	0.79	1.2	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 25 A; di <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V;	-	72	94	ns
Q <sub>r</sub>	recovered charge	V <sub>DS</sub> = 50 V	-	227	296	nC



**Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values**

T<sub>j</sub> = 25 °C



**Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values**

T<sub>j</sub> = 25 °C; I<sub>D</sub> = 25 A

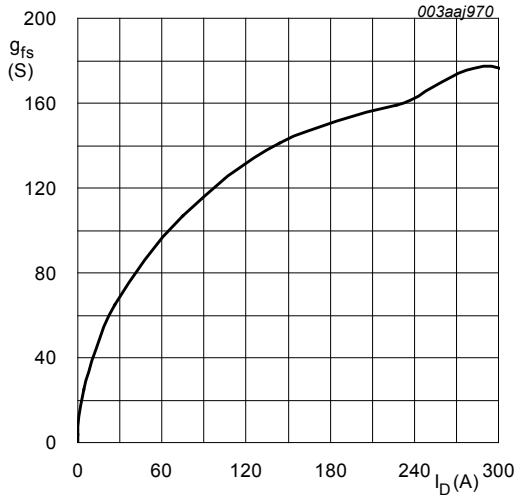


Fig. 8. Forward transconductance as a function of drain current; typical values

$T_j = 25^\circ\text{C}; V_{DS} = 10\text{V}$

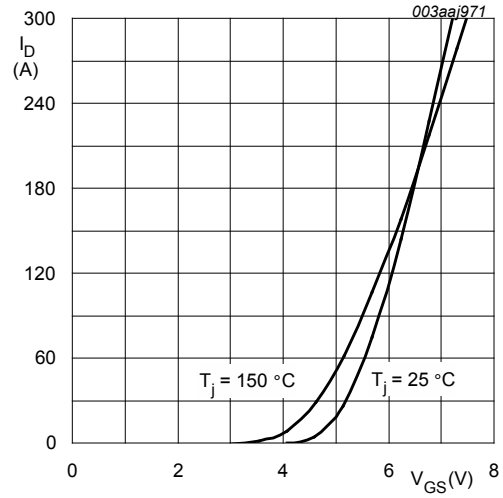


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$V_{DS} = 10\text{V}$

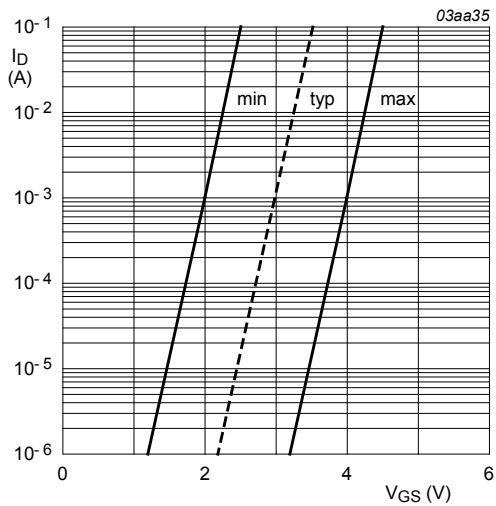


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$

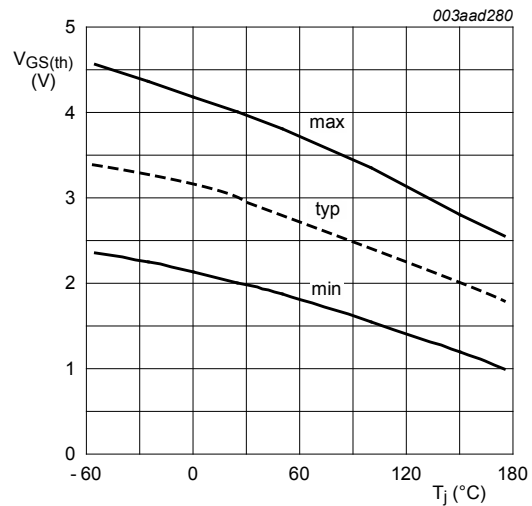
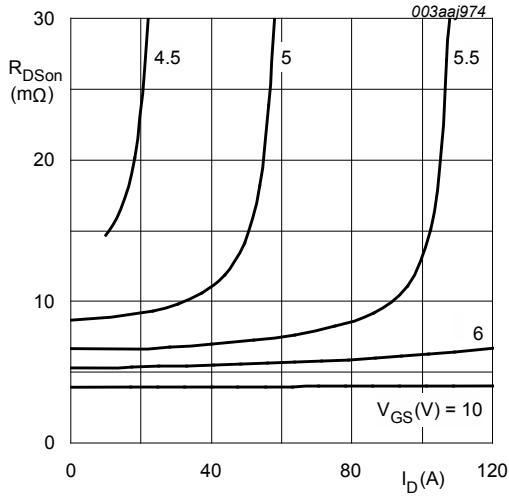


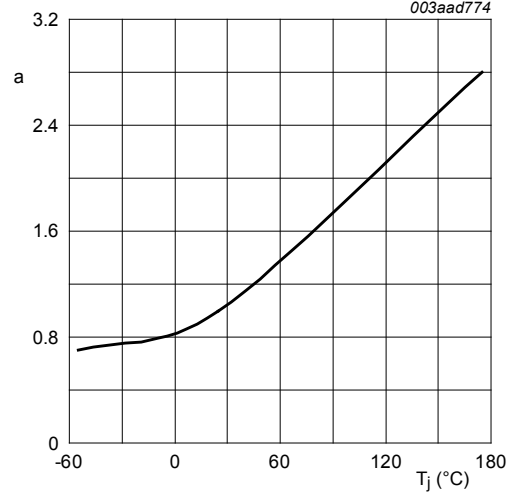
Fig. 11. Gate-source threshold voltage as a function of junction temperature

$I_D = 1\text{ mA}; V_{DS} = V_{GS}$



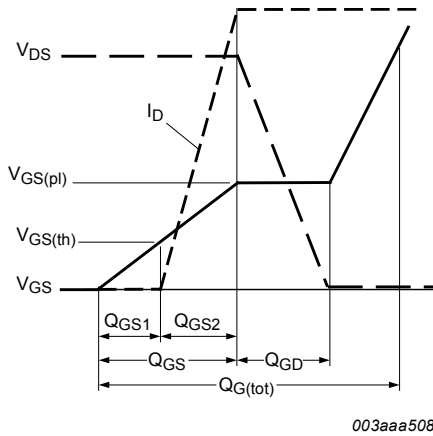
**Fig. 12. Drain-source on-state resistance as a function of drain current; typical values**

$T_j = 25^\circ\text{C}$

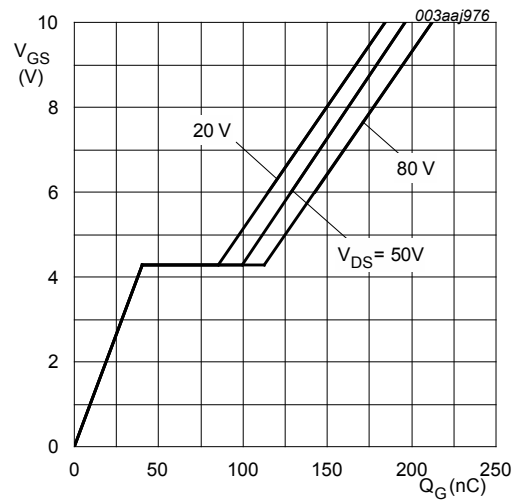


**Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature**

$$a = \frac{R_{DS(on)}}{R_{DS(on)@25^\circ\text{C}}}$$



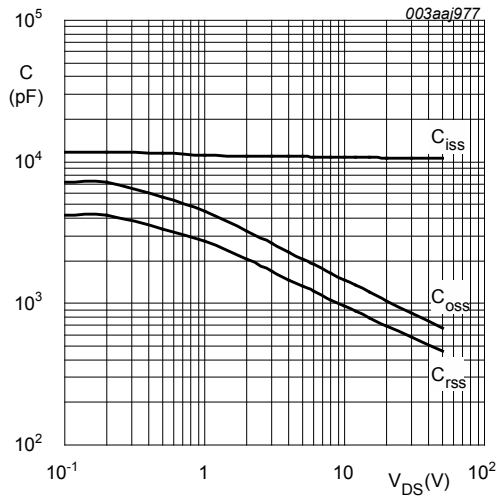
**Fig. 14. Gate charge waveform definitions**



**Fig. 15. Gate-source voltage as a function of gate charge; typical values**

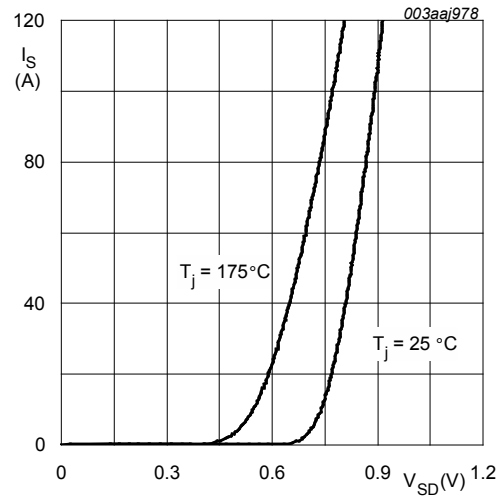
$T_j = 25^\circ\text{C}; I_D = 25\text{A}$





**Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**

$$V_{GS} = 0V; f = 1MHz$$

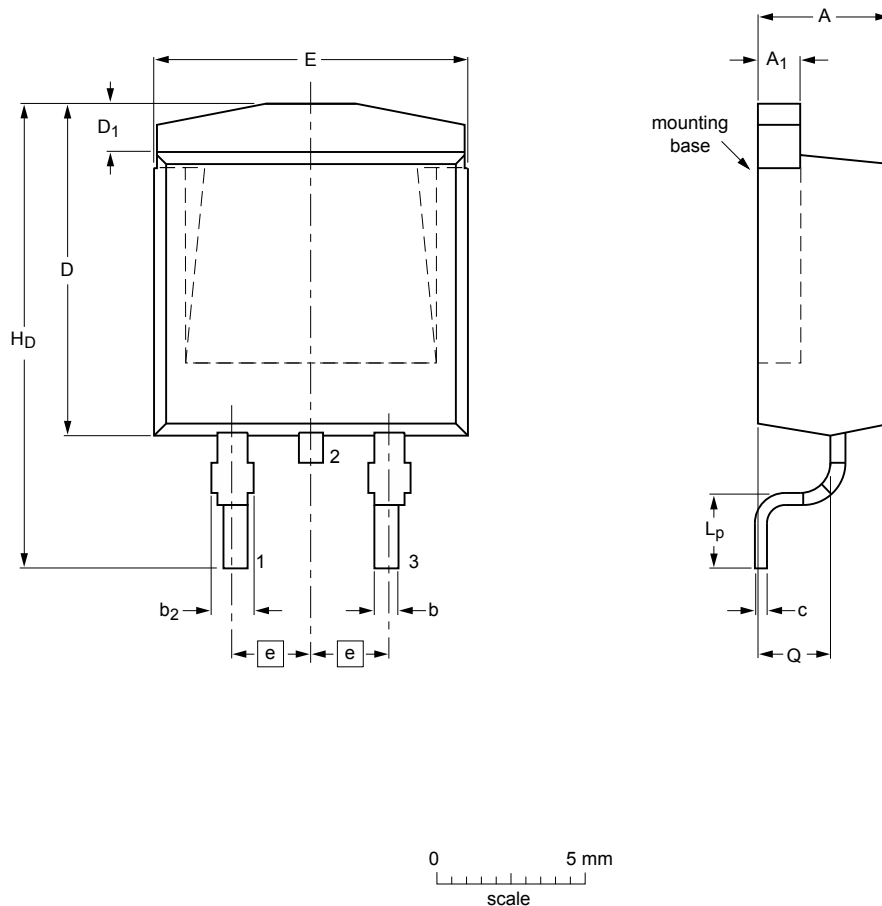


**Fig. 17. Source current as a function of source-drain voltage; typical values**

$$V_{GS} = 0V$$

### 11. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped) SOT404



Dimensions (mm are the original dimensions)

Unit	A	A <sub>1</sub>	b	b <sub>2</sub>	c	D	D <sub>1</sub>	E	e	H <sub>D</sub>	L <sub>p</sub>	Q
max	4.5	1.40	0.85	1.45	0.64	11	1.6	10.3		15.8	2.9	2.6
nom									2.54			
min	4.1	1.27	0.60	1.05	0.46		1.2	9.7		14.8	2.1	2.2

sot404\_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT404					-06-03-16- 13-02-25

Fig. 18. Package outline D2PAK (SOT404)

## 12. Legal information

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