



# PSMN7R6-100BSE

N-channel 100 V 7.6 mΩ standard level MOSFET in D2PAK

18 December 2012

Product data sheet

## 1. General description

Standard level N-channel MOSFET in a D2PAK package qualified to 175 °C. Part of Nexperia's "NextPower Live" portfolio, the PSMN7R6-100BSE complements the latest "hot-swap" controllers - robust enough to withstand substantial inrush currents during turn on, whilst offering a low  $R_{DS(on)}$  characteristic to keep temperatures down and efficiency up in continued use. Ideal for telecommunication systems based on a 48 V backplane / supply rail.

## 2. Features and benefits

- Enhanced forward biased safe operating area for superior linear mode operation
- Very low  $R_{DS(on)}$  for low conduction losses

## 3. Applications

- Electronic fuse
- Hot swap
- Load switch
- Soft start

## 4. Quick reference data

Table 1. Quick reference data

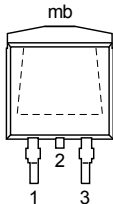
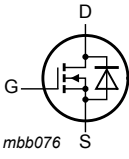
| Symbol                         | Parameter                        | Conditions  |     | Min | Typ | Max | Unit |
|--------------------------------|----------------------------------|---|-----|-----|-----|-----|------|
| $V_{DS}$                       | drain-source voltage             | $T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$   |     | -   | -   | 100 | V    |
| $I_D$                          | drain current                    | $T_{mb} = 100\text{ °C}; V_{GS} = 10\text{ V};$ <a href="#">Fig. 1</a>                            | [1] | -   | -   | 75  | A    |
| $P_{tot}$                      | total power dissipation          | $T_{mb} = 25\text{ °C};$ <a href="#">Fig. 2</a>   |     | -   | -   | 296 | W    |
| <b>Static characteristics</b>  |                                  |   |     |     |     |     |      |
| $R_{DS(on)}$                   | drain-source on-state resistance | $V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C};$ <a href="#">Fig. 12</a>            |     | -   | 6.5 | 7.6 | mΩ   |
| <b>Dynamic characteristics</b> |                                  |   |     |     |     |     |      |
| $Q_{GD}$                       | gate-drain charge                | $V_{GS} = 10\text{ V}; I_D = 25\text{ A}; V_{DS} = 50\text{ V};$ <a href="#">Fig. 14; Fig. 15</a> |     | -   | 41  | -   | nC   |
| $Q_{G(tot)}$                   | total gate charge                |   |     | -   | 128 | -   | nC   |

| Symbol                      | Parameter                                    | Conditions   | Min | Typ | Max | Unit |
|-----------------------------|--|--|-----|-----|-----|------|
| <b>Avalanche Ruggedness</b> |  |  |     |     |     |      |
| $E_{DS(AL)S}$               | non-repetitive drain-source avalanche energy | $V_{GS} = 10\text{ V}$ ; $T_{j(\text{init})} = 25\text{ °C}$ ; $I_D = 75\text{ A}$ ; $V_{sup} \leq 100\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; unclamped; <a href="#">Fig. 3</a> | -   | -   | 426 | mJ   |

[1] Continuous current limited by package

## 5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description                       | Simplified outline   | Graphic symbol   |
|-----|--------|-----------------------------------|--|--|
| 1   | G      | gate                              |  <p style="text-align: center;"><b>D2PAK (SOT404)</b></p> |  <p style="text-align: center;"><i>mbb076</i></p> |
| 2   | D      | drain <sup>[1]</sup>              |  |  |
| 3   | S      | source                            |  |  |
| mb  | D      | mounting base; connected to drain |  |  |

[1] It is not possible to make connection to pin 2

## 6. Ordering information

Table 3. Ordering information

| Type number    | Package |  | Version |
|----------------|---------|--|---------|
|                | Name    | Description  |         |
| PSMN7R6-100BSE | D2PAK   | plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped) | SOT404  |

## 7. Marking

Table 4. Marking codes

| Type number    | Marking code  |
|----------------|---------------|
| PSMN7R6-100BSE | PSMN7R6100BSE |

## 8. Limiting values

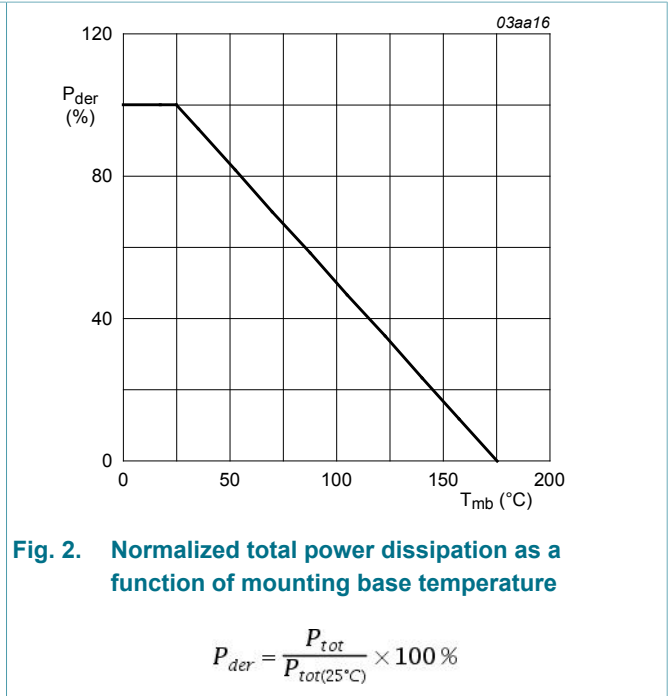
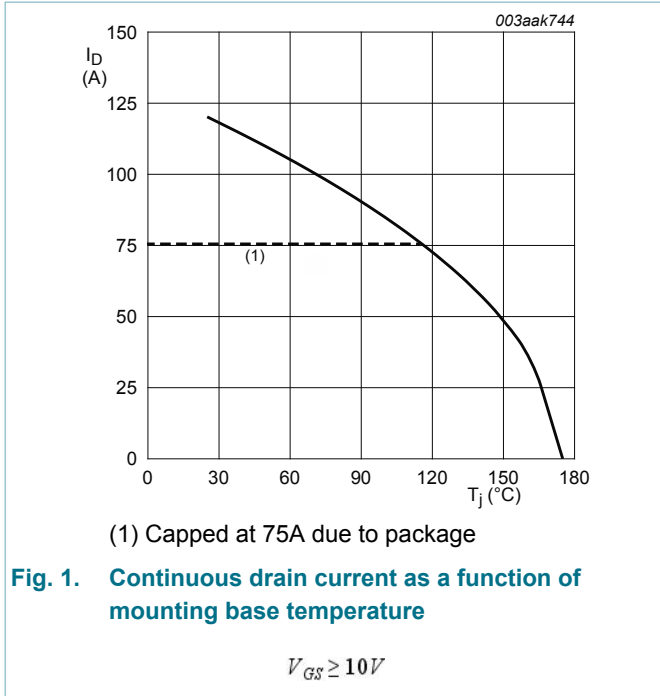
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol    | Parameter            | Conditions  | Min | Max | Unit |
|-----------|----------------------|---|-----|-----|------|
| $V_{DS}$  | drain-source voltage | $T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$                                | -   | 100 | V    |
| $V_{DGR}$ | drain-gate voltage   | $T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$ | -   | 100 | V    |

| Symbol                      | Parameter                                    | Conditions   |     | Min | Max | Unit |
|-----------------------------|--|--|-----|-----|-----|------|
| V <sub>GS</sub>             | gate-source voltage                          |  |     | -20 | 20  | V    |
| I <sub>D</sub>              | drain current                                | V <sub>GS</sub> = 10 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 1</a>   | [1] | -   | 75  | A    |
|                             |  | V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 100 °C; <a href="#">Fig. 1</a>   | [1] | -   | 75  | A    |
| I <sub>DM</sub>             | peak drain current                           | pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C; <a href="#">Fig. 4</a>  |     | -   | 481 | A    |
| P <sub>tot</sub>            | total power dissipation                      | T <sub>mb</sub> = 25 °C; <a href="#">Fig. 2</a>  |     | -   | 296 | W    |
| T <sub>stg</sub>            | storage temperature                          |  |     | -55 | 175 | °C   |
| T <sub>j</sub>              | junction temperature                         |  |     | -55 | 175 | °C   |
| T <sub>sld(M)</sub>         | peak soldering temperature                   |  |     | -   | 260 | °C   |
| <b>Source-drain diode</b>   |  |  |     |     |     |      |
| I <sub>S</sub>              | source current                               | T <sub>mb</sub> = 25 °C  | [1] | -   | 75  | A    |
| I <sub>SM</sub>             | peak source current                          | pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C  |     | -   | 481 | A    |
| <b>Avalanche Ruggedness</b> |  |  |     |     |     |      |
| E <sub>DS(AL)S</sub>        | non-repetitive drain-source avalanche energy | V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; I <sub>D</sub> = 75 A; V <sub>sup</sub> ≤ 100 V; R <sub>GS</sub> = 50 Ω; unclamped; <a href="#">Fig. 3</a> |     | -   | 426 | mJ   |

[1] Continuous current limited by package



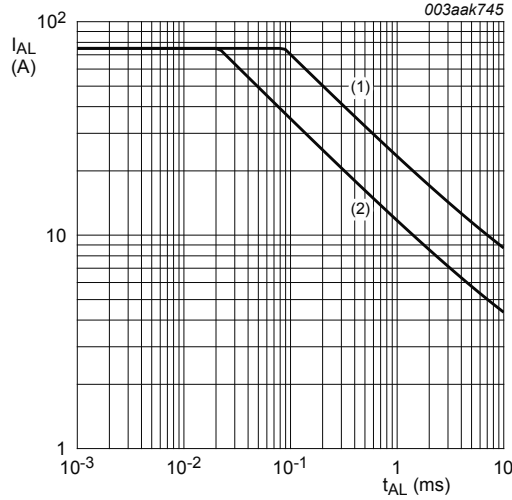


Fig. 3. Single pulse avalanche rating; avalanche current as a function of avalanche time

(1)  $T_{j (init)} = 25^{\circ}C$ ; (2)  $T_{j (init)} = 100^{\circ}C$

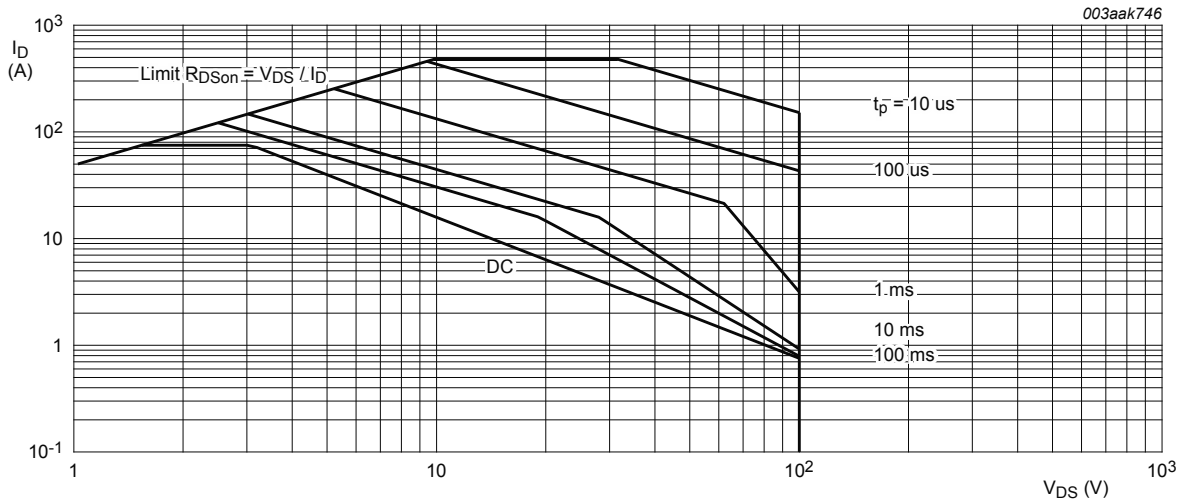


Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^{\circ}C$ ;  $I_{DM}$  is a single pulse

## 9. Thermal characteristics

Table 6. Thermal characteristics

| Symbol         | Parameter   | Conditions  | Min | Typ  | Max  | Unit |
|----------------|---|---|-----|------|------|------|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | Fig. 5  | -   | 0.42 | 0.51 | K/W  |
| $R_{th(j-a)}$  | thermal resistance from junction to ambient       | Minimum footprint; mounted on a printed circuit board | -   | 50   | -    | K/W  |

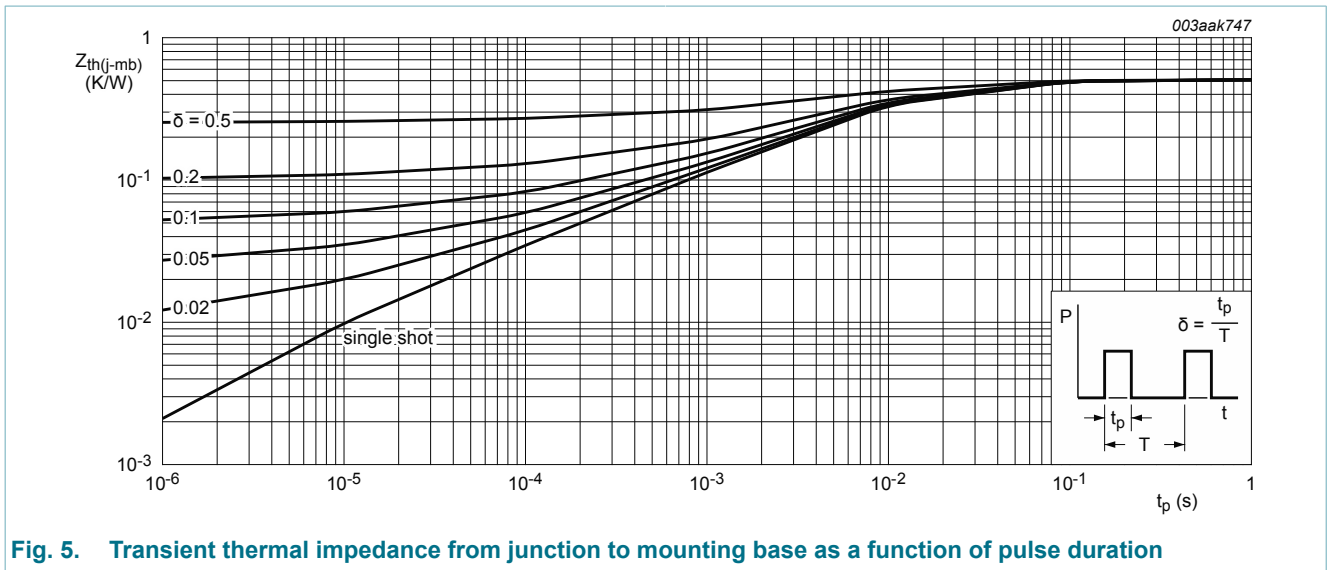


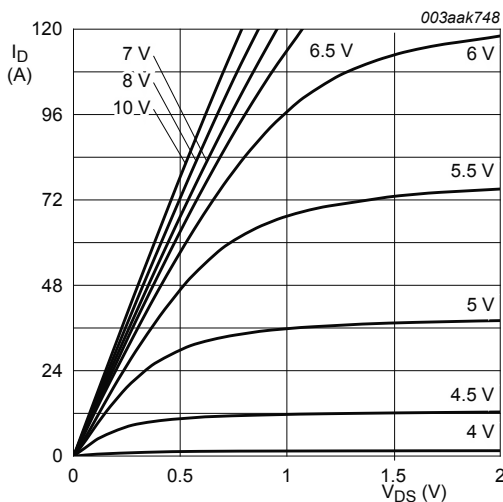
Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

## 10. Characteristics

Table 7. Characteristics

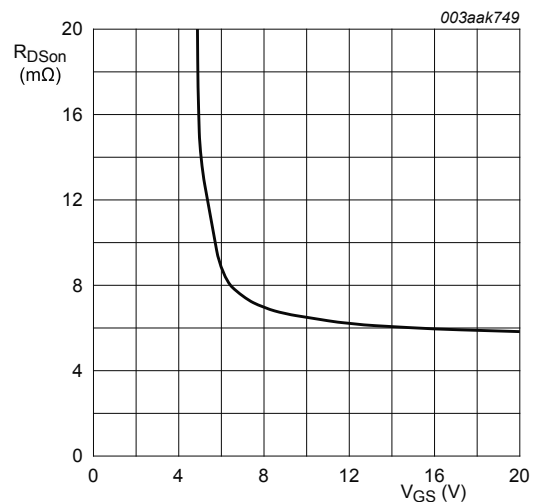
| Symbol                        | Parameter                        | Conditions   | Min  | Typ  | Max  | Unit    |
|-------------------------------|----------------------------------|--|------|------|------|---------|
| <b>Static characteristics</b> |                                  |  |      |      |      |         |
| $V_{(BR)DSS}$                 | drain-source breakdown voltage   | $I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$   | 100  | -    | -    | V       |
|                               |                                  | $I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$  | 90   | -    | -    | V       |
| $V_{GS(th)}$                  | gate-source threshold voltage    | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$ ;<br><a href="#">Fig. 10</a> ; <a href="#">Fig. 11</a>        | 2    | 3    | 4    | V       |
| $V_{GSth}$                    | gate-source threshold voltage    | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C$ ;<br><a href="#">Fig. 11</a>                                 | 1    | -    | -    | V       |
|                               |                                  | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C$ ;<br><a href="#">Fig. 11</a>                                 | -    | -    | 4.6  | V       |
| $I_{DSS}$                     | drain leakage current            | $V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$  | -    | 0.1  | 2    | $\mu A$ |
|                               |                                  | $V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ C$   | -    | -    | 500  | $\mu A$ |
| $I_{GSS}$                     | gate leakage current             | $V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$  | -    | 10   | 100  | nA      |
|                               |                                  | $V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$   | -    | 10   | 100  | nA      |
| $R_{DSon}$                    | drain-source on-state resistance | $V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C$ ;<br><a href="#">Fig. 12</a>                            | -    | 6.5  | 7.6  | mΩ      |
|                               |                                  | $V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 100 \text{ }^\circ C$ ;<br><a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a> | -    | -    | 13.7 | mΩ      |
|                               |                                  | $V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ C$ ;<br><a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a> | -    | -    | 20.5 | mΩ      |
| $R_G$                         | gate resistance                  | $f = 1 \text{ MHz}$  | 0.42 | 0.83 | 1.66 | Ω       |

| Symbol                         | Parameter                    | Conditions  | Min | Typ  | Max | Unit |
|--------------------------------|------------------------------|---|-----|------|-----|------|
| <b>Dynamic characteristics</b> |                              |   |     |      |     |      |
| Q <sub>G(tot)</sub>            | total gate charge            | I <sub>D</sub> = 25 A; V <sub>DS</sub> = 50 V; V <sub>GS</sub> = 10 V;<br><a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a> | -   | 128  | -   | nC   |
|                                |                              | I <sub>D</sub> = 0 A; V <sub>DS</sub> = 0 V; V <sub>GS</sub> = 10 V   | -   | 110  | -   | nC   |
| Q <sub>GS</sub>                | gate-source charge           | I <sub>D</sub> = 25 A; V <sub>DS</sub> = 50 V; V <sub>GS</sub> = 10 V;<br><a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a> | -   | 33   | -   | nC   |
| Q <sub>GD</sub>                | gate-drain charge            |   | -   | 41   | -   | nC   |
| V <sub>GS(pl)</sub>            | gate-source plateau voltage  | I <sub>D</sub> = 25 A; V <sub>DS</sub> = 50 V; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>                            | -   | 5.3  | -   | V    |
| C <sub>iss</sub>               | input capacitance            | V <sub>DS</sub> = 50 V; V <sub>GS</sub> = 0 V; f = 1 MHz;   | -   | 7110 | -   | pF   |
| C <sub>oss</sub>               | output capacitance           | T <sub>j</sub> = 25 °C; <a href="#">Fig. 16</a>   | -   | 450  | -   | pF   |
| C <sub>rss</sub>               | reverse transfer capacitance |   | -   | 310  | -   | pF   |
| t <sub>d(on)</sub>             | turn-on delay time           | V <sub>DS</sub> = 50 V; R <sub>L</sub> = 2 Ω; V <sub>GS</sub> = 10 V;   | -   | 31   | -   | ns   |
| t <sub>r</sub>                 | rise time                    | R <sub>G(ext)</sub> = 5 Ω   | -   | 48   | -   | ns   |
| t <sub>d(off)</sub>            | turn-off delay time          |   | -   | 82   | -   | ns   |
| t <sub>f</sub>                 | fall time                    |   | -   | 47   | -   | ns   |
| <b>Source-drain diode</b>      |                              |   |     |      |     |      |
| V <sub>SD</sub>                | source-drain voltage         | I <sub>S</sub> = 25 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 17</a>                               | -   | 0.8  | 1.2 | V    |
| t <sub>rr</sub>                | reverse recovery time        | I <sub>S</sub> = 25 A; di <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V;  | -   | 69   | -   | ns   |
| Q <sub>r</sub>                 | recovered charge             | V <sub>DS</sub> = 50 V  | -   | 210  | -   | nC   |



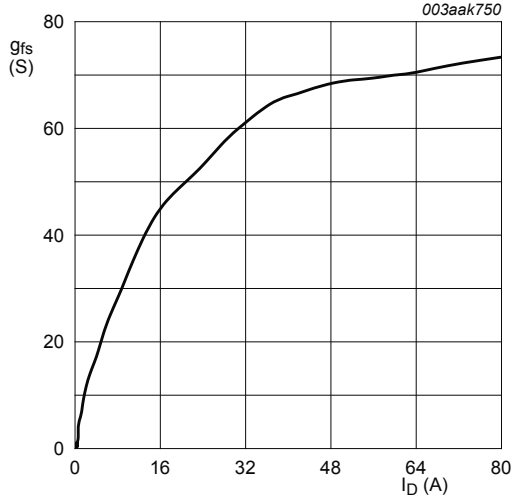
**Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values**

T<sub>j</sub> = 25 °C



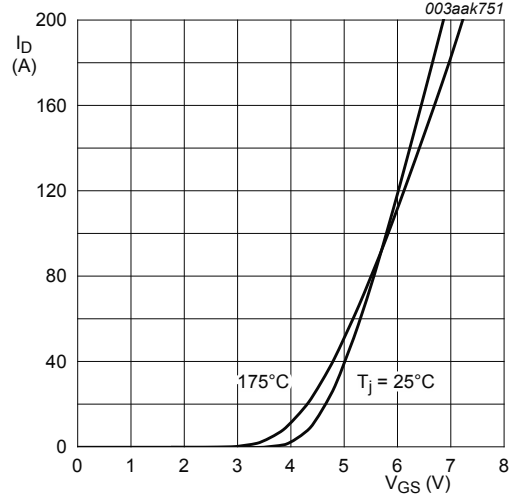
**Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values**

T<sub>j</sub> = 25 °C; I<sub>D</sub> = 25 A



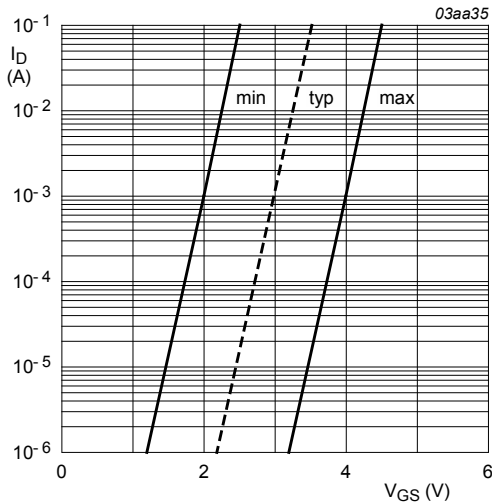
**Fig. 8. Forward transconductance as a function of drain current; typical values**

$T_j = 25^\circ\text{C}; V_{DS} = 10\text{V}$



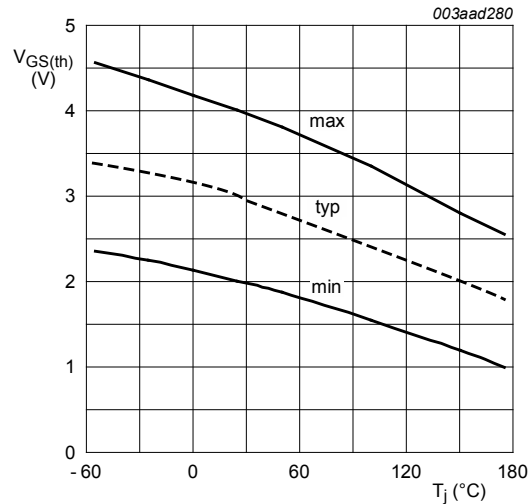
**Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values**

$V_{DS} = 10\text{V}$



**Fig. 10. Sub-threshold drain current as a function of gate-source voltage**

$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$



**Fig. 11. Gate-source threshold voltage as a function of junction temperature**

$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

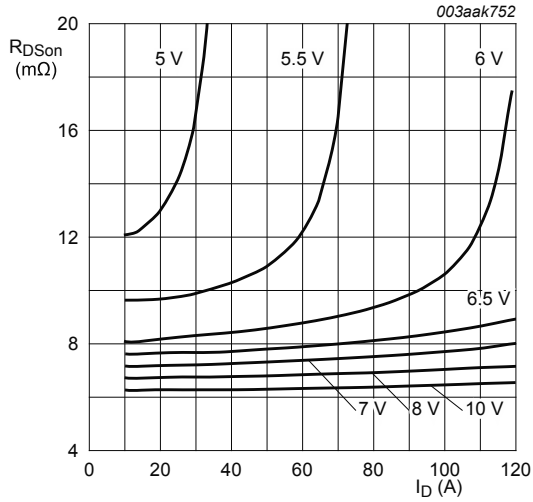


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

$$T_j = 25^\circ\text{C}$$

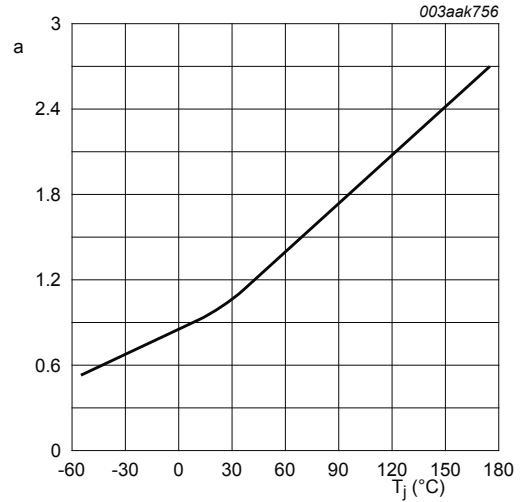


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DS(on)}}{R_{DS(on)}(25^\circ\text{C})}$$

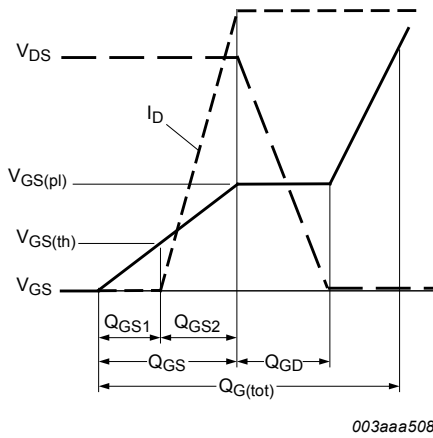


Fig. 14. Gate charge waveform definitions

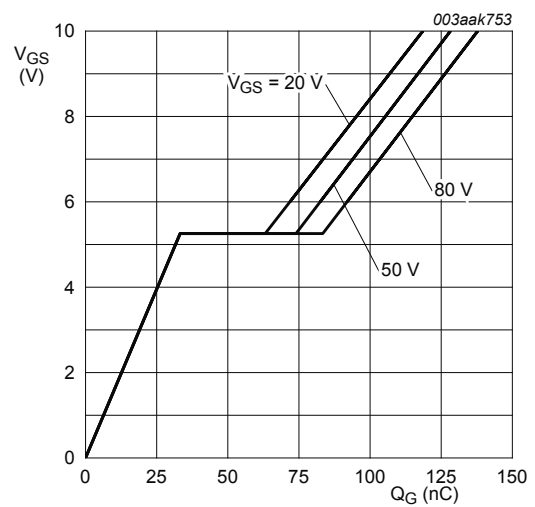
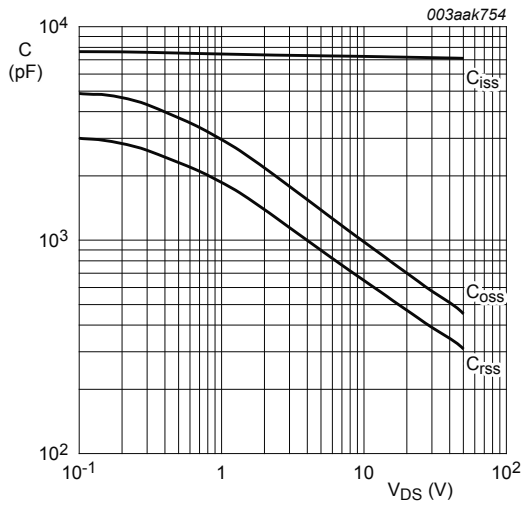


Fig. 15. Gate-source voltage as a function of gate charge; typical values

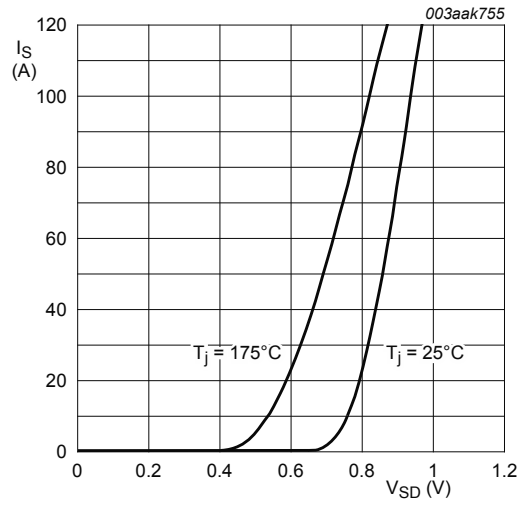
$$T_j = 25^\circ\text{C}; I_D = 25\text{A}$$





**Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**

$$V_{GS} = 0V; f = 1MHz$$



**Fig. 17. Source current as a function of source-drain voltage; typical values**

$$V_{GS} = 0V$$

### 11. Package outline

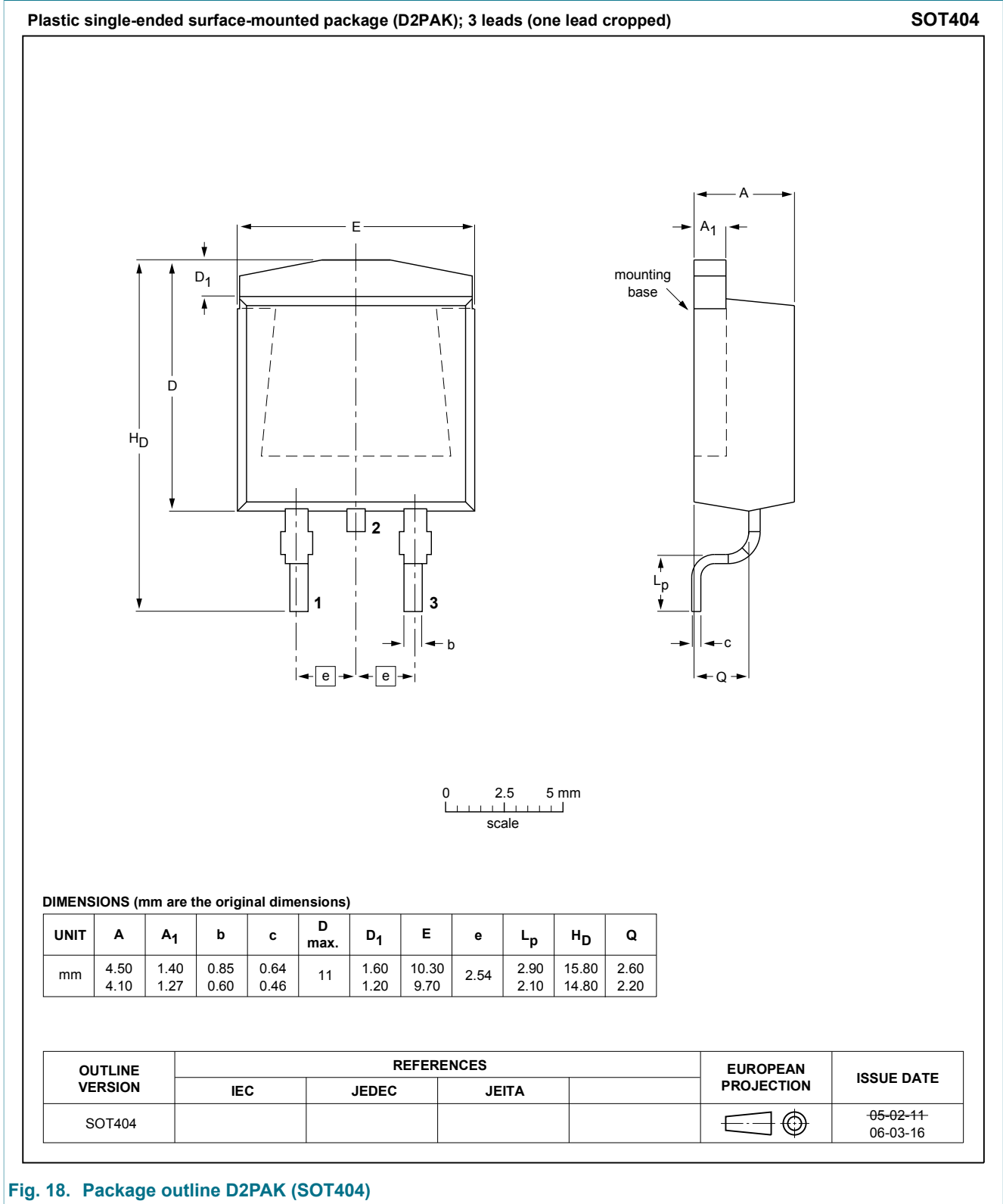


Fig. 18. Package outline D2PAK (SOT404)

## 12. Legal information

### 12.1 Data sheet status

| Document status [1][2]         | Product status [3] | Definition  |
|--------------------------------|--------------------|---|
| Objective [short] data sheet   | Development        | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification      | This document contains data from the preliminary specification.                       |
| Product [short] data sheet     | Production         | This document contains the product specification.                                     |

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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