



PSMN8R9-100BSE

N-channel 100 V, 10 mOhm, standard level MOSFET in D2PAK

28 October 2020

Product data sheet

1. General description

SuperSOA N-channel enhancement mode MOSFET in a D2PAK package qualified to 175 °C. PSMN8R9-100BSE delivers low $R_{DS(on)}$ and very strong linear-mode (SOA) performance, and complements the latest "hot-swap" controllers - robust enough to withstand substantial inrush currents during turn on, low $R_{DS(on)}$ to minimize I^2R losses and deliver optimum efficiency when turned fully ON.

2. Features and benefits

- Avalanche rated, 100% tested
- Low $R_{DS(on)}$ for low I^2R conduction losses
- D2PAK package

3. Applications

- Hot swap
- Load switch
- Soft start
- E-fuse
- Telecommunication systems based on a 48 V backplane/supply rail

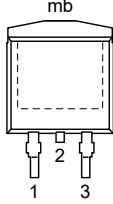
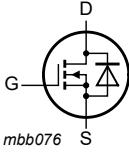
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	100	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	-	-	75	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; Fig. 3	-	-	419	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	-	296	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; Fig. 12	-	8	10	m Ω
Dynamic characteristics						
Q_{GD}	gate-drain charge	$I_D = 25\text{ A}$; $V_{DS} = 50\text{ V}$; $V_{GS} = 10\text{ V}$; Fig. 14 ; Fig. 15	-	32	45	nC
$Q_{G(tot)}$	total gate charge		-	114	160	nC
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 75\text{ A}$; $V_{sup} \leq 100\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped; Fig. 4	-	-	422	mJ

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>D2PAK (SOT404)</p>	
2	D	drain[1]		
3	S	source		
mb	D	mounting base; connected to drain		

[1] It is not possible to make connection to pin 2.

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN8R9-100BSE	D2PAK	plastic, single-ended surface-mounted package (D2PAK); 3 terminals (one lead cropped); 2.54 mm pitch; 11 mm x 10 mm x 4.3 mm body	SOT404

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN8R9-100BSE	PSMN8R9 100BSE

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	100	V
V_{DGR}	drain-gate voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	100	V
V_{GS}	gate-source voltage		-20	20	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	296	W
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	-	75	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; Fig. 2	-	74	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; Fig. 3	-	419	A
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
$T_{slid(M)}$	peak soldering temperature		-	260	°C
Source-drain diode					
I_S	source current	$T_{mb} = 25\text{ °C}$	-	75	A

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Symbol	Parameter	Conditions	Min	Max	Unit
I_{SM}	peak source current	pulsed; $t_p \leq 10 \mu s$; $T_{mb} = 25^\circ C$	-	419	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 75 A$; $V_{sup} \leq 100 V$; $R_{GS} = 50 \Omega$; $V_{GS} = 10 V$; $T_{j(init)} = 25^\circ C$; unclamped; Fig. 4	-	422	mJ

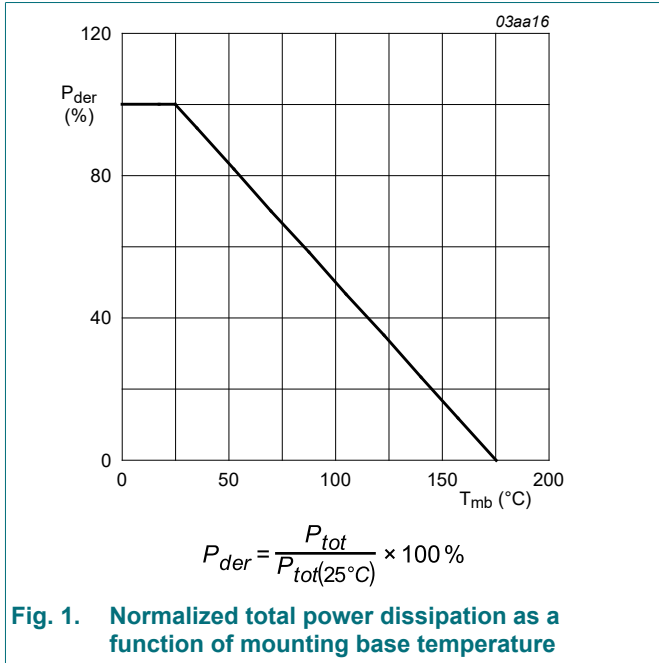


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

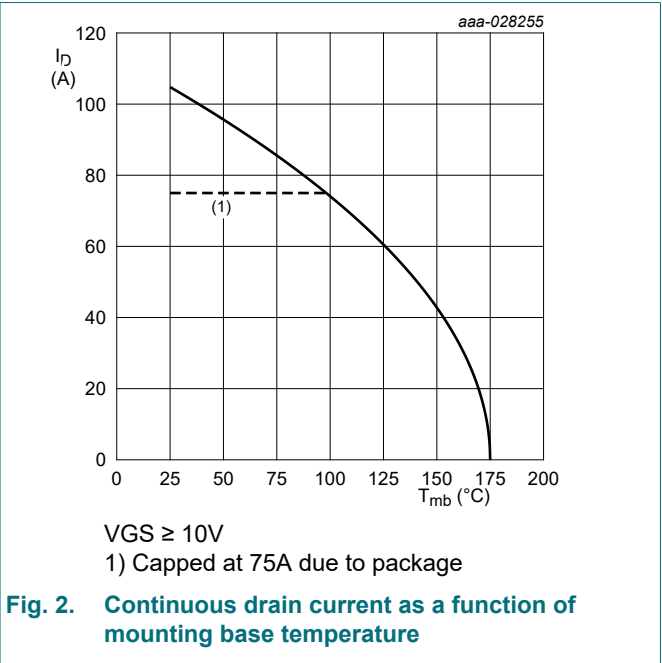


Fig. 2. Continuous drain current as a function of mounting base temperature

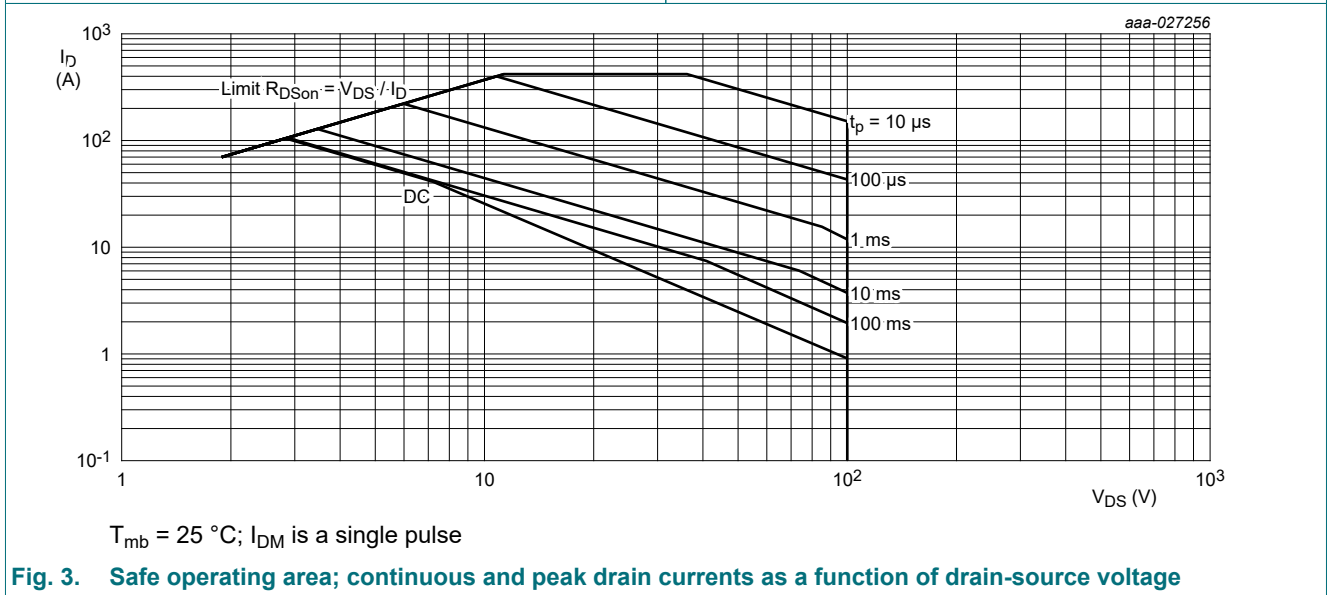
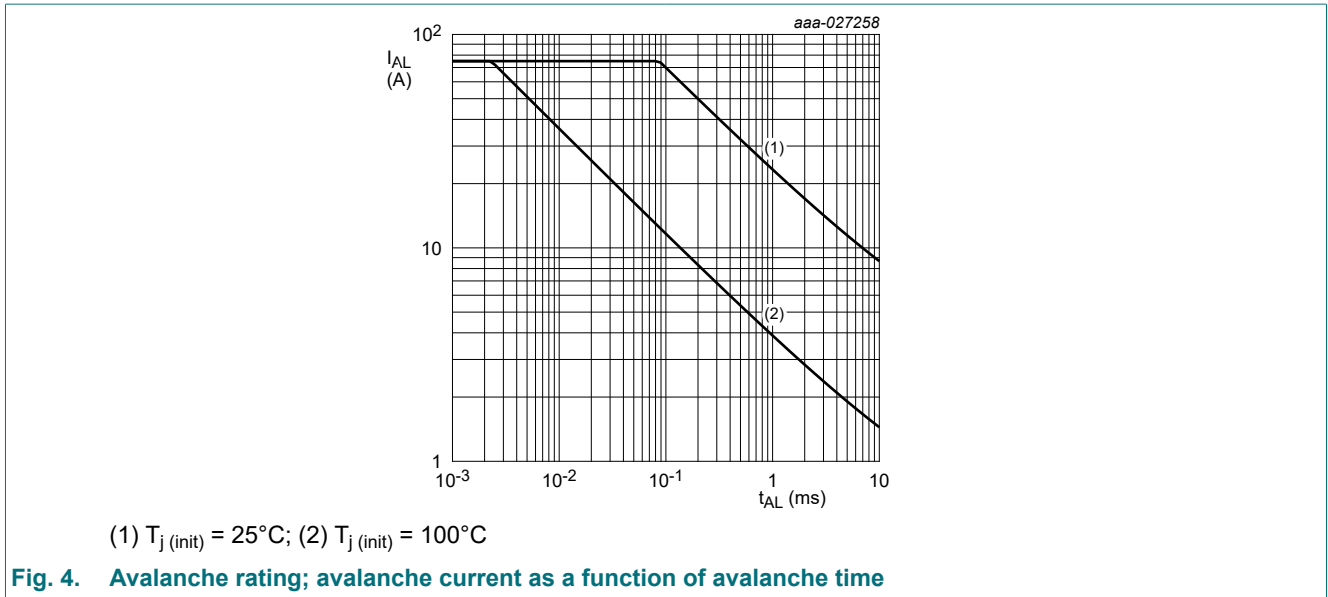


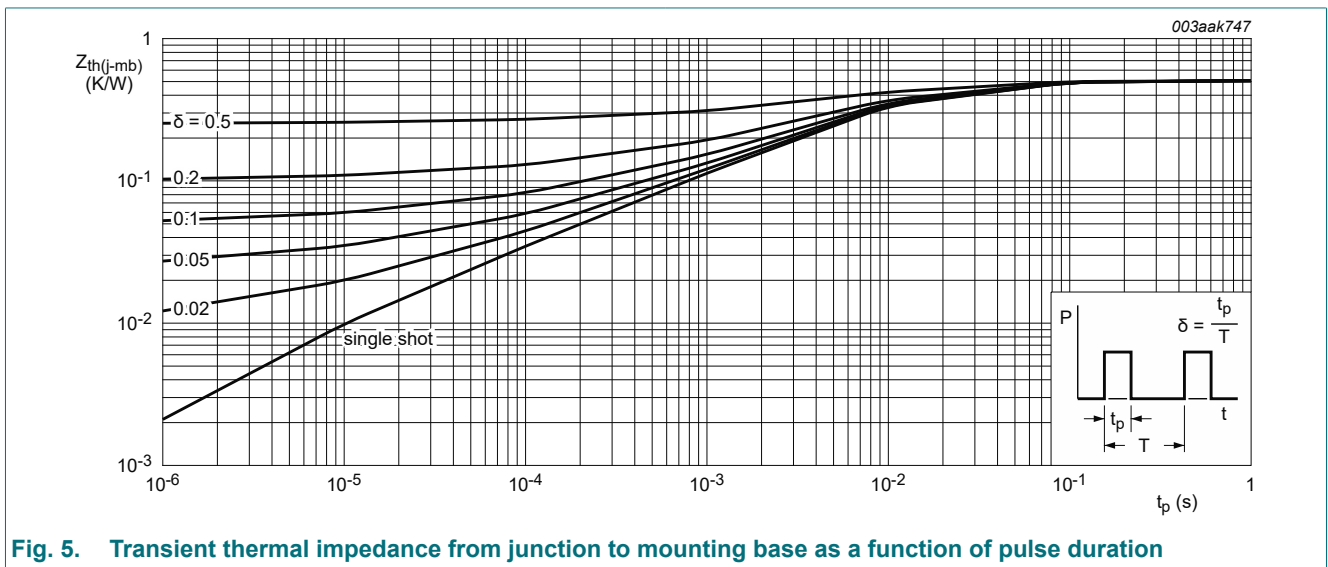
Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{\text{th}(j\text{-mb})}$	thermal resistance from junction to mounting base	Fig. 5	-	0.42	0.51	K/W
$R_{\text{th}(j\text{-a})}$	thermal resistance from junction to ambient		-	50	-	K/W



10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	100	-	-	V
		$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	90	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 10 ; Fig. 11	1.8	2.7	4	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 175 \text{ }^\circ\text{C};$ Fig. 11	1	-	-	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ Fig. 11	-	-	4.6	V
I_{DSS}	drain leakage current	$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.1	2	μA
		$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ\text{C}$	-	-	500	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 12	-	8	10	m Ω
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 100 \text{ }^\circ\text{C};$ Fig. 13	-	-	18.5	m Ω
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ\text{C};$ Fig. 13	-	-	27	m Ω
R_G	gate resistance	$f = 1 \text{ MHz}$	0.4	0.8	1.6	m Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 50 \text{ V}; V_{GS} = 10 \text{ V};$ Fig. 14 ; Fig. 15	-	114	160	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$	-	45	63	nC
Q_{GS}	gate-source charge	$I_D = 25 \text{ A}; V_{DS} = 50 \text{ V}; V_{GS} = 10 \text{ V};$ Fig. 14 ; Fig. 15	-	33	46	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	18	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	15	-	nC
Q_{GD}	gate-drain charge		-	32	45	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25 \text{ A}; V_{DS} = 50 \text{ V};$ Fig. 14 ; Fig. 15	-	5.3	-	V
C_{iss}	input capacitance	$V_{DS} = 50 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ Fig. 16	-	7028	9488	pF
C_{oss}	output capacitance	$T_j = 25 \text{ }^\circ\text{C};$ Fig. 16	-	447	603	pF
C_{rss}	reverse transfer capacitance		-	237	332	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 50 \text{ V}; R_L = 2 \text{ } \Omega; V_{GS} = 10 \text{ V};$ Fig. 16	-	28	42	ns
t_r	rise time	$R_{G(ext)} = 5 \text{ } \Omega$	-	52	78	ns
$t_{d(off)}$	turn-off delay time		-	60	90	ns
t_f	fall time		-	44	66	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 17	-	0.83	1.2	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{rr}	reverse recovery time	$I_S = 25 \text{ A}$; $di_S/dt = -100 \text{ A}/\mu\text{s}$; $V_{GS} = 0 \text{ V}$;	-	77	100	ns
Q_r	recovered charge	$V_{DS} = 50 \text{ V}$	[1]	248	322	nC

[1] includes capacitive recovery

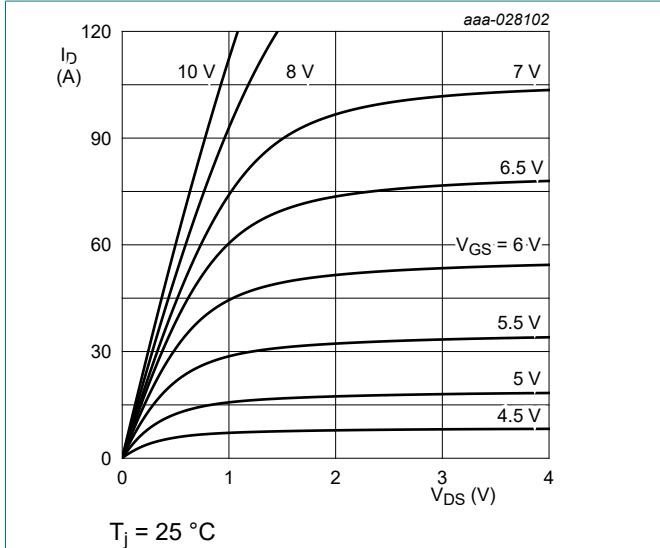


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

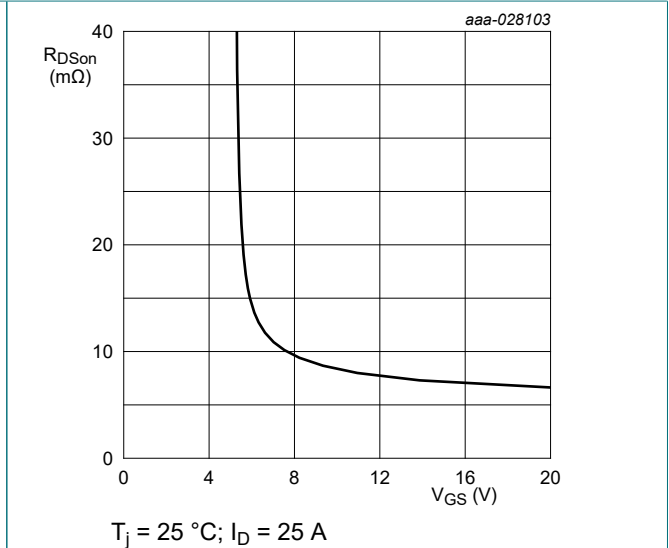


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

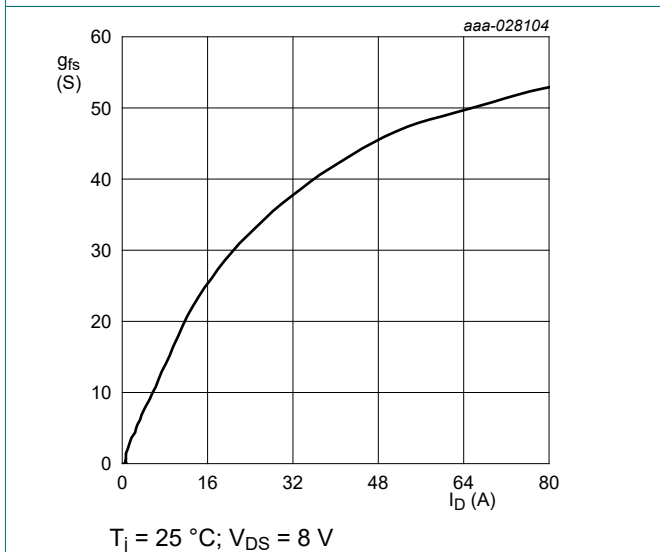


Fig. 8. Forward transconductance as a function of drain current; typical values

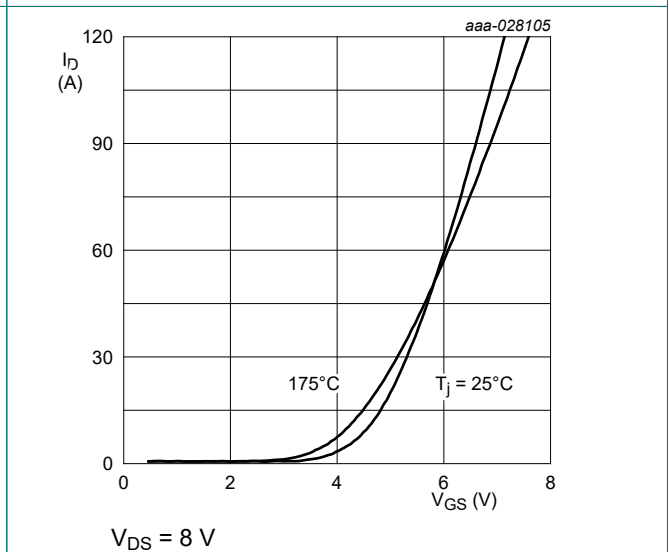


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

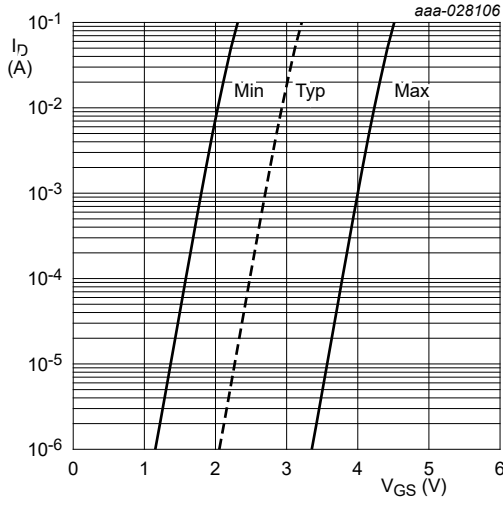


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

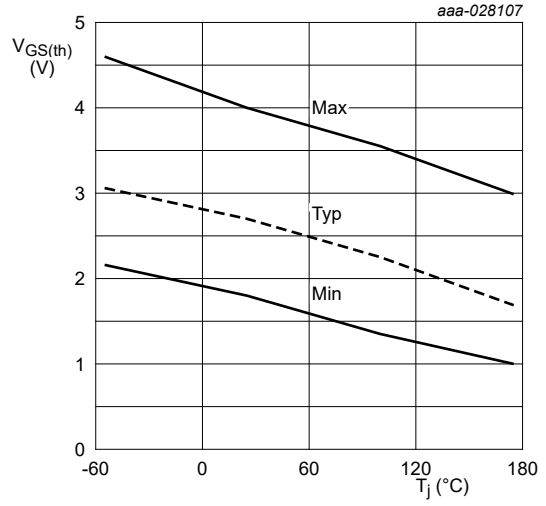


Fig. 11. Gate-source threshold voltage as a function of junction temperature

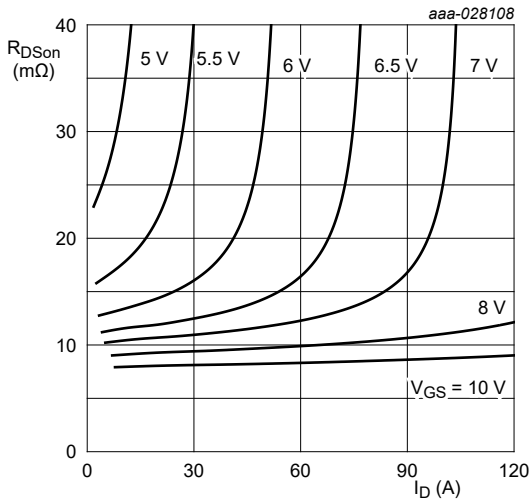
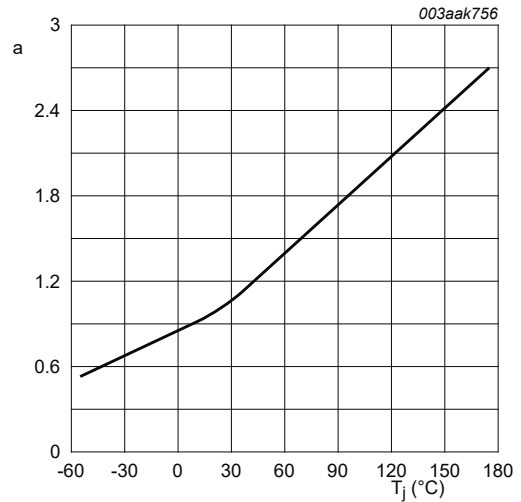
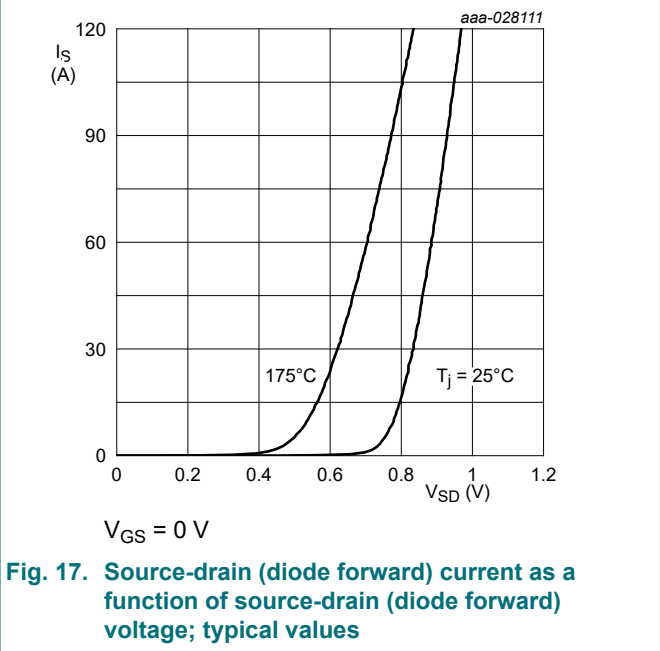
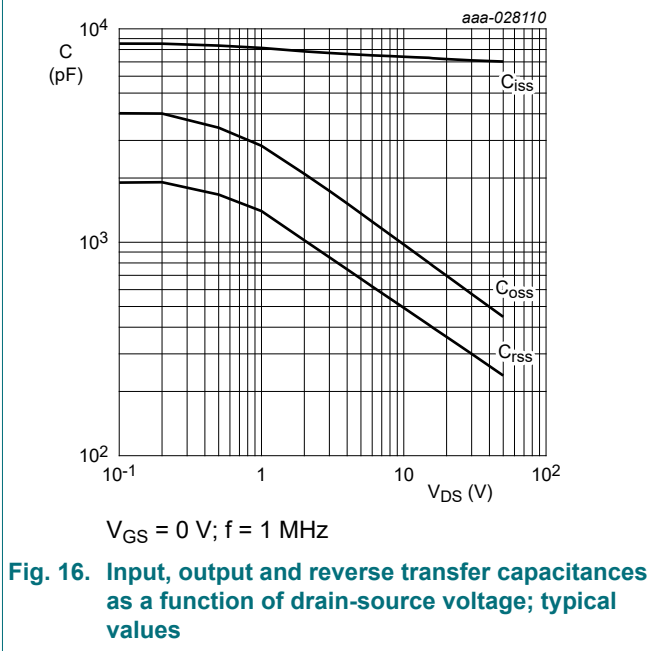
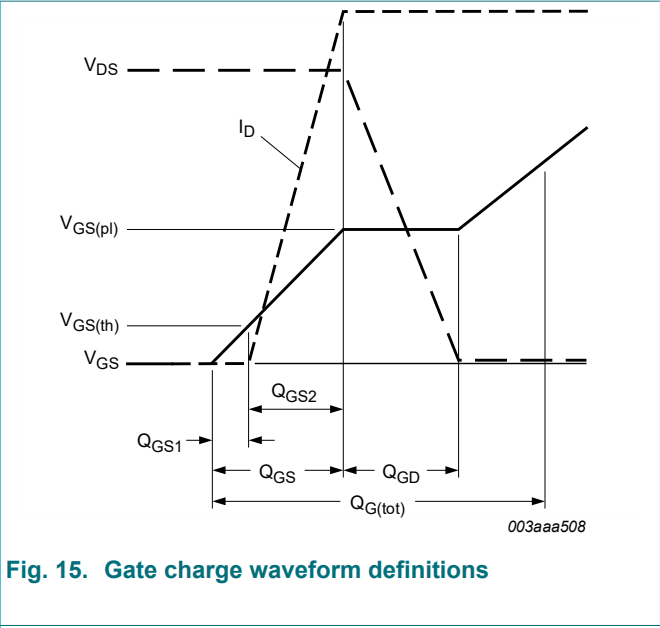
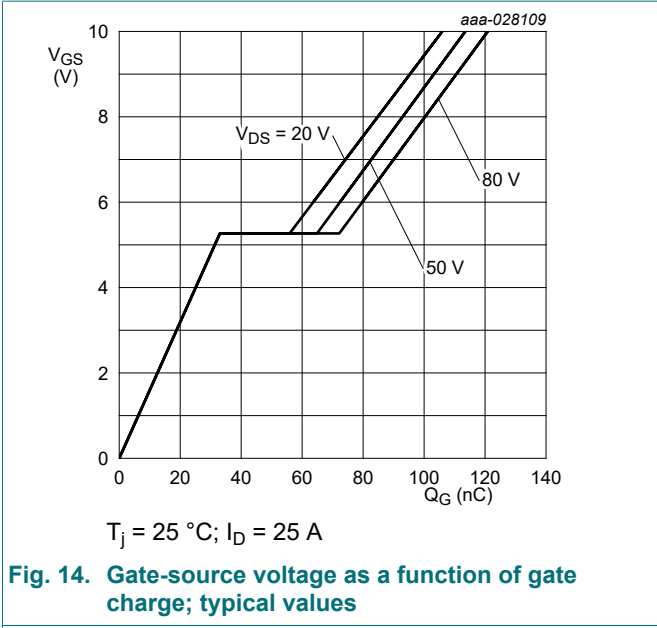


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon}(25\text{ °C})}$$

Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature



11. Package outline

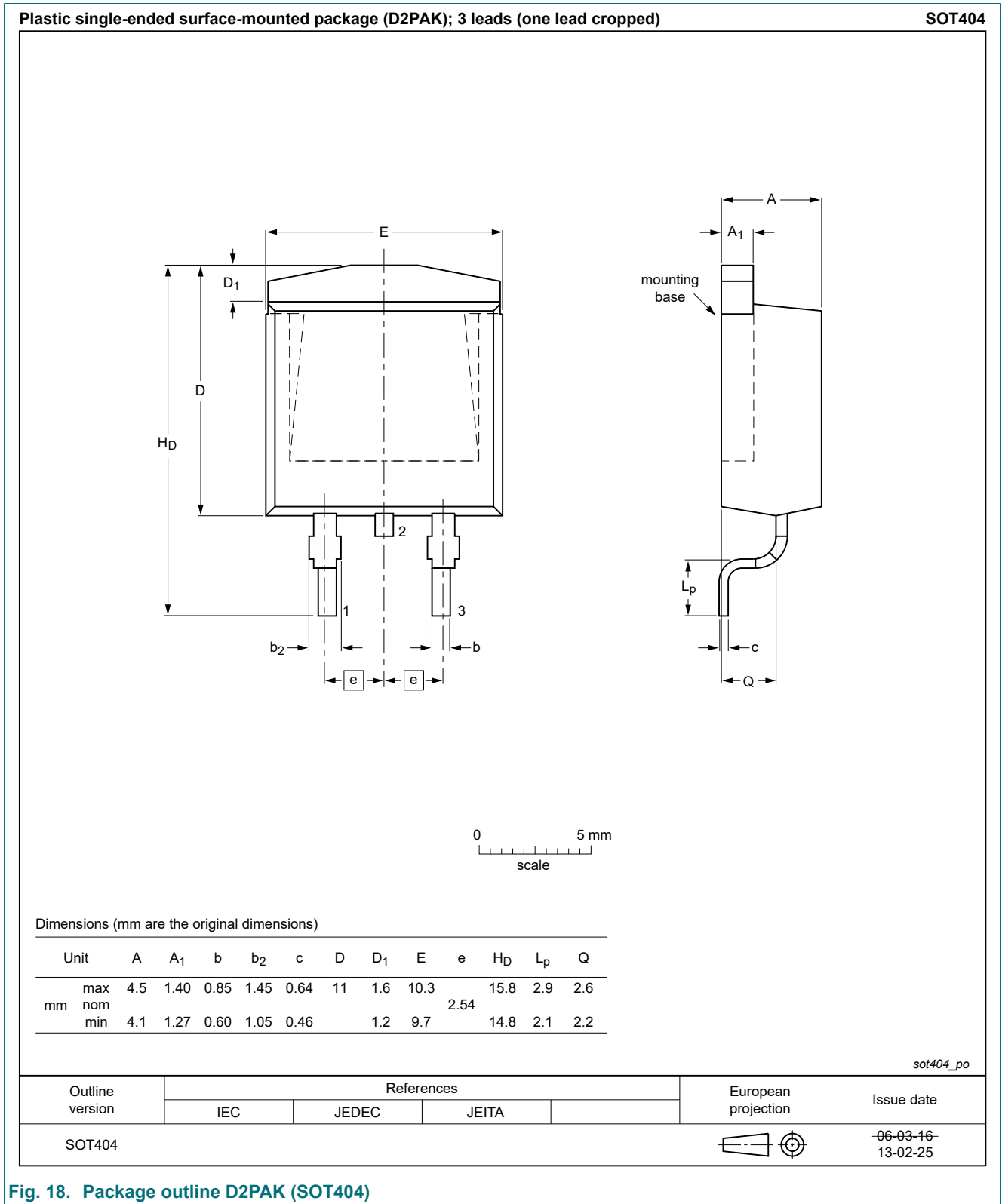


Fig. 18. Package outline D2PAK (SOT404)

12. Soldering

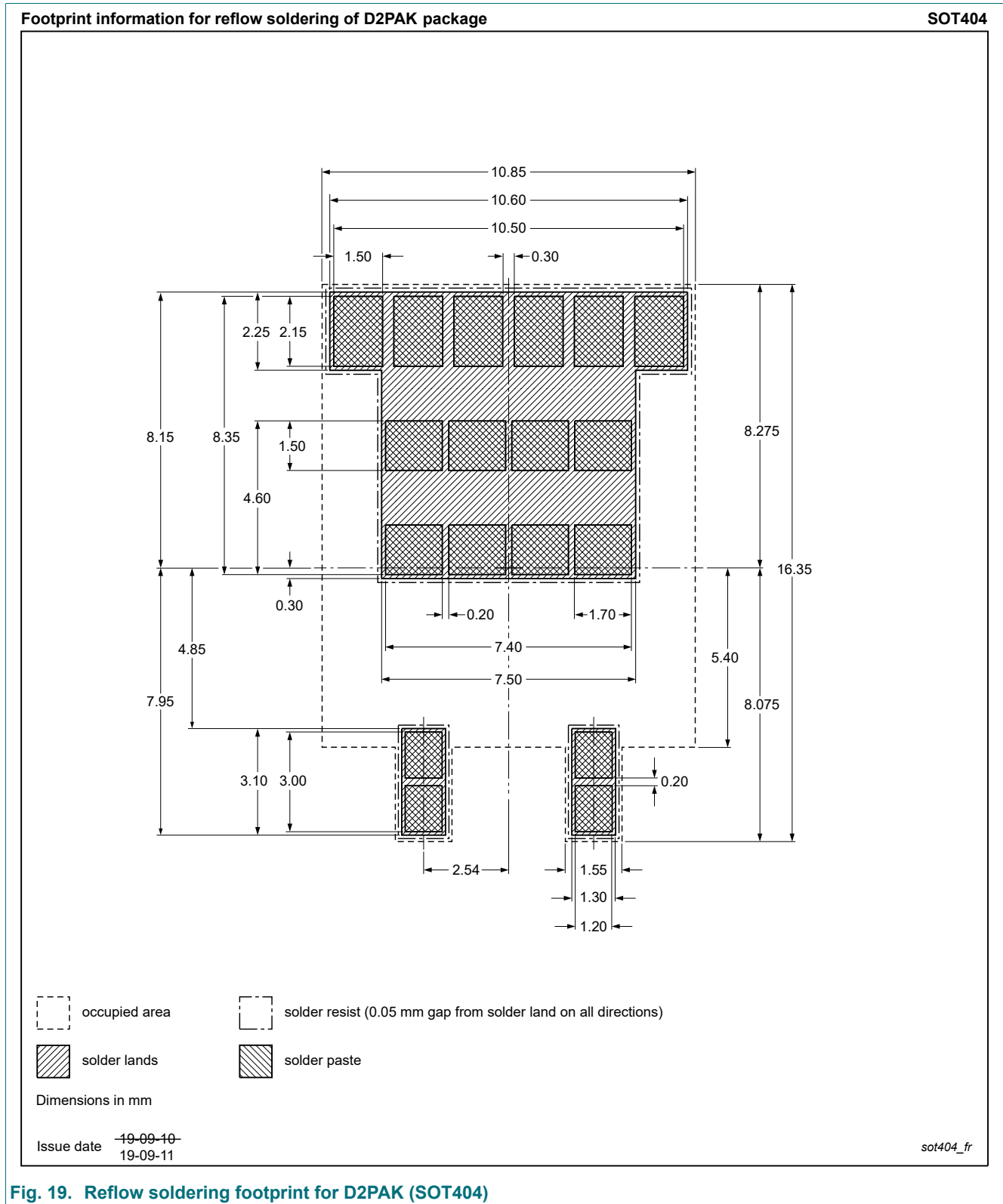


Fig. 19. Reflow soldering footprint for D2PAK (SOT404)

13. Legal information

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Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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