PSMN9R8-100YSF

NextPower 100 V, 10.2 mOhm N-channel MOSFET in LFPAK56 package

20 June 2023 Product data sheet

1. General description

NextPower 100 V, standard level gate drive MOSFET. Qualified to 175 °C and recommended for industrial and consumer applications.

2. Features and benefits

- Low Q_{rr} for higher efficiency and lower spiking
- Low Q_G × R_{DSon} FOM for high efficiency switching applications
- Strong avalanche energy rating (E_{AS})
- Avalanche rated and 100% tested
- Ha-free and RoHS compliant LFPAK56 package
- Wave-solderable LFPAK56 package

3. Applications

- Synchronous rectifier in AC-DC and DC-DC
- Primary side switch in 48 V DC-DC
- BLDC motor control
- USB-PD and mobile fast-charge adapters
- Flyback and resonant topologies

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	-	100	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2		-	-	80	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	147	W
T_j	junction temperature			-55	-	175	°C
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 20 A; T_j = 25 °C; Fig. 12		-	8.3	10.2	mΩ
		V_{GS} = 10 V; I_D = 20 A; T_j = 100 °C; Fig. 13		-	13	16.2	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	I_D = 20 A; V_{DS} = 50 V; V_{GS} = 10 V; T_j = 25 °C; Fig. 14; Fig. 15		1.8	6	13.8	nC
$Q_{G(tot)}$	total gate charge			16.8	34	50.4	nC
Avalanche ruggedness							
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 30.4 A; V_{sup} ≤ 100 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped; t_p = 56 µs; Fig. 4	[1]	-	-	111	mJ

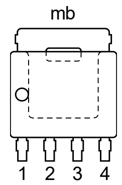
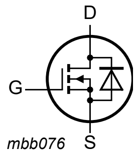
nexperia

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Source-drain diode							
Q_r	recovered charge	I_S = 20 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 50 V; T_j = 25 °C; Fig. 18		-	22	-	nC

[1] Protected by 100% test

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LFPAK56; Power-SO8 (SOT669)	
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN9R8-100YSF	LFPAK56; Power-SO8	plastic, single-ended surface-mounted package; 4 terminals	SOT669

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN9R8-100YSF	9F8S10Y

8. Limiting values

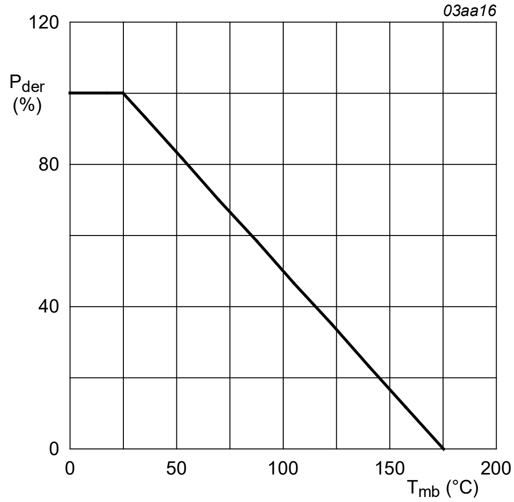
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).Tj = 25 °C unless otherwise stated.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	100	V
V_{DGR}	drain-gate voltage	25 °C ≤ T_j ≤ 175 °C; R_{GS} = 20 kΩ		-	100	V
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	147	W
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2		-	80	A
		V_{GS} = 10 V; T_{mb} = 100 °C; Fig. 2		-	57	A
I_{DM}	peak drain current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C; Fig. 3		-	320	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C

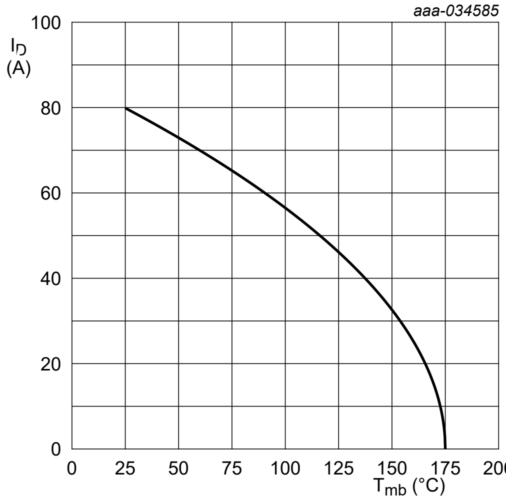
Symbol	Parameter	Conditions		Min	Max	Unit
$T_{sld(M)}$	peak soldering temperature			-	260	°C
Source-drain diode						
I_S	source current	T_{mb} = 25 °C		-	80	A
I_{SM}	peak source current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C		-	320	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 30.4 A; V_{sup} ≤ 100 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped; t_p = 56 µs; Fig. 4	[1]	-	111	mJ
I_{AS}	non-repetitive avalanche current	V_{sup} ≤ 100 V; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; R_{GS} = 50 Ω; Fig. 4	[1]	-	30.4	A

[1] Protected by 100% test



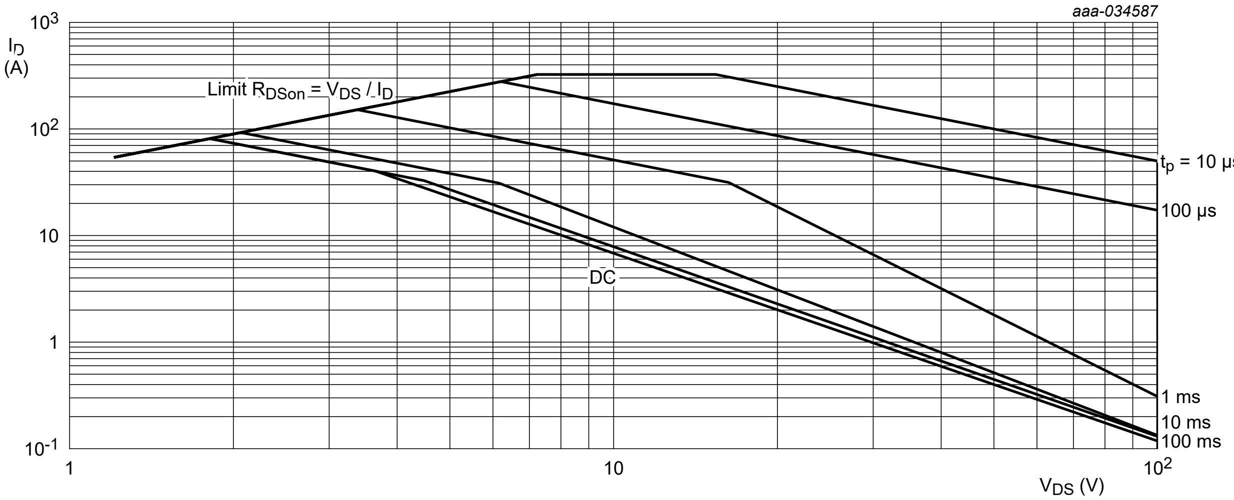
$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig. 1. Normalized total power dissipation as a function of mounting base temperature



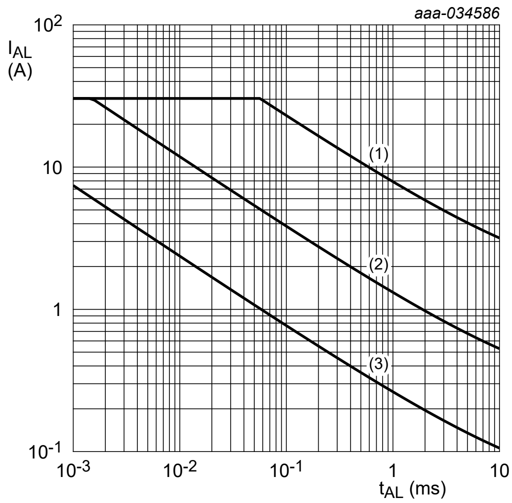
V_{GS} ≥ 10 V
80 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

Fig. 2. Continuous drain current as a function of mounting base temperature



T_{mb} = 25 °C; I_{DM} is a single pulse

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



(1) $T_{j\,(init)}$ = 25 °C; (2) $T_{j\,(init)}$ = 150 °C; (3) Repetitive Avalanche

Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5		-	0.92	1.02	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 6		-	42	-	K/W
		Fig. 7		-	85	-	K/W

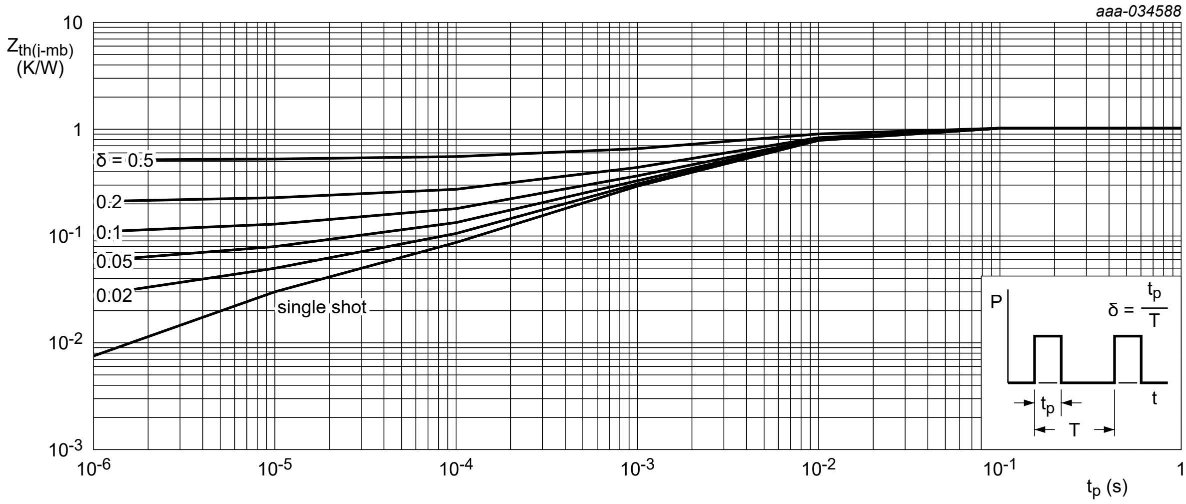
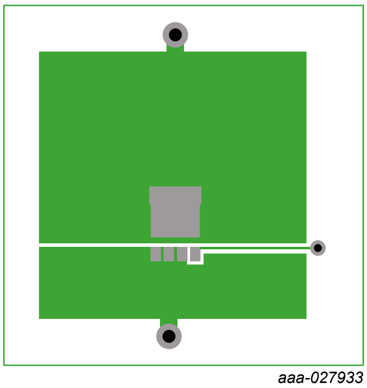
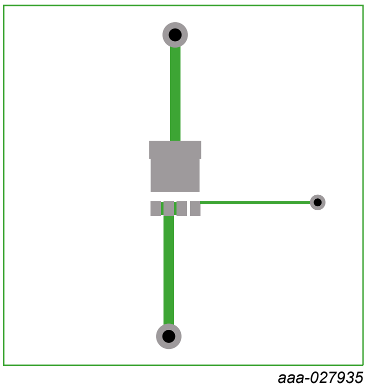


Fig. 5. **Transient thermal impedance from junction to mounting base as a function of pulse duration**



Copper area 25.4 mm square; 70 μm thick on FR4 board

Fig. 6. **PCB layout for thermal resistance from junction to ambient**



70 μm thick copper on FR4 board

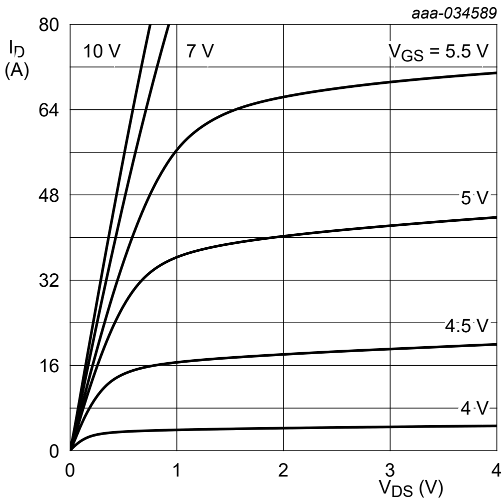
Fig. 7. **PCB layout with minimum footprint for thermal resistance from junction to ambient**

10. Characteristics

Table 7. Characteristics

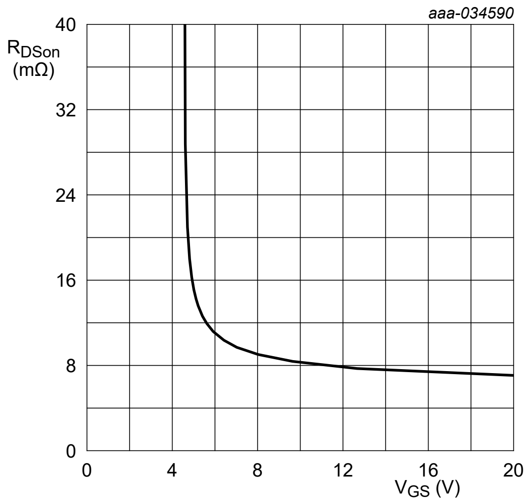
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 μA; V_{GS} = 0 V; T_j = 25 °C		100	-	-	V
		I_D = 250 μA; V_{GS} = 0 V; T_j = -55 °C		90	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS}=V_{GS}; T_j = 25 °C; Fig. 11		2	3	4	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = 175 °C		-	1.8	-	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = -55 °C		-	3.4	-	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	25 °C ≤ T_j ≤ 150 °C		-	-7.4	-	mV/K
I_{DSS}	drain leakage current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C		-	0.01	1	μA
		V_{DS} = 100 V; V_{GS} = 0 V; T_j = 125 °C		-	5	100	μA
I_{GSS}	gate leakage current	V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
		V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 20 A; T_j = 25 °C; Fig. 12		-	8.3	10.2	mΩ
		V_{GS} = 7 V; I_D = 20 A; T_j = 25 °C; Fig. 12		-	9.7	15	mΩ
		V_{GS} = 10 V; I_D = 20 A; T_j = 100 °C; Fig. 13		-	13	16.2	mΩ
		V_{GS} = 10 V; I_D = 20 A; T_j = 175 °C; Fig. 13		-	18.4	23.2	mΩ
R_G	gate resistance	f = 1 MHz; T_j = 25 °C		0.8	1.6	3.2	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 20 A; V_{DS} = 50 V; V_{GS} = 10 V; T_j = 25 °C; Fig. 14; Fig. 15		16.8	34	50.4	nC
		I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V; T_j = 25 °C		-	17.5	-	nC
Q_{GS}	gate-source charge	I_D = 20 A; V_{DS} = 50 V; V_{GS} = 10 V; T_j = 25 °C; Fig. 14; Fig. 15		6.2	10.3	14.4	nC
$Q_{GS(th)}$	pre-threshold gate-source charge			-	6.8	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge			-	3.5	-	nC
Q_{GD}	gate-drain charge			1.8	6	13.8	nC
$V_{GS(pl)}$	gate-source plateau voltage	I_D = 20 A; V_{DS} = 50 V; T_j = 25 °C; Fig. 14; Fig. 15		-	4.6	-	V
C_{iss}	input capacitance	V_{DS} = 50 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; Fig. 16		1450	2417	3384	pF
C_{oss}	output capacitance			347	579	926	pF
C_{rss}	reverse transfer capacitance			2	20	52	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 50 V; R_L = 2.5 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 5 Ω; T_j = 25 °C		-	10	-	ns
t_r	rise time			-	9	-	ns
$t_{d(off)}$	turn-off delay time			-	22	-	ns
t_f	fall time			-	12	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 20 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 17		-	0.83	1	V
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 50 V; T_j = 25 °C; Fig. 18		-	31	-	ns
Q_r	recovered charge			-	22	-	nC



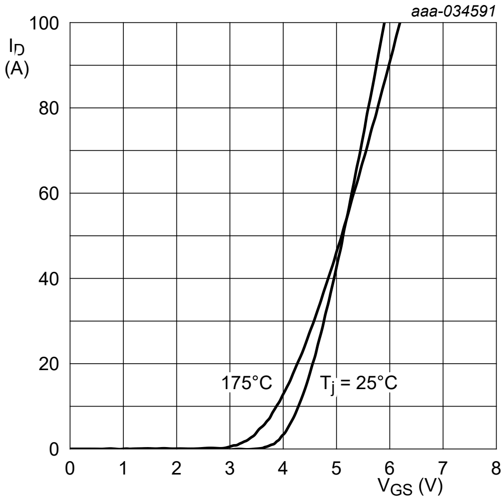
T_j = 25 °C

Fig. 8. Output characteristics; drain current as a function of drain-source voltage; typical values



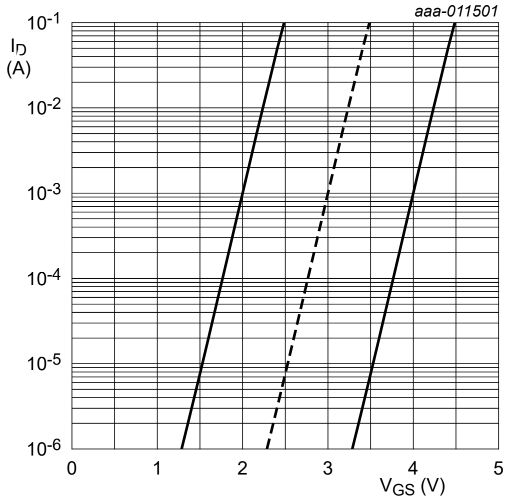
T_j = 25 °C; I_D = 20 A

Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values



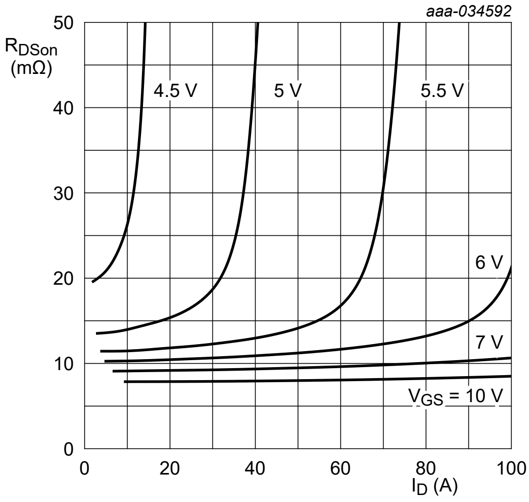
V_{DS} = 8 V

Fig. 10. Transfer characteristics; drain current as a function of gate-source voltage; typical values



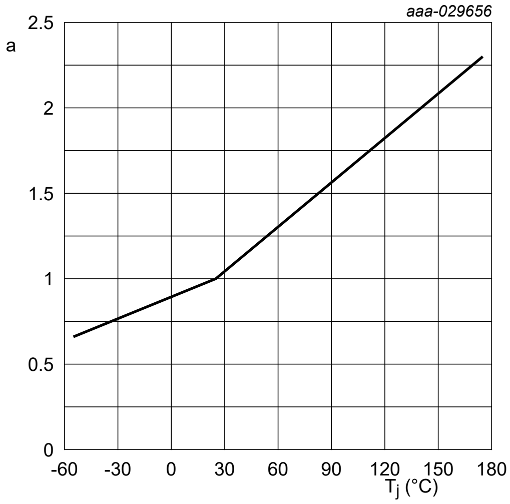
T_j = 25 °C; V_{DS} = 5 V

Fig. 11. Sub-threshold drain current as a function of gate-source voltage



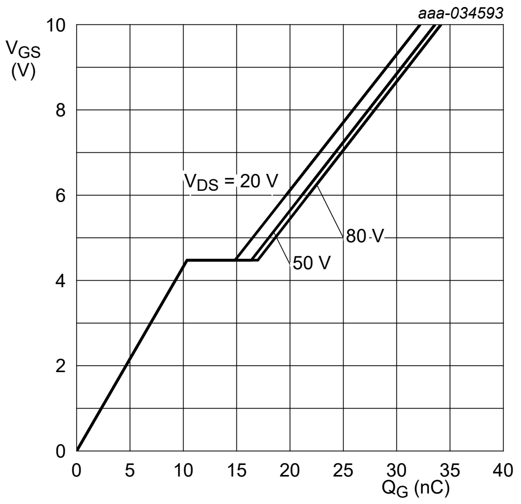
T_j = 25 °C

Fig. 12. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon\ (25°C)}}$$

Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature



T_j = 25 °C; I_D = 20 A

Fig. 14. Gate-source voltage as a function of gate charge; typical values

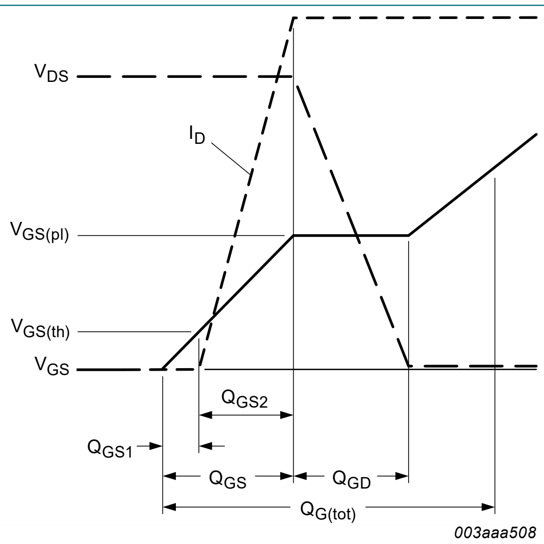
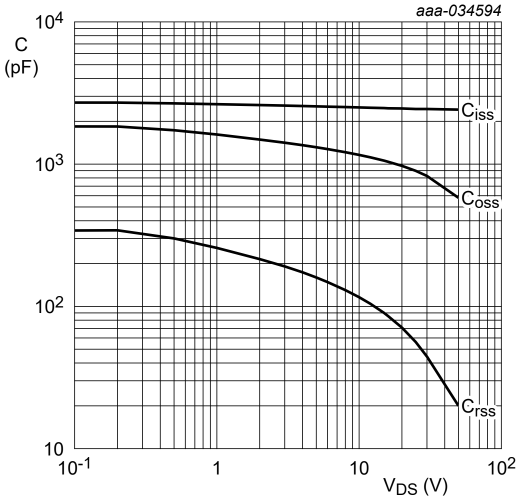
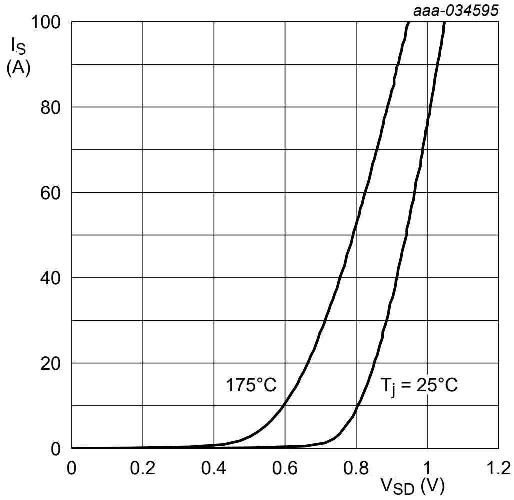


Fig. 15. Gate charge waveform definitions



V_{GS} = 0 V; f = 1 MHz

Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



V_{GS} = 0 V

Fig. 17. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

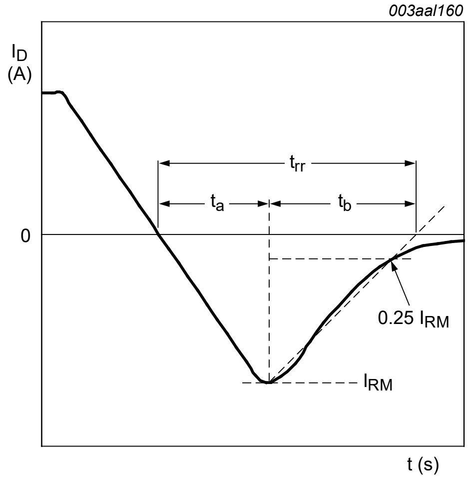
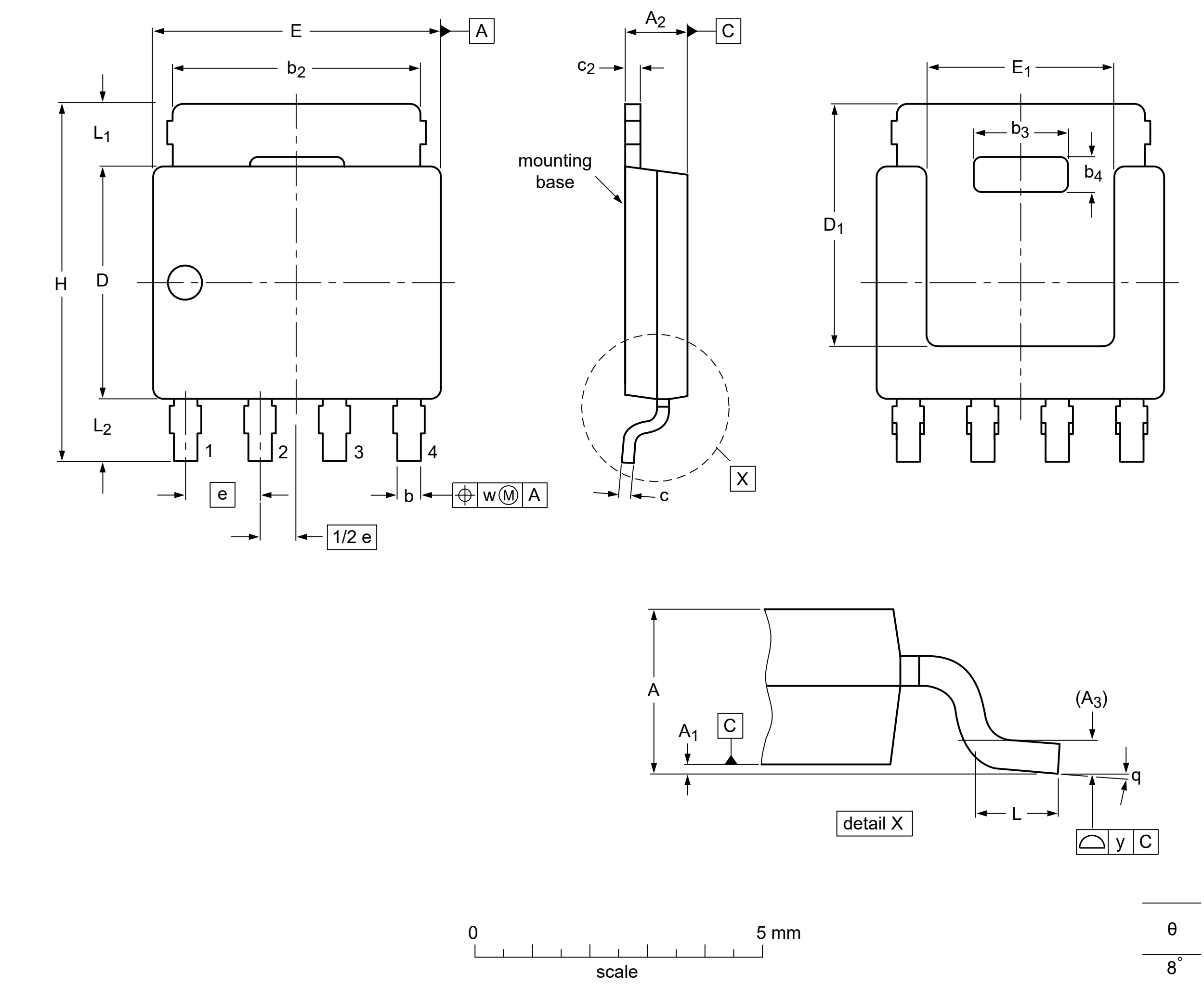


Fig. 18. Reverse recovery timing definition

11. Package outline

Plastic single-ended surface-mounted package (LFPAK56; Power-SO8); 4 leads **SOT669**



Dimensions (mm are the original dimensions)

Unit[1]		A	A_1	A_2	A_3	b	b_2	b_3	b_4	c	c_2	D[1]	D_1[1]	E[1]	E_1[1]	e	H	L	L_1	L_2	w	y	θ
mm	max	1.20	0.15	1.10		0.50	4.41	2.2	0.9	0.25	0.30	4.10	4.20	5.0	3.3		6.2	0.85	1.3	1.3			8°
	nom				0.25											1.27					0.25	0.1	
	min	1.01	0.00	0.95		0.35	3.62	2.0	0.7	0.19	0.24	3.80		4.8	3.1		5.8	0.40	0.8	0.8			0°

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

sot669_po

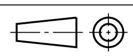
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT669		MO-235				~~11-03-25~~ 13-02-27

Fig. 19. Package outline LFPAK56; Power-SO8 (SOT669)

12. Soldering

Footprint information for reflow soldering **SOT669**

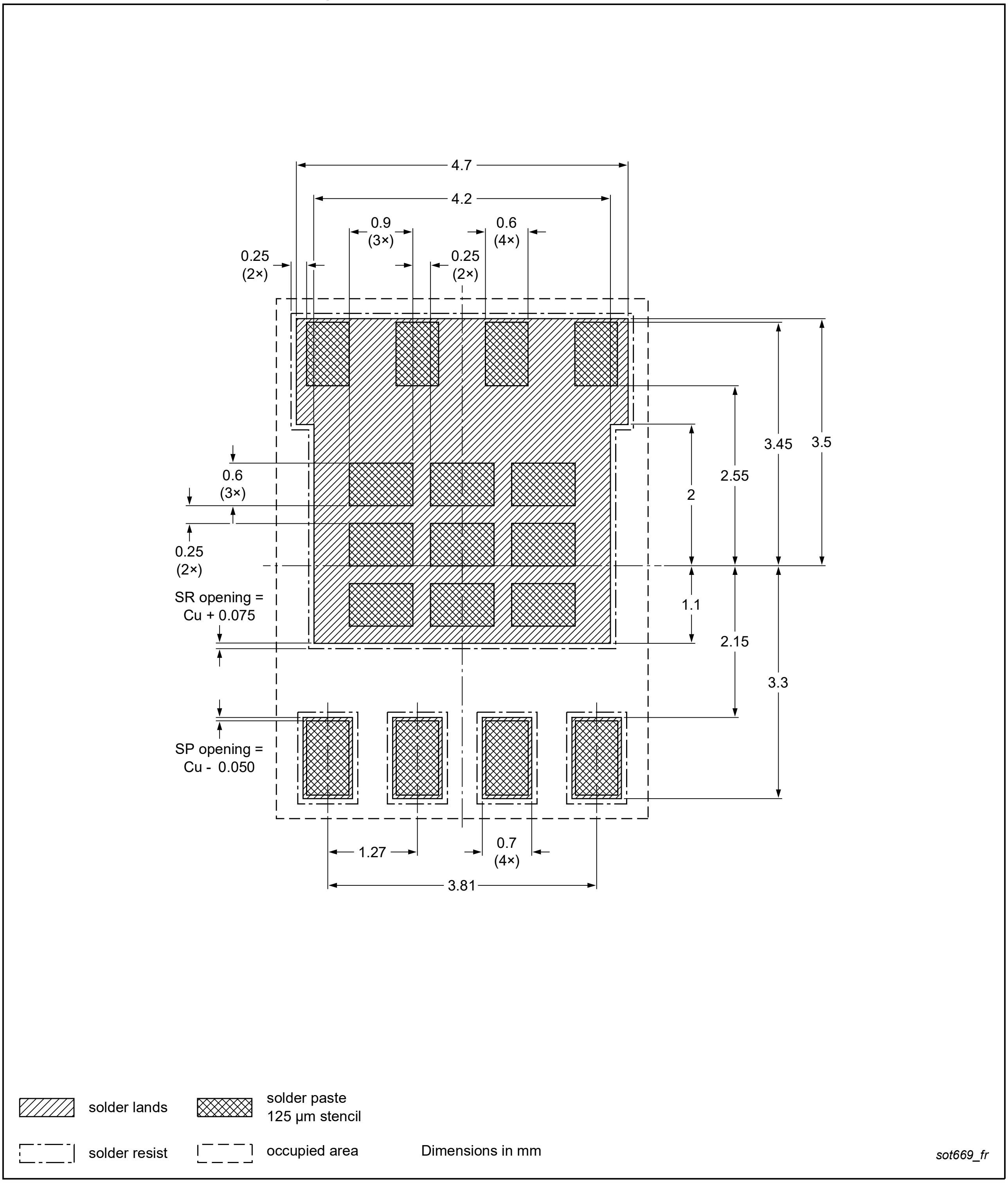


Fig. 20. Reflow soldering footprint for LFPAK56; Power-SO8 (SOT669)

Wave soldering footprint information for LFPAK56 package **SOT669**

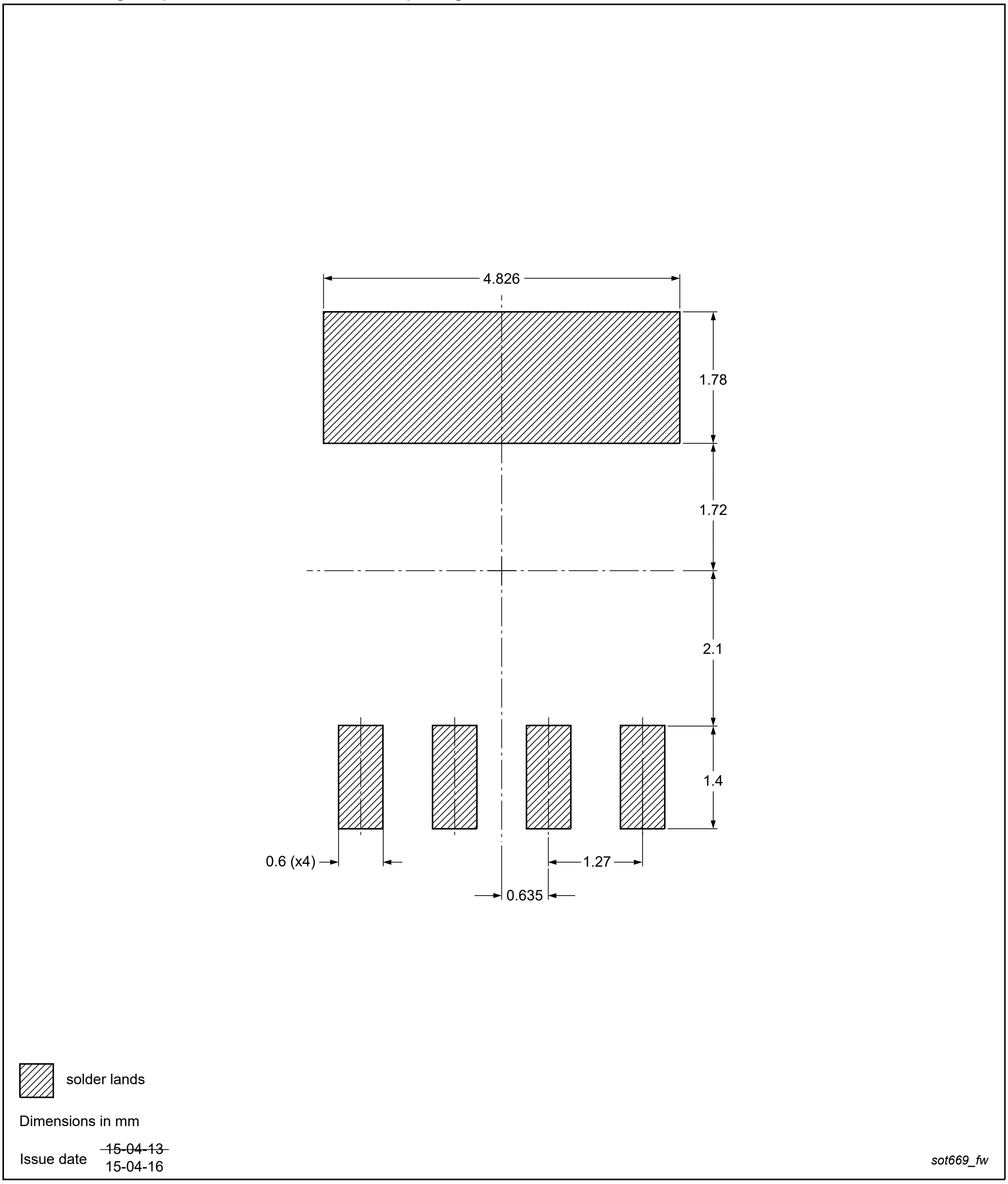


Fig. 21. Wave soldering footprint for LFPAK56; Power-SO8 (SOT669)

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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