
# PSMNR82-30YLE

## N-channel 30 V, 0.87 mOhm, ASFET for hotswap with enhanced SOA in LFPAK56

13 October 2022 **Product data sheet**

## 1. General description

N-channel enhancement mode ASFET for hotswap with enhanced SOA in LFPAK56 package optimized for low $R_{DSon}$ and strong safe operating area, optimized for hot-swap, inrush and linear-mode applications.

## 2. Features and benefits

- Fully optimized Safe Operating Area (SOA) for superior linear mode operation
- Optimized for low $R_{DSon}$ / low $I^2R$ conduction losses
- LFPAK56E package for applications that demand the highest performance and reliability in a 30 $mm^2$ footprint
- Low leakage < 1 µA at 25 °C
- Copper-clip for low parasitic inductance and resistance
- High reliability LFPAK package, qualified to 175 °C

## 3. Applications

- Hot swap in 12 V-20 V applications
- e-Fuse
- DC switch
- Load switch
- Battery protection

## 4. Quick reference data

**Table 1. Quick reference data**

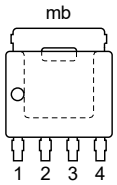
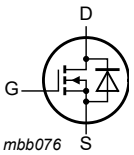
| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | 25 °C ≤ $T_j$ ≤ 175 °C | | - | - | 30 | V |
| $I_D$ | drain current | $V_{GS}$ = 10 V; $T_{mb}$ = 25 °C; Fig. 2 | [1] | - | - | 330 | A |
| $P_{tot}$ | total power dissipation | $T_{mb}$ = 25 °C; Fig. 1 | | - | - | 268 | W |
| $T_j$ | junction temperature | | | -55 | - | 175 | °C |
| **Static characteristics** | | | | | | | |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 25 °C; Fig. 10 | | - | 0.73 | 0.87 | mΩ |
| | | $V_{GS}$ = 7 V; $I_D$ = 25 A; $T_j$ = 25 °C; Fig. 10 | | - | 0.87 | 1.25 | mΩ |
| **Dynamic characteristics** | | | | | | | |
| $Q_{GD}$ | gate-drain charge | $I_D$ = 25 A; $V_{DS}$ = 15 V; $V_{GS}$ = 4.5 V; $T_j$ = 25 °C; Fig. 12; Fig. 13 | | 1.8 | 10 | 20 | nC |
| $Q_{G(tot)}$ | total gate charge | | | 18 | 41 | 68 | nC |

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Source-drain diode** | | | | | | | |
| S | softness factor | $I_S$ = 25 A; $dI_S/dt$ = -100 A/µs; $V_{GS}$ = 0 V; $V_{DS}$ = 15 V; $T_j$ = 25 °C; Fig. 16 | | - | 1.03 | - | |

[1] 330 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

## 5. Pinning information

**Table 2. Pinning information**

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|---|---|---|---|---|
| 1 | S | source |  **LFPAK56; Power-SO8 (SOT669)** |  |
| 2 | S | source | | |
| 3 | S | source | | |
| 4 | G | gate | | |
| mb | D | mounting base; connected to drain | | |

## 6. Ordering information

**Table 3. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| PSMNR82-30YLE | LFPAK56; Power-SO8 | plastic, single-ended surface-mounted package; 4 terminals | SOT669 |

## 7. Marking

**Table 4. Marking codes**

| Type number | Marking code |
|---|---|
| PSMNR82-30YLE | E82L30Y |

## 8. Limiting values

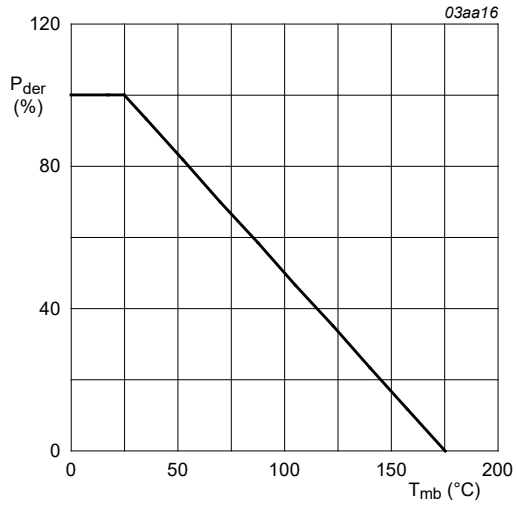
**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Tj = 25 °C unless otherwise stated.*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | 25 °C ≤ $T_j$ ≤ 175 °C | | - | 30 | V |
| $V_{DGR}$ | drain-gate voltage | 25 °C ≤ $T_j$ ≤ 175 °C; $R_{GS}$ = 20 kΩ | | - | 30 | V |
| $V_{GS}$ | gate-source voltage | | | -20 | 20 | V |
| $P_{tot}$ | total power dissipation | $T_{mb}$ = 25 °C; Fig. 1 | | - | 268 | W |
| $I_D$ | drain current | $V_{GS}$ = 10 V; $T_{mb}$ = 25 °C; Fig. 2 | [1] | - | 330 | A |
| | | $V_{GS}$ = 10 V; $T_{mb}$ = 100 °C; Fig. 2 | | - | 295 | A |
| $I_{DM}$ | peak drain current | pulsed; $t_p$ ≤ 10 µs; $T_{mb}$ = 25 °C; Fig. 3 | | - | 1667 | A |
| $T_{stg}$ | storage temperature | | | -55 | 175 | °C |
| $T_j$ | junction temperature | | | -55 | 175 | °C |

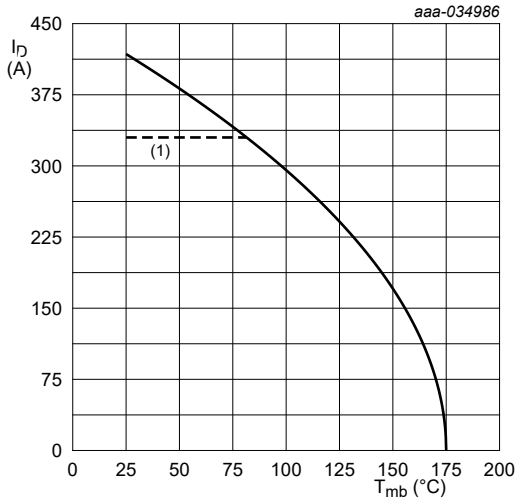
| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $T_{sld(M)}$ | peak soldering temperature | | | - | 260 | °C |
| **Source-drain diode** | | | | | | |
| $I_S$ | source current | $T_{mb}$ = 25 °C | | - | 268 | A |
| $I_{SM}$ | peak source current | pulsed; $t_p \leq$ 10 µs; $T_{mb}$ = 25 °C | | - | 1667 | A |
| **Avalanche ruggedness** | | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $I_D$ = 25 A; $V_{sup} \leq$ 30 V; $R_{GS}$ = 50 Ω; $V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; unclamped; $t_p$ = 5.5 ms | [2] | - | 2.7 | J |
| $I_{AS}$ | non-repetitive avalanche current | $V_{sup} \leq$ 30 V; $V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; $R_{GS}$ = 50 Ω | [2] | - | 190 | A |

[1] 330 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
[2] Protected by 100% test.



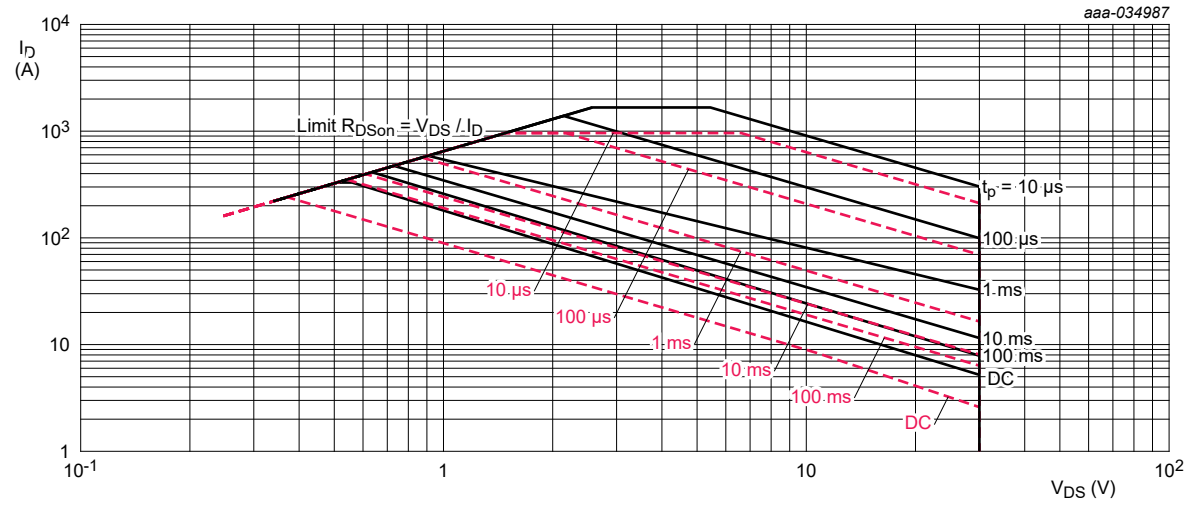

$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

**Fig. 1. Normalized total power dissipation as a function of mounting base temperature**




$V_{GS} \geq 10$ V
(1) 330 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

**Fig. 2. Continuous drain current as a function of mounting base temperature**




$T_{mb}$ = 25 °C (solid black line);$T_{mb}$ = 125 °C (red dashed line); $I_{DM}$ is a single pulse

**Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**

# 9. Thermal characteristics

**Table 6. Thermal characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | Fig. 4 | | - | 0.42 | 0.56 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | Fig. 5 | | - | 42 | - | K/W |
| | | Fig. 6 | | - | 85 | - | K/W |

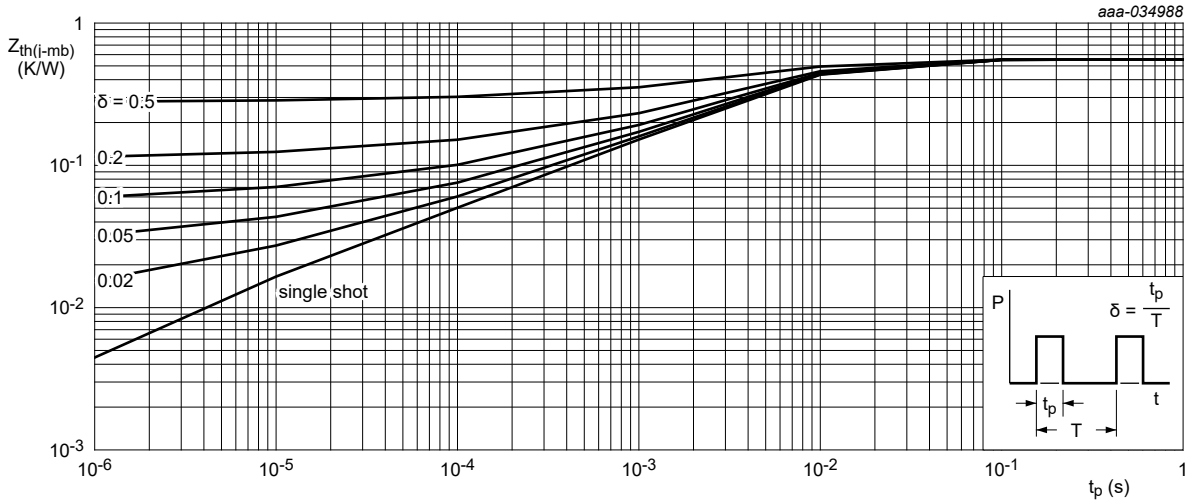
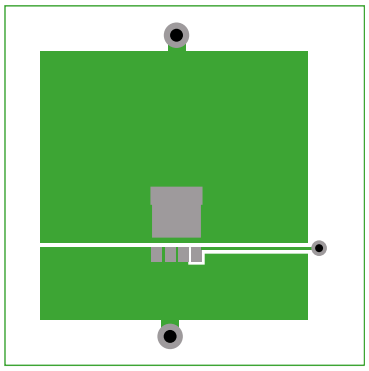
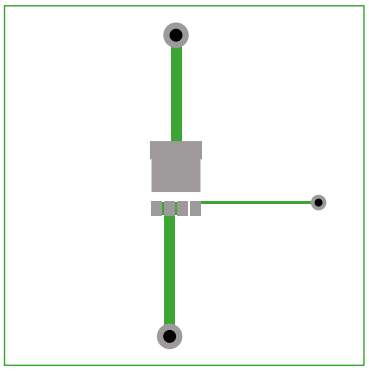



**Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration**




Copper area 25.4 mm square; 70 µm thick on FR4 board

**Fig. 5. PCB layout for thermal resistance from junction to ambient**




70 µm thick copper on FR4 board

**Fig. 6. PCB layout with minimum footprint for thermal resistance from junction to ambient**

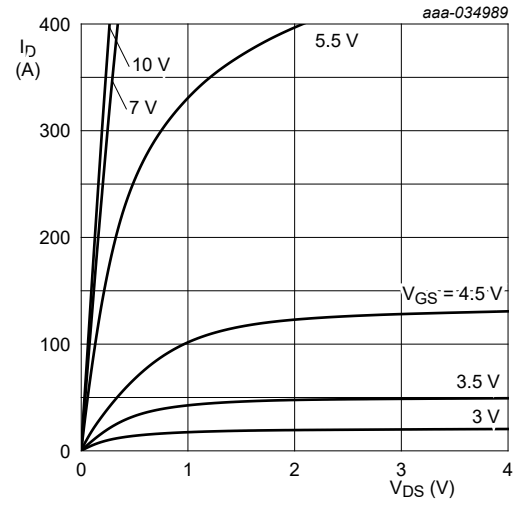
# 10. Characteristics

**Table 7. Characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D$ = 250 µA; $V_{GS}$ = 0 V; $T_j$ = 25 °C | | 30 | - | - | V |
| | | $I_D$ = 250 µA; $V_{GS}$ = 0 V; $T_j$ = -55 °C | | 27 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D$ = 2 mA; $V_{DS}$=$V_{GS}$; $T_j$ = 25 °C | | 1.2 | 1.79 | 2.2 | V |
| $\Delta V_{GS(th)}/\Delta T$ | gate-source threshold voltage variation with temperature | 25 °C ≤ $T_j$ ≤ 150 °C | | - | -3.7 | - | mV/K |
| $I_{DSS}$ | drain leakage current | $V_{DS}$ = 24 V; $V_{GS}$ = 0 V; $T_j$ = 25 °C | | - | - | 1 | µA |
| | | $V_{DS}$ = 24 V; $V_{GS}$ = 0 V; $T_j$ = 125 °C | | - | 7.2 | - | µA |
| $I_{GSS}$ | gate leakage current | $V_{GS}$ = 16 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C | | - | - | 100 | nA |
| | | $V_{GS}$ = -16 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C | | - | - | 100 | nA |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 25 °C; Fig. 10 | | - | 0.73 | 0.87 | mΩ |
| | | $V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 150 °C; Fig. 11 | | - | - | 1.6 | mΩ |
| | | $V_{GS}$ = 7 V; $I_D$ = 25 A; $T_j$ = 25 °C; Fig. 10 | | - | 0.87 | 1.25 | mΩ |
| | | $V_{GS}$ = 7 V; $I_D$ = 25 A; $T_j$ = 150 °C; Fig. 11 | | - | - | 2.3 | mΩ |
| $R_G$ | gate resistance | f = 1 MHz; $T_j$ = 25 °C | | 1.3 | 3.2 | 8 | Ω |
| **Dynamic characteristics** | | | | | | | |
| $Q_{G(tot)}$ | total gate charge | $I_D$ = 25 A; $V_{DS}$ = 15 V; $V_{GS}$ = 4.5 V; $T_j$ = 25 °C; Fig. 12; Fig. 13 | | 18 | 41 | 68 | nC |
| | | $I_D$ = 25 A; $V_{DS}$ = 15 V; $V_{GS}$ = 10 V; $T_j$ = 25 °C; Fig. 12; Fig. 13 | | 41 | 90 | 149 | nC |
| | | $I_D$ = 0 A; $V_{DS}$ = 0 V; $V_{GS}$ = 10 V; $T_j$ = 25 °C | | - | 46 | - | nC |

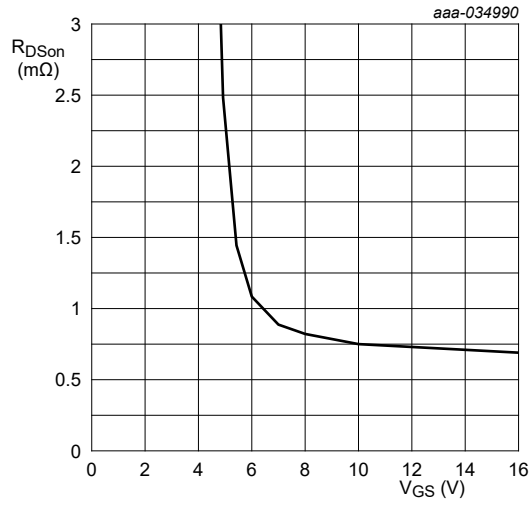
| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $Q_{GS}$ | gate-source charge | $I_D$ = 25 A; $V_{DS}$ = 15 V; $V_{GS}$ = 4.5 V; $T_j$ = 25 °C; Fig. 12; Fig. 13 | | 5 | 19 | 36 | nC |
| $Q_{GS(th)}$ | pre-threshold gate-source charge | | | 2.7 | 10 | 19 | nC |
| $Q_{GS(th-pl)}$ | post-threshold gate-source charge | | | 2.4 | 9 | 17 | nC |
| $Q_{GD}$ | gate-drain charge | | | 1.8 | 10 | 20 | nC |
| $V_{GS(pl)}$ | gate-source plateau voltage | $I_D$ = 25 A; $V_{DS}$ = 15 V; $T_j$ = 25 °C; Fig. 12; Fig. 13 | | - | 3.2 | - | V |
| $C_{iss}$ | input capacitance | $V_{DS}$ = 15 V; $V_{GS}$ = 0 V; f = 1 MHz; $T_j$ = 25 °C; Fig. 14 | | 4052 | 6754 | 10131 | pF |
| $C_{oss}$ | output capacitance | | | 1234 | 2056 | 3084 | pF |
| $C_{rss}$ | reverse transfer capacitance | | | 93 | 343 | 823 | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DS}$ = 15 V; $R_L$ = 0.6 Ω; $V_{GS}$ = 4.5 V; $R_{G(ext)}$ = 5 Ω; $T_j$ = 25 °C | | - | 49 | - | ns |
| $t_r$ | rise time | | | - | 95 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | | - | 37 | - | ns |
| $t_f$ | fall time | | | - | 44 | - | ns |
| $Q_{oss}$ | output charge | $V_{GS}$ = 0 V; $V_{DS}$ = 15 V; f = 1 MHz; $T_j$ = 25 °C | | - | 49 | - | nC |
| **Source-drain diode** | | | | | | | |
| $V_{SD}$ | source-drain voltage | $I_S$ = 25 A; $V_{GS}$ = 0 V; $T_j$ = 25 °C; Fig. 15 | | - | 0.78 | 1 | V |
| $t_{rr}$ | reverse recovery time | $I_S$ = 25 A; $dI_S/dt$ = -100 A/µs; $V_{GS}$ = 0 V; $V_{DS}$ = 15 V; $T_j$ = 25 °C; Fig. 16 | | - | 35 | - | ns |
| $Q_r$ | recovered charge | | [1] | - | 28 | - | nC |
| $t_a$ | reverse recovery rise time | | | - | 17.3 | - | ns |
| $t_b$ | reverse recovery fall time | | | - | 17.9 | - | ns |
| S | softness factor | | | - | 1.03 | - | |

[1] includes capacitive recovery



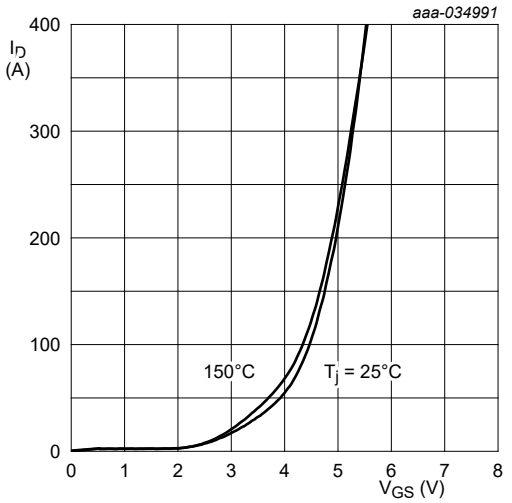

$T_j$ = 25 °C

**Fig. 7. Output characteristics; drain current as a function of drain-source voltage; typical values**



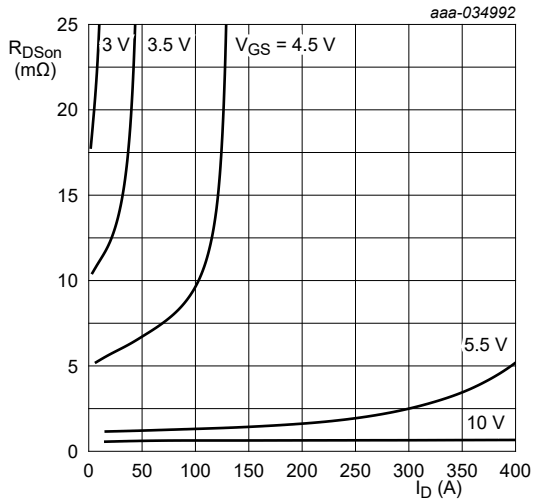

$T_j$ = 25 °C; $I_D$ = 25 A

**Fig. 8. Drain-source on-state resistance as a function of gate-source voltage; typical values**



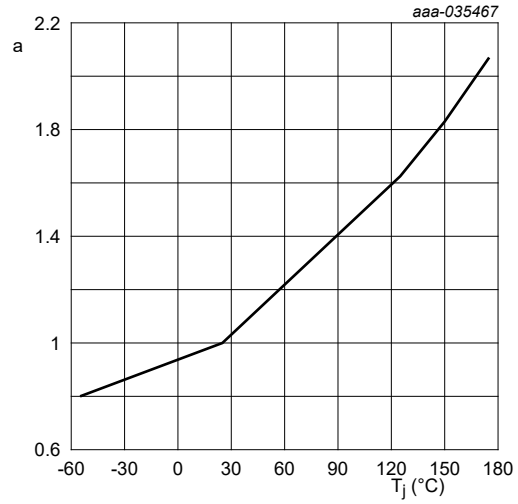

$V_{DS}$ = 8 V

**Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values**



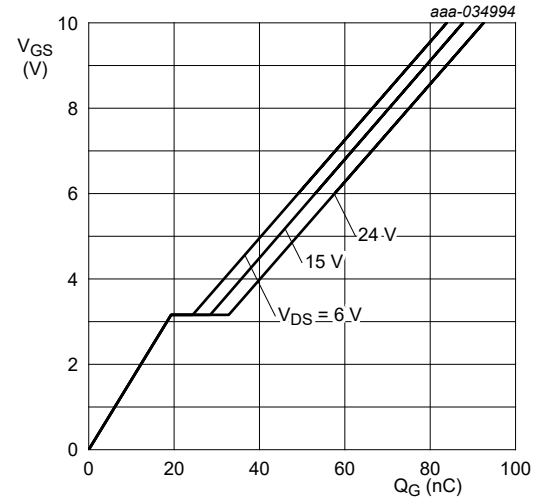

$T_j$ = 25 °C

**Fig. 10. Drain-source on-state resistance as a function of drain current; typical values**




$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

**Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature**




$T_j$ = 25 °C; $I_D$ = 25 A

**Fig. 12. Gate-source voltage as a function of gate charge; typical values**

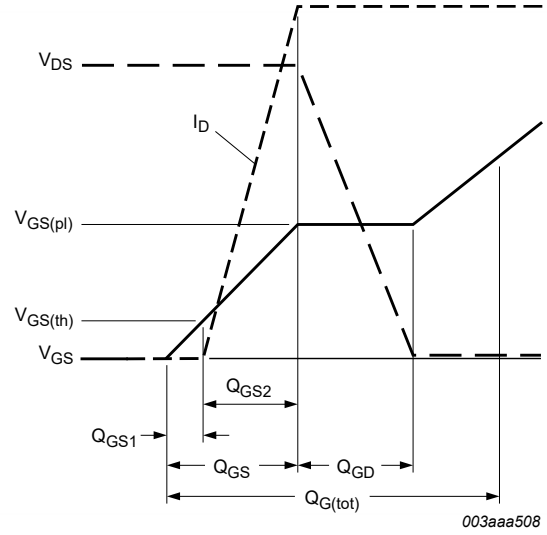
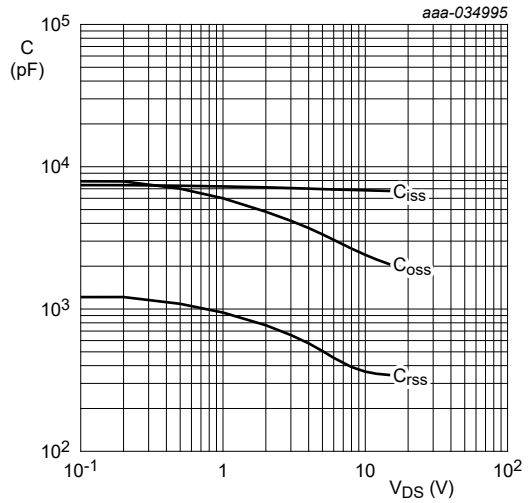
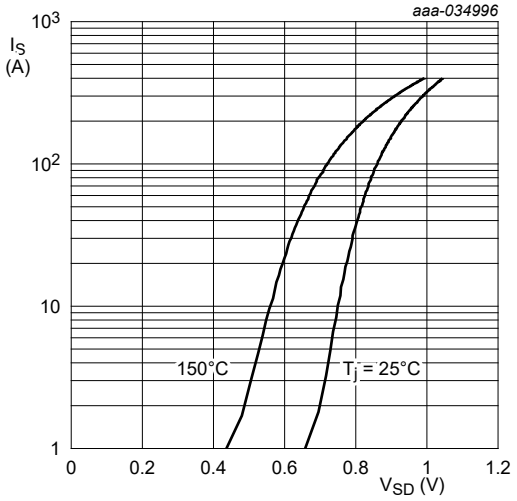



Fig. 13. Gate charge waveform definitions




$V_{GS}$ = 0 V; f = 1 MHz

Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values




$V_{GS}$ = 0 V

Fig. 15. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

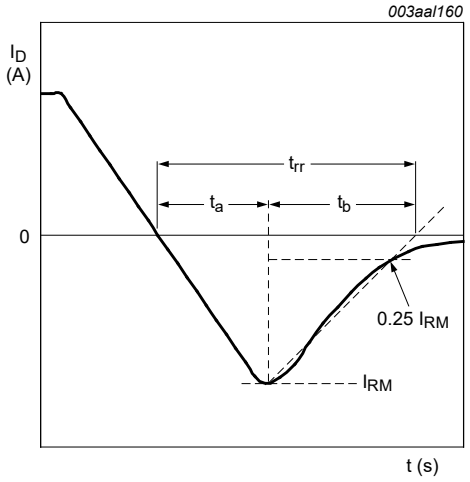
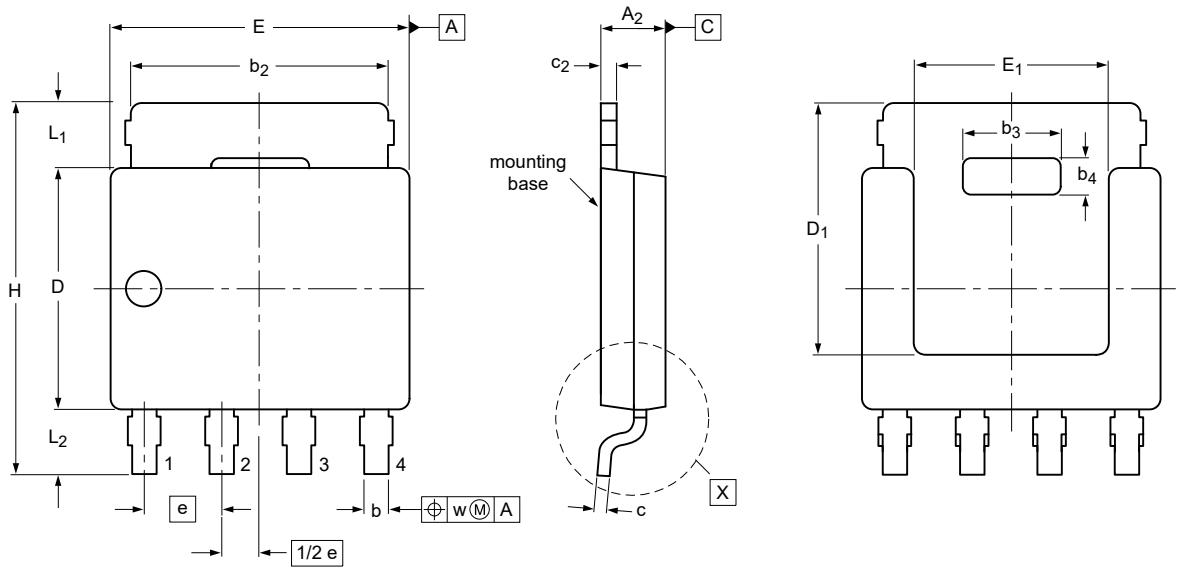



Fig. 16. Reverse recovery timing definition

# 11. Package outline

**Plastic single-ended surface-mounted package (LFPAK56; Power-SO8); 4 leads** **SOT669**




Dimensions (mm are the original dimensions)

| Unit(1) | | A | $A_1$ | $A_2$ | $A_3$ | b | $b_2$ | $b_3$ | $b_4$ | c | $c_2$ | D(1) | $D_1$(1) | E(1) | $E_1$(1) | e | H | L | $L_1$ | $L_2$ | w | y | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | max | 1.20 | 0.15 | 1.10 | | 0.50 | 4.41 | 2.2 | 0.9 | 0.25 | 0.30 | 4.10 | 4.20 | 5.0 | 3.3 | | 6.2 | 0.85 | 1.3 | 1.3 | | | 8° |
| | nom | | | | 0.25 | | | | | | | | | | | 1.27 | | | | | 0.25 | 0.1 | |
| | min | 1.01 | 0.00 | 0.95 | | 0.35 | 3.62 | 2.0 | 0.7 | 0.19 | 0.24 | 3.80 | | 4.8 | 3.1 | | 5.8 | 0.40 | 0.8 | 0.8 | | | 0° |

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

*sot669_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT669 | | MO-235 | | | | ~~11-03-25~~ 13-02-27 |

**Fig. 17. Package outline LFPAK56; Power-SO8 (SOT669)**

## 12. Soldering

**Footprint information for reflow soldering** **SOT669**

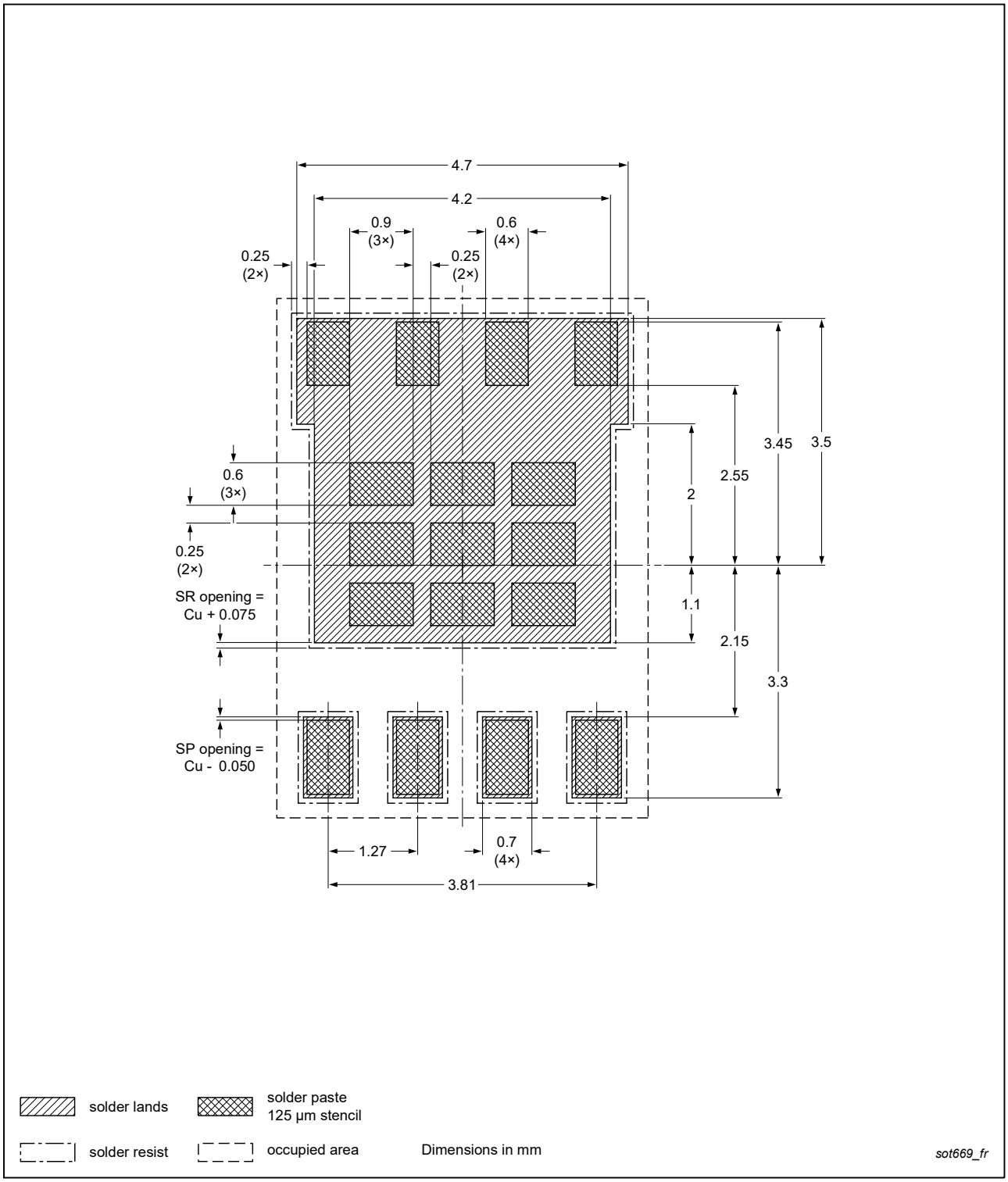



**Fig. 18. Reflow soldering footprint for LFPAK56; Power-SO8 (SOT669)**

**Wave soldering footprint information for LFPAK56 package** **SOT669**

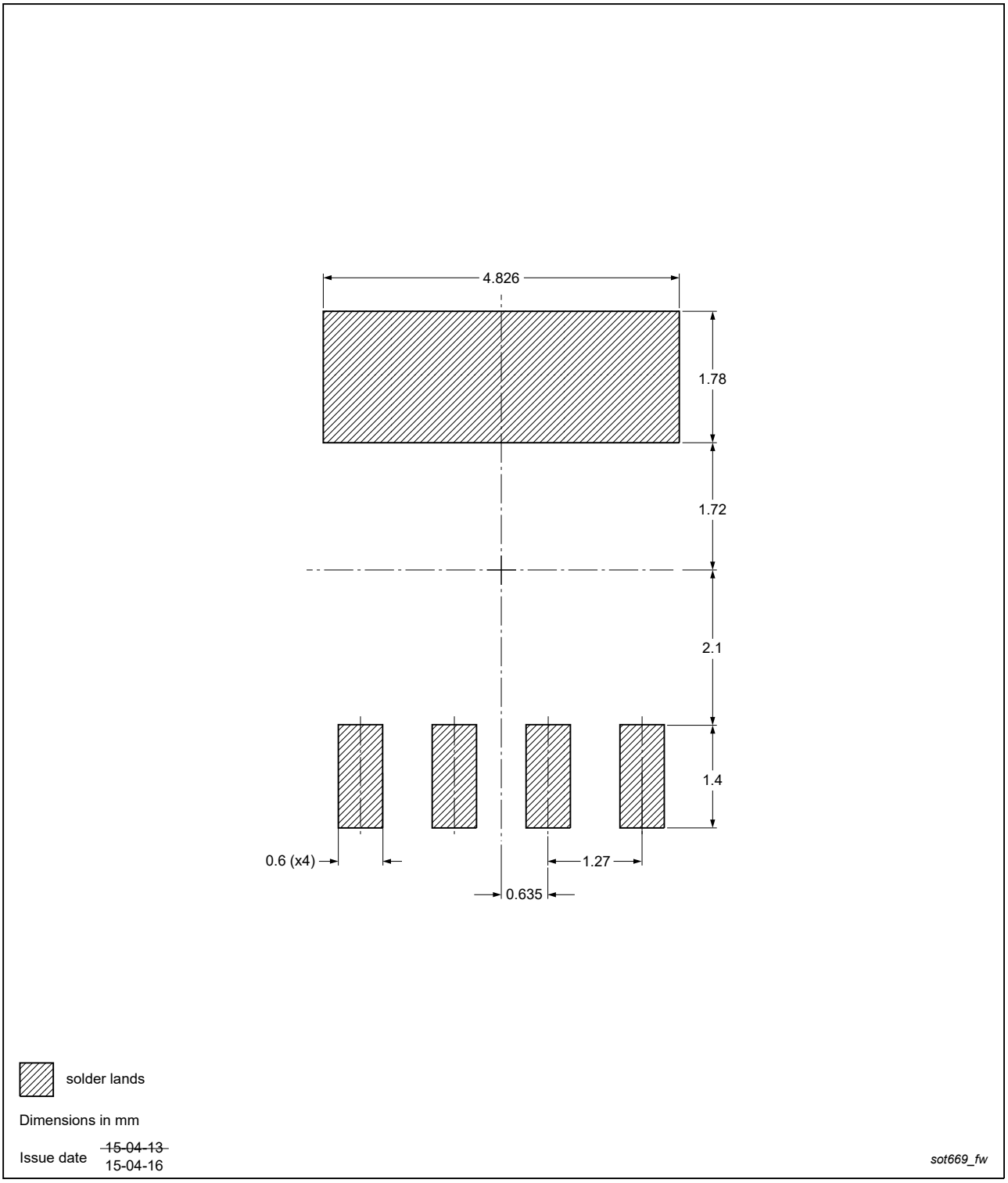



**Fig. 19. Wave soldering footprint for LFPAK56; Power-SO8 (SOT669)**

# 13. Legal information

## Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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