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Kind regards,

Team Nexperia

# PEMD30; PUMD30

## NPN/PNP double resistor-equipped transistors; R1 = 2.2 kΩ, R2 = open

Rev. 01 — 31 March 2006 Product data sheet

## 1. Product profile

### 1.1 General description

NPN/PNP double Resistor-Equipped Transistors (RET) in Surface-Mounted Device (SMD) plastic packages.

Table 1. Product overview

| Type number | Package | | PNP/PNP complement | NPN/NPN complement |
|---|---|---|---|---|
| | Philips | JEITA | | |
| PEMD30 | SOT666 | - | PEMB30 | PEMH30 |
| PUMD30 | SOT363 | SC-88 | PUMB30 | PUMH30 |

### 1.2 Features

- 100 mA output current capability
- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs

### 1.3 Applications

- Low current peripheral driver
- Control of IC inputs
- Cost-saving alternative for BC847BPN and BC847BVN
- Switching loads

### 1.4 Quick reference data

Table 2. Quick reference data

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Per transistor; for the PNP transistor with negative polarity** | | | | | | |
| $V_{CEO}$ | collector-emitter voltage | open base | - | - | 50 | V |
| $I_O$ | output current | | - | - | 100 | mA |
| R1 | bias resistor 1 (input) | | 1.54 | 2.2 | 2.86 | kΩ |

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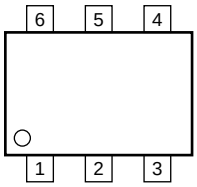
## 2. Pinning information

Table 3. Pinning

| Pin | Description | Simplified outline | Symbol |
|---|---|---|---|
| 1 | GND (emitter) TR1 | | |
| 2 | input (base) TR1 | | |
| 3 | output (collector) TR2 | | |
| 4 | GND (emitter) TR2 | | |
| 5 | input (base) TR2 | | |
| 6 | output (collector) TR1 | | |

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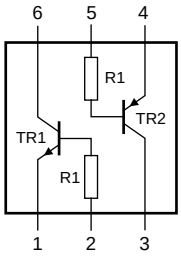


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## 3. Ordering information

Table 4. Ordering information

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| PEMD30 | - | plastic surface-mounted package; 6 leads | SOT666 |
| PUMD30 | SC-88 | plastic surface-mounted package; 6 leads | SOT363 |

## 4. Marking

Table 5. Marking codes

| Type number | Marking code[1] |
|---|---|
| PEMD30 | 2U |
| PUMD30 | *B3 |

[1] * = -: made in Hong Kong
* = p: made in Hong Kong
* = t: made in Malaysia
* = W: made in China

## 5. Limiting values

**Table 6. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| **Per transistor; for the PNP transistor with negative polarity** | | | | | | |
| $V_{CBO}$ | collector-base voltage | open emitter | | - | 50 | V |
| $V_{CEO}$ | collector-emitter voltage | open base | | - | 50 | V |
| $V_{EBO}$ | emitter-base voltage | open collector | | - | 5 | V |
| $I_O$ | output current | | | - | 100 | mA |
| $I_{CM}$ | peak collector current | single pulse; $t_p \leq 1$ ms | | - | 100 | mA |
| $P_{tot}$ | total power dissipation | $T_{amb} \leq 25$ °C | | | | |
| | SOT363 | | [1] | - | 200 | mW |
| | SOT666 | | [1][2] | - | 200 | mW |
| **Per device** | | | | | | |
| $P_{tot}$ | total power dissipation | $T_{amb} \leq 25$ °C | | | | |
| | SOT363 | | [1] | - | 300 | mW |
| | SOT666 | | [1][2] | - | 300 | mW |
| $T_{stg}$ | storage temperature | | | –65 | +150 | °C |
| $T_j$ | junction temperature | | | - | 150 | °C |
| $T_{amb}$ | ambient temperature | | | –65 | +150 | °C |

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

[2] Reflow soldering is the only recommended soldering method.

## 6. Thermal characteristics

**Table 7. Thermal characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Per transistor** | | | | | | | |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | | | | | |
| | SOT363 | | [1] | - | - | 625 | K/W |
| | SOT666 | | [1][2] | - | - | 625 | K/W |
| **Per device** | | | | | | | |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | | | | | |
| | SOT363 | | [1] | - | - | 416 | K/W |
| | SOT666 | | [1][2] | - | - | 416 | K/W |

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

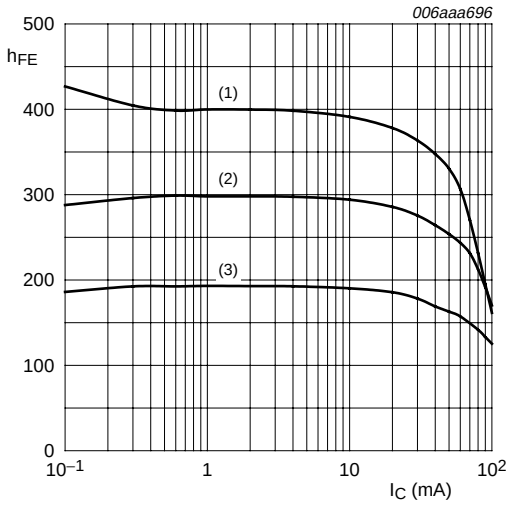
[2] Reflow soldering is the only recommended soldering method.

## 7. Characteristics

**Table 8. Characteristics**

*$T_{amb}$ = 25 °C unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Per transistor; for the PNP transistor with negative polarity** | | | | | | |
| $I_{CBO}$ | collector-base cut-off current | $V_{CB}$ = 50 V; $I_E$ = 0 A | - | - | 100 | nA |
| $I_{CEO}$ | collector-emitter cut-off current | $V_{CE}$ = 30 V; $I_B$ = 0 A | - | - | 1 | µA |
| | | $V_{CE}$ = 30 V; $I_B$ = 0 A; $T_j$ = 150 °C | - | - | 50 | µA |
| $I_{EBO}$ | emitter-base cut-off current | $V_{EB}$ = 5 V; $I_C$ = 0 A | - | - | 100 | nA |
| $h_{FE}$ | DC current gain | $V_{CE}$ = 5 V; $I_C$ = 20 mA | 30 | - | - | |
| $V_{CEsat}$ | collector-emitter saturation voltage | $I_C$ = 10 mA; $I_B$ = 0.5 mA | - | - | 150 | mV |
| R1 | bias resistor 1 (input) | | 1.54 | 2.2 | 2.86 | kΩ |
| $C_c$ | collector capacitance | $V_{CB}$ = 10 V; $I_E$ = $i_e$ = 0 A; f = 1 MHz | | | | |
| | TR1 (NPN) | | - | - | 2.5 | pF |
| | TR2 (PNP) | | - | - | 3 | pF |



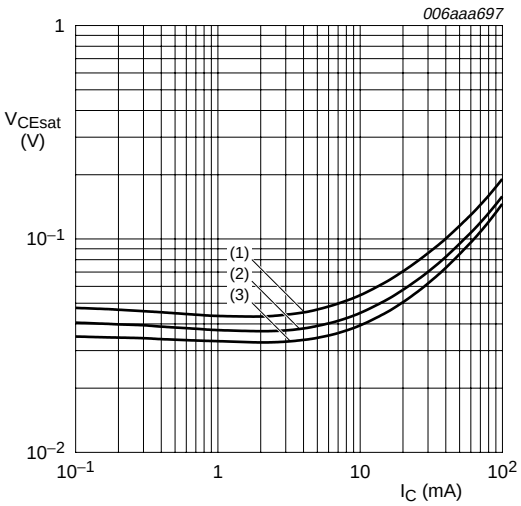

$V_{CE}$ = 5 V

(1) $T_{amb}$ = 100 °C

(2) $T_{amb}$ = 25 °C

(3) $T_{amb}$ = −40 °C

**Fig 1. TR1 (NPN): DC current gain as a function of collector current; typical values**



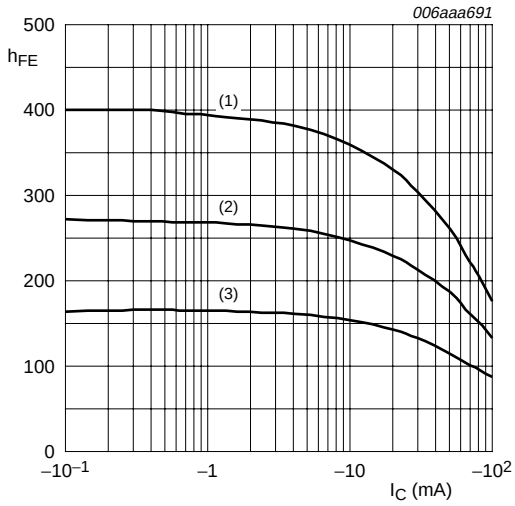

$I_C/I_B$ = 20

(1) $T_{amb}$ = 100 °C

(2) $T_{amb}$ = 25 °C

(3) $T_{amb}$ = −40 °C

**Fig 2. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values**



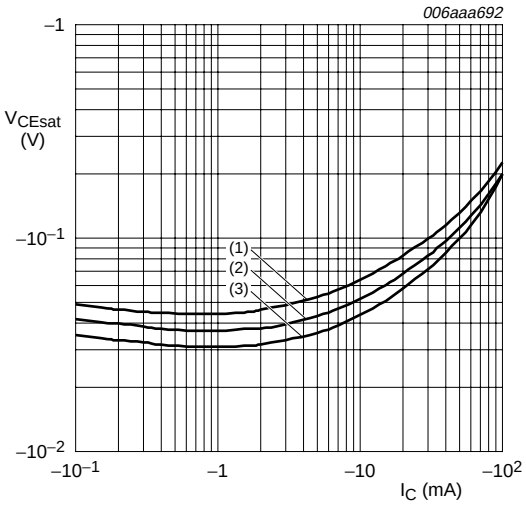

$V_{CE}$ = −5 V

(1) $T_{amb}$ = 100 °C

(2) $T_{amb}$ = 25 °C

(3) $T_{amb}$ = −40 °C

**Fig 3. TR2 (PNP): DC current gain as a function of collector current; typical values**




$I_C/I_B$ = 20

(1) $T_{amb}$ = 100 °C

(2) $T_{amb}$ = 25 °C

(3) $T_{amb}$ = −40 °C

**Fig 4. TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values**

## 8. Package outline

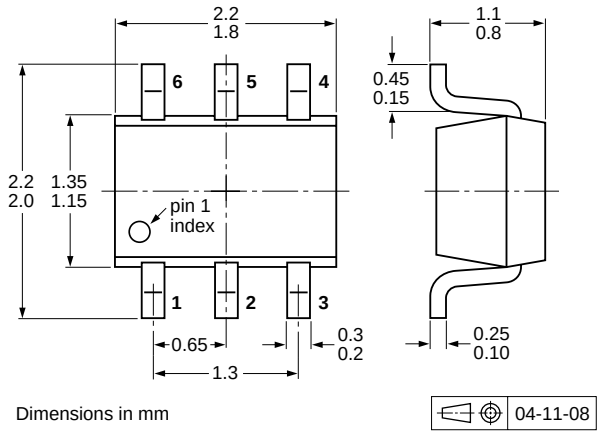



Fig 5. Package outline SOT363 (SC-88)

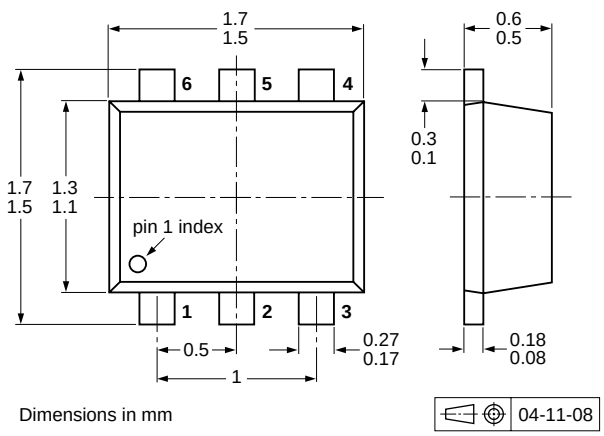



Fig 6. Package outline SOT666

## 9. Packing information

Table 9. Packing methods

*The indicated -xxx are the last three digits of the 12NC ordering code.*[1]

| Type number | Package | Description | Packing quantity | | | |
|---|---|---|---|---|---|---|
| | | | 3000 | 4000 | 8000 | 10000 |
| PEMD30 | SOT666 | 2 mm pitch, 8 mm tape and reel | - | - | -315 | - |
| | | 4 mm pitch, 8 mm tape and reel | - | -115 | - | - |
| PUMD30 | SOT363 | 4 mm pitch, 8 mm tape and reel; T1 [2] | -115 | - | - | -135 |
| | | 4 mm pitch, 8 mm tape and reel; T2 [3] | -125 | - | - | -165 |

[1] For further information and the availability of packing methods, see Section 13.

[2] T1: normal taping

[3] T2: reverse taping

## 10. Soldering

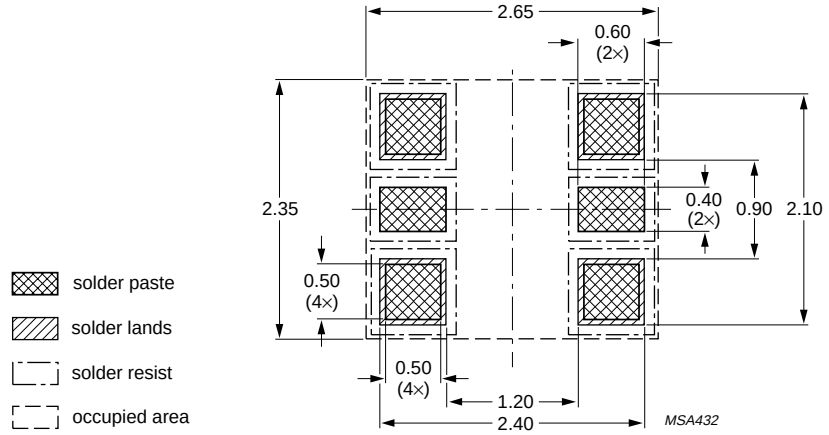



**Fig 7. Reflow soldering footprint SOT363 (SC-88)**

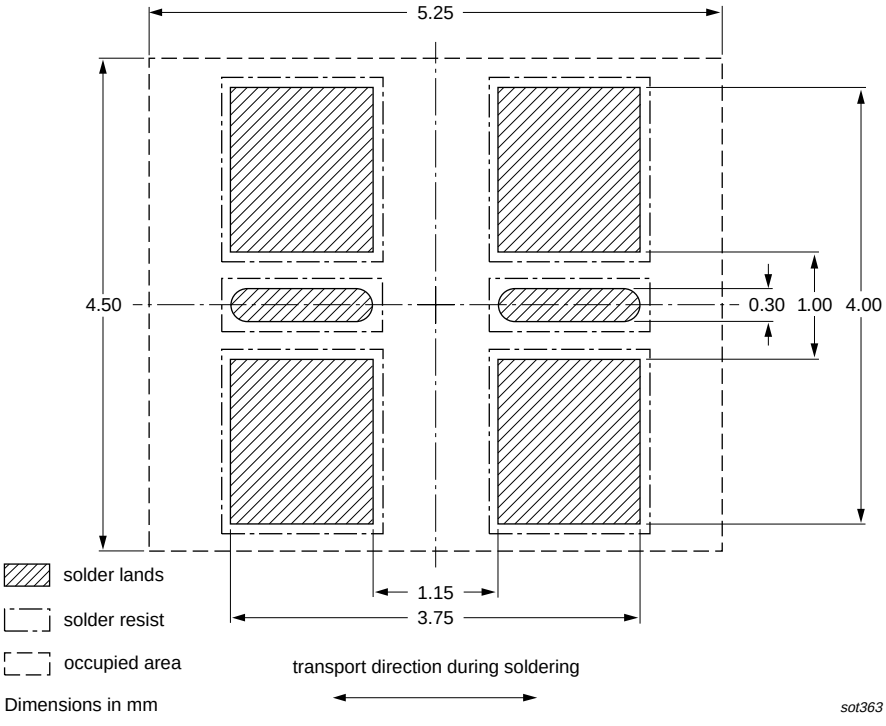
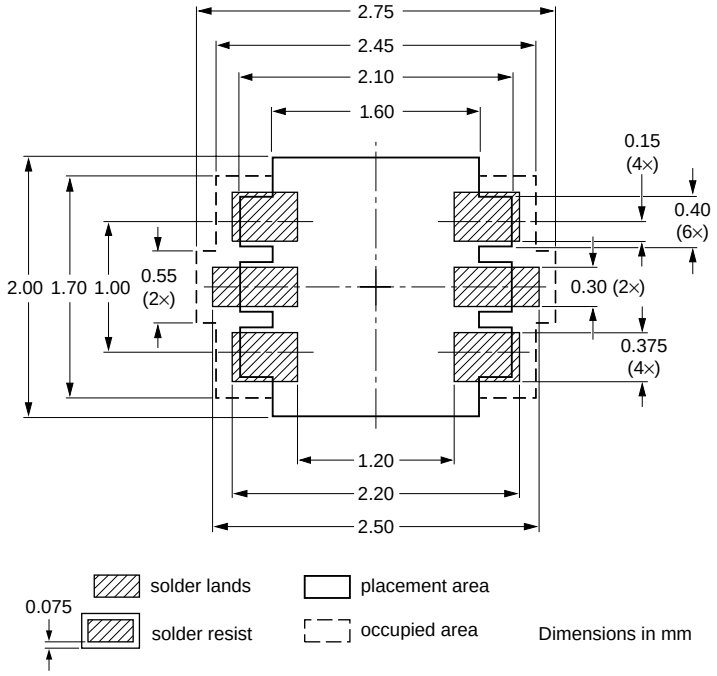



**Fig 8. Wave soldering footprint SOT363 (SC-88)**




Reflow soldering is the only recommended soldering method.

**Fig 9. Reflow soldering footprint SOT666**

## 11. Revision history

Table 10. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| PEMD30_PUMD30_1 | 20060331 | Product data sheet | - | - |

# 12. Legal information

## 12.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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**Date of release: 31 March 2006**

**Document identifier: PEMD30_PUMD30_1**

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